5 V, Slew-Rate Limited, Half-Duplex and Full-Duplex RS-485/RS-422 Transceivers

ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857

FEATURES

- EIA RS-485-/RS-422-compliant
- Data rate options
  - ADM4850/ADM4854: 115 kbps
  - ADM4851/ADM4855: 500 kbps
  - ADM4852/ADM4856: 2.5 Mbps
  - ADM4853/ADM4857: 10 Mbps
- Half- and full-duplex options
- Reduced slew rates for low EMI
- True fail-safe receiver inputs
- 5 µA (maximum) supply current in shutdown mode
- Up to 256 transceivers on one bus
- Outputs high-Z when disabled or powered off
- −7 V to +12 V bus common-mode range
- Thermal shutdown and short-circuit protection
- Pin-compatible with the MAX308x
- Specified over the −40°C to +85°C temperature range
- Available in 8-lead SOIC, LFCSP, and MSOP packages

APPLICATIONS

- Low power RS-485 applications
- EMI-sensitive systems
- DTE-DCE interfaces
- Industrial control
- Packet switching
- Local area networks
- Level translators

FUNCTIONAL BLOCK DIAGRAMS

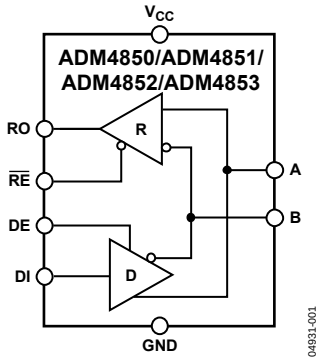

Figure 1.

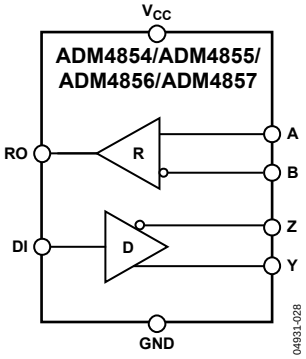

Figure 2.

GENERAL DESCRIPTION

The ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 are differential line transceivers suitable for high speed half- and full-duplex data communication on multipoint bus transmission lines. They are designed for balanced data transmission and comply with EIA Standards RS-485 and RS-422. The ADM4850/ADM4851/ADM4852/ADM4853 are half-duplex transceivers that share differential lines and have separate enable inputs for the driver and receiver. The full-duplex ADM4854/ADM4855/ADM4856/ADM4857 transceivers have dedicated differential line driver outputs and receiver inputs.

The parts have a 1/8-unit-load receiver input impedance, which allows up to 256 transceivers on one bus. Because only one driver should be enabled at any time, the output of a disabled or powered-down driver is three-stated to avoid overloading the bus.

The receiver inputs have a true fail-safe feature, which ensures a logic high output level when the inputs are open or shorted. This guarantees that the receiver outputs are in a known state before communication begins and when communication ends.

The driver outputs are slew-rate limited to reduce EMI and data errors caused by reflections from improperly terminated buses. Excessive power dissipation caused by bus contention or by output shorting is prevented with a thermal shutdown circuit.

The parts are fully specified over the commercial and industrial temperature ranges and are available in 8-lead SOIC, LFCSP (ADM4850/ADM4851/ADM4852/ADM4853), and MSOP (ADM4850 only) packages.

Table 1. Selection Table

Part No.	Half-/Full-Duplex	Data Rate
ADM4850	Half	115 kbps
ADM4851	Half	500 kbps
ADM4852	Half	2.5 Mbps
ADM4853	Half	10 Mbps
ADM4854	Full	115 kbps
ADM4855	Full	500 kbps
ADM4856	Full	2.5 Mbps
ADM4857	Full	10 Mbps

Rev. B

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Changes to Figure 29 ... 12
Change to Shutdown Mode Section ... 13
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 15

4/09—Rev. 0 to Rev. A

Changes to Ordering Guide ... 15

10/04—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}			V_{CC}	V	R = ∞, see Figure 18[1]
	2.0		5	V	R = 50 Ω (RS-422), see Figure 18
	1.5		5	V	R = 27 Ω (RS-485), see Figure 18
$\|V_{OD3}\|$	1.5		5	V	V_{TST} = −7 V to 12 V, see Figure 19
$\Delta\|V_{OD}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, see Figure 18
Common-Mode Output Voltage, V_{OC}			3	V	R = 27 Ω or 50 Ω, see Figure 18
$\Delta\|V_{OC}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, see Figure 18
Output Short-Circuit Current, V_{OUT} = High	−200		+200	mA	−7 V < V_{OUT} < +12 V
Output Short-Circuit Current, V_{OUT} = Low	−200		+200	mA	−7 V < V_{OUT} < +12 V
DRIVER INPUT LOGIC					
CMOS Input Logic Threshold Low			0.8	V	
CMOS Input Logic Threshold High	2.0			V	
CMOS Logic Input Current (DI)			±1	µA	
DE Input Resistance to GND		220		kΩ	
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	−200	−125	−30	mV	−7 V < V_{OC} < +12 V
Input Hysteresis		20		mV	−7 V < V_{OC} < +12 V
Input Resistance (A, B)	96	150		kΩ	−7 V < V_{OC} < +12 V
Input Current (A, B)			0.125	mA	V_{IN} = +12 V
			−0.1	mA	V_{IN} = −7 V
CMOS Logic Input Current ($\overline{RE}$)			±1	µA	
CMOS Output Voltage Low			0.4	V	I_{OUT} = +4 mA
CMOS Output Voltage High	4.0			V	I_{OUT} = −4 mA
Output Short-Circuit Current	7		85	mA	V_{OUT} = GND or V_{CC}
Three-State Output Leakage Current			±2	µA	0.4 V ≤ V_{OUT} ≤ 2.4 V
POWER SUPPLY CURRENT					
115 kbps Options (ADM4850/ADM4854)			5	µA	DE = 0 V, $\overline{RE}$ = V_{CC} (shutdown)
		36	60	µA	DE = 0 V, $\overline{RE}$ = 0 V
		100	160	µA	DE = V_{CC}
500 kbps Options (ADM4851/ADM4855)			5	µA	DE = 0 V, $\overline{RE}$ = V_{CC} (shutdown)
		80	120	µA	DE = 0 V, $\overline{RE}$ = 0 V
		120	200	µA	DE = V_{CC}
2.5 Mbps Options (ADM4852/ADM4856)			5	µA	DE = 0 V, $\overline{RE}$ = V_{CC} (shutdown)
		250	400	µA	DE = 0 V, $\overline{RE}$ = 0 V
		320	500	µA	DE = V_{CC}
10 Mbps Options (ADM4853/ADM4857)			5	µA	DE = 0 V, $\overline{RE}$ = V_{CC} (shutdown)
		250	400	µA	DE = 0 V, $\overline{RE}$ = 0 V
		320	500	µA	DE = V_{CC}

[1] Guaranteed by design.

ADM4850/ADM4854 TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Maximum Data Rate	115			kbps	
Propagation Delay, t_{PLH}, t_{PHL}	600		2500	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 20
Skew, t_{SKEW}			70	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 20
Rise/Fall Times, t_R, t_F	600		2400	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 20
Enable Time, t_{ZH}			2000	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 21, ADM4850
Disable Time, t_{ZL}			2000	ns	R_L = 500 Ω, C_L = 15 pF, see Figure 21, ADM4850
Enable Time from Shutdown		4000		ns	R_L = 500 Ω, C_L = 100 pF, see Figure 21, ADM4850
RECEIVER					
Propagation Delay, t_{PLH}, t_{PHL}	400		1000	ns	C_L = 15 pF, see Figure 22
Differential Skew, t_{SKEW}			255	ns	C_L = 15 pF, see Figure 22
Enable Time		5	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 23, ADM4850
Disable Time		20	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 23, ADM4850
Enable Time from Shutdown		4000		ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 23, ADM4850
Time to Shutdown	50	330	3000	ns	ADM4850[1]

[1] The half-duplex device is put into shutdown mode by driving $\overline{RE}$ high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

ADM4851/ADM4855 TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Maximum Data Rate	500			kbps	
Propagation Delay, t_{PLH}, t_{PHL}	250		600	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 20
Skew, t_{SKEW}			40	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 20
Rise/Fall Times, t_R, t_F	200		600	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 20
Enable Time, t_{ZH}			1000	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 21, ADM4851
Disable Time, t_{ZL}			1000	ns	R_L = 500 Ω, C_L = 15 pF, see Figure 21, ADM4851
Enable Time from Shutdown		4000		ns	R_L = 500 Ω, C_L = 100 pF, see Figure 21, ADM4851
RECEIVER					
Propagation Delay, t_{PLH}, t_{PHL}	400		1000	ns	C_L = 15 pF, see Figure 22
Differential Skew, t_{SKEW}			250	ns	C_L = 15 pF, see Figure 22
Enable Time		5	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 23, ADM4851
Disable Time		20	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 23, ADM4851
Enable Time from Shutdown		4000		ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 23, ADM4851
Time to Shutdown	50	330	3000	ns	ADM4851[1]

[1] The half-duplex device is put into shutdown mode by driving $\overline{RE}$ high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

ADM4852/ADM4856 TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Maximum Data Rate	2.5			Mbps	
Propagation Delay, t_{PLH}, t_{PHL}	50		180	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 20
Skew, t_{SKEW}			50	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 20
Rise/Fall Times, t_R, t_F			140	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 20
Enable Time, t_{ZH}			180	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 21, ADM4852
Disable Time, t_{ZL}			180	ns	R_L = 500 Ω, C_L = 15 pF, see Figure 21, ADM4852
Enable Time from Shutdown		4000		ns	R_L = 500 Ω, C_L = 100 pF, see Figure 21, ADM4852
RECEIVER					
Propagation Delay, t_{PLH}, t_{PHL}	55		190	ns	C_L = 15 pF, see Figure 22
Differential Skew, t_{SKEW}			50	ns	C_L = 15 pF, see Figure 22
Enable Time		5	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 23, ADM4852
Disable Time		20	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 23, ADM4852
Enable Time from Shutdown		4000		ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 23, ADM4852
Time to Shutdown	50	330	3000	ns	ADM4852[1]

[1] The half-duplex device is put into shutdown mode by driving $\overline{RE}$ high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

ADM4853/ADM4857 TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Maximum Data Rate	10			Mbps	
Propagation Delay, t_{PLH}, t_{PHL}	0		30	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 20
Skew, t_{SKEW}			10	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 20
Rise/Fall Times, t_R, t_F			30	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 20
Enable Time, t_{ZH}			35	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 21, ADM4853
Disable Time, t_{ZL}			35	ns	R_L = 500 Ω, C_L = 15 pF, see Figure 21, ADM4853
Enable Time from Shutdown		4000		ns	R_L = 500 Ω, C_L = 100 pF, see Figure 21, ADM4853
RECEIVER					
Propagation Delay, t_{PLH}, t_{PHL}	55		190	ns	C_L = 15 pF, see Figure 22
Differential Skew, t_{SKEW}			30	ns	C_L = 15 pF, see Figure 22
Enable Time		5	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 23, ADM4853
Disable Time		20	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 23, ADM4853
Enable Time from Shutdown		4000		ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 23, ADM4853
Time to Shutdown	50	330	3000	ns	ADM4853[1]

[1] The half-duplex device is put into shutdown mode by driving $\overline{RE}$ high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
V_{CC} to GND	6 V
Digital I/O Voltage (DE, $\overline{RE}$, DI, RO)	−0.3 V to V_{CC} + 0.3 V
Driver Output/Receiver Input Voltage	−9 V to +14 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
θ_{JA} Thermal Impedance	
SOIC	110°C/W
LFCSP	62°C/W
MSOP	133.1°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

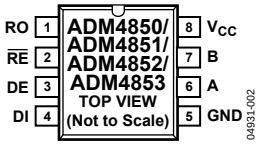

Figure 3. ADM4850/ADM4851/ADM4852/ADM4853 Pin Configuration, SOIC and MSOP

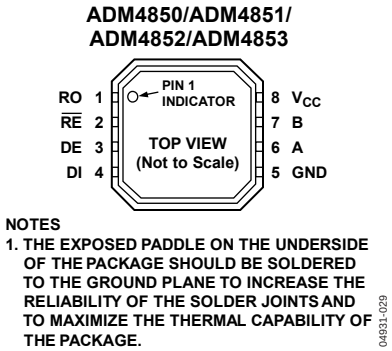

Figure 4. ADM4850/ADM4851/ADM4852/ADM4853 Pin Configuration, LFCSP

Table 8. ADM4850/ADM4851/ADM4852/ADM4853 Pin Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output. When RO is enabled, if (A − B) ≥ −30 mV, RO = high; if (A − B) ≤ −200 mV, RO = low.
2	$\overline{RE}$	Receiver Output Enable. A low level on this pin enables the receiver output, RO. A high level places RO into a high impedance state.
3	DE	Driver Output Enable. A high level on this pin enables the driver differential inputs, A and B. A low level places them into a high impedance state.
4	DI	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high, whereas a logic high on DI forces A high and B low.
5	GND	Ground.
6	A	Noninverting Receiver Input A/Noninverting Driver Output A.
7	B	Inverting Receiver Input B/Inverting Driver Output B.
8	V_{CC}	5 V Power Supply.

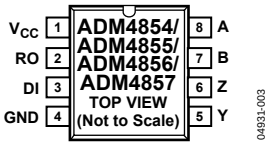

Figure 5. ADM4854/ADM4855/ADM4856/ADM4857 Pin Configuration, SOIC

Table 9. ADM4854/ADM4855/ADM4856/ADM4857 Pin Descriptions

Pin No.	Mnemonic	Description
1	V_{CC}	5 V Power Supply.
2	RO	Receiver Output. When RO is enabled, if (A − B) ≥ −30 mV, RO = high; if (A − B) ≤ −200 mV, RO = low.
3	DI	Driver Input. When the driver is enabled, a logic low on DI forces Y low and Z high, whereas a logic high on DI forces Y high and Z low.
4	GND	Ground.
5	Y	Noninverting Driver Output.
6	Z	Inverting Driver Output.
7	B	Inverting Receiver Input.
8	A	Noninverting Receiver Input.

TYPICAL PERFORMANCE CHARACTERISTICS

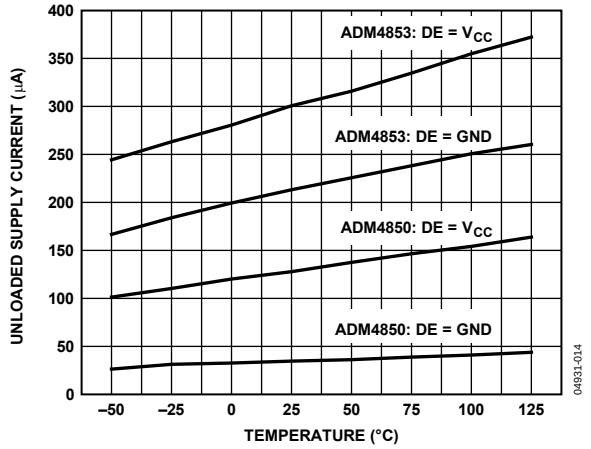

Figure 6. Unloaded Supply Current vs. Temperature

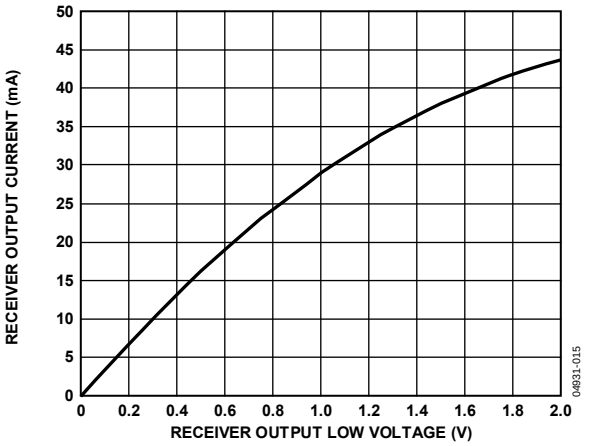

Figure 7. Receiver Output Current vs. Receiver Output Low Voltage

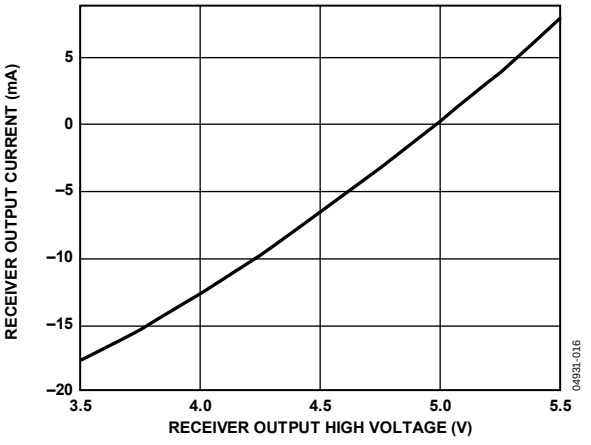

Figure 8. Receiver Output Current vs. Receiver Output High Voltage

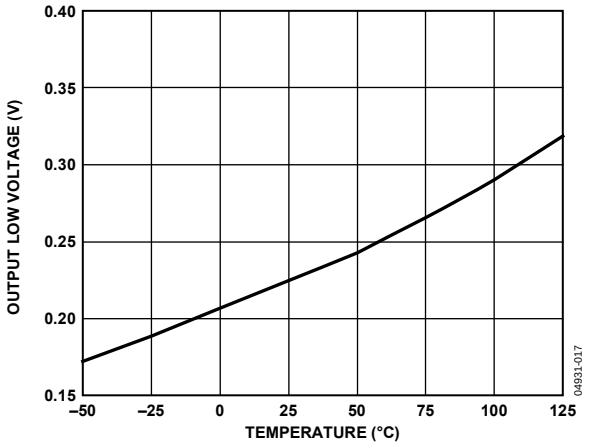

Figure 9. Receiver Output Low Voltage vs. Temperature

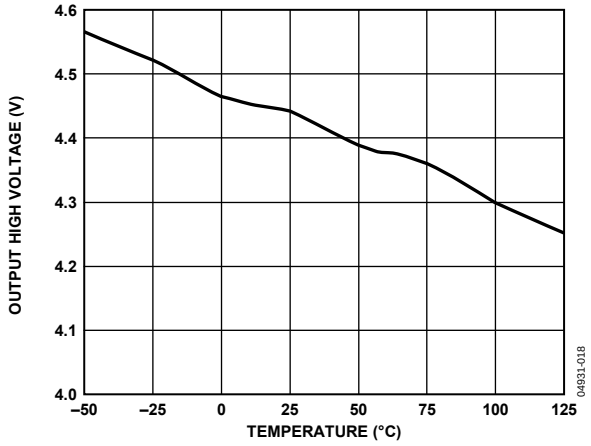

Figure 10. Receiver Output High Voltage vs. Temperature

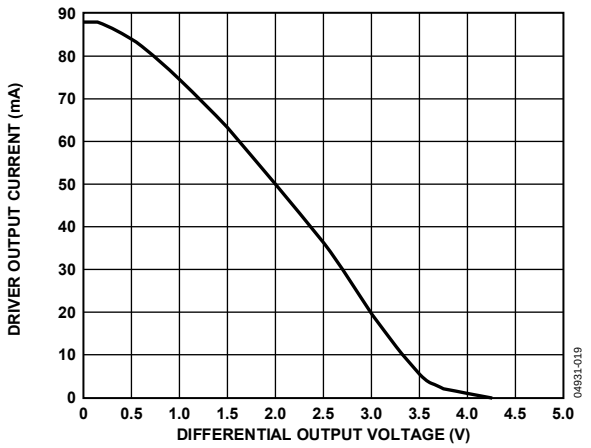

Figure 11. Driver Output Current vs. Differential Output Voltage

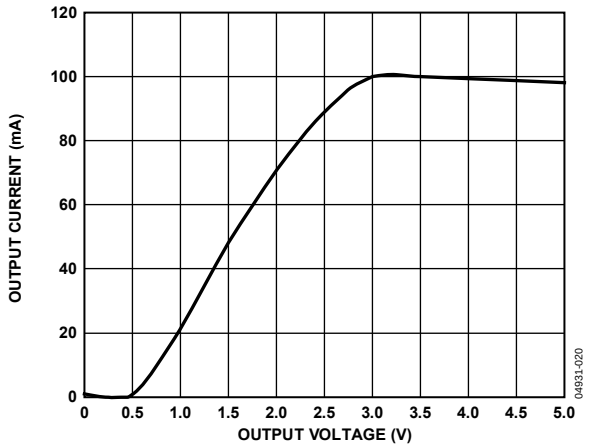

Figure 12. Output Current vs. Driver Output Low Voltage

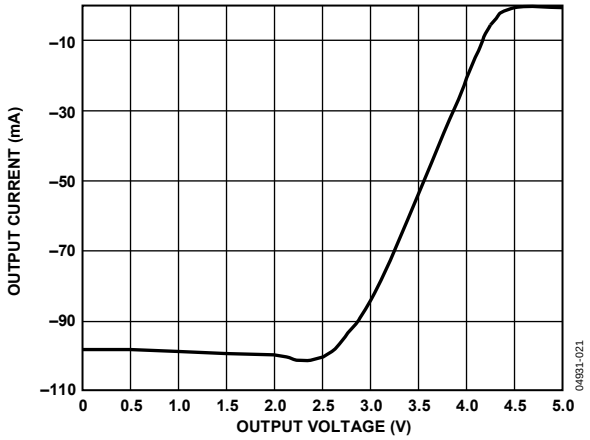

Figure 13. Output Current vs. Driver Output High Voltage

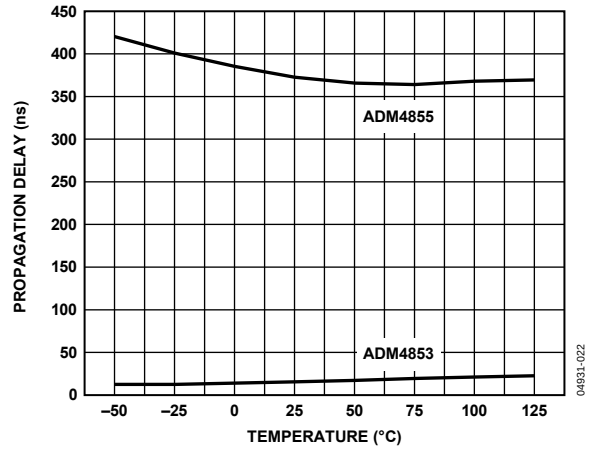

Figure 14. Driver Propagation Delay vs. Temperature

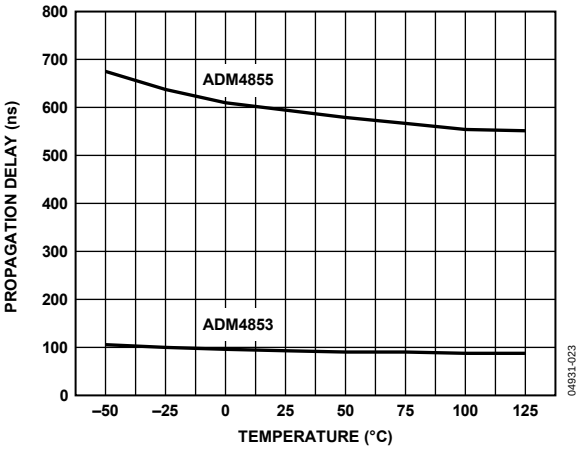

Figure 15. Receiver Propagation Delay vs. Temperature

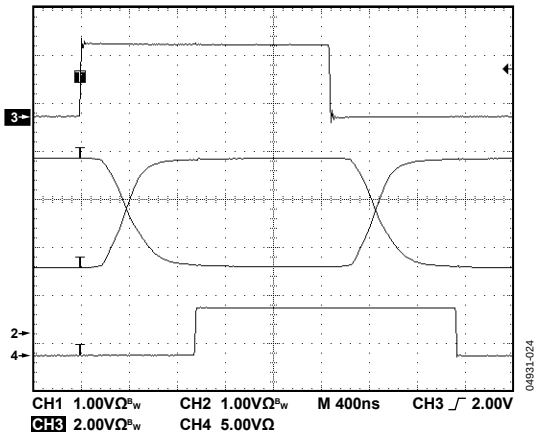

Figure 16. Driver/Receiver Propagation Delay (ADM4855, 500 kbps)

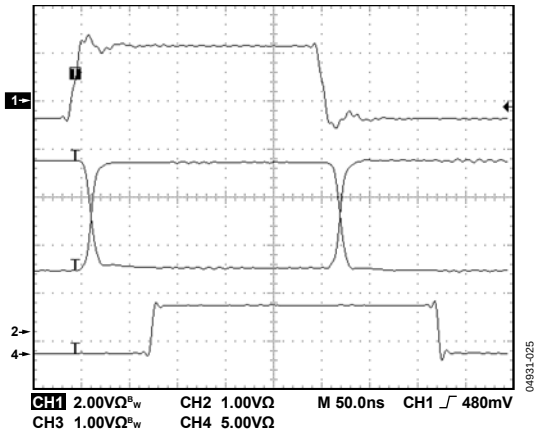

Figure 17. Driver/Receiver Propagation Delay (ADM4857, 4 Mbps)

TEST CIRCUITS

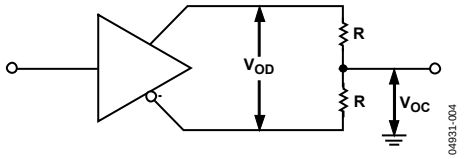

Figure 18. Driver Voltage Measurement

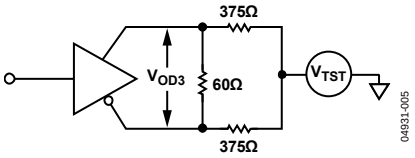

Figure 19. Driver Voltage Measurement over Common-Mode Voltage Range

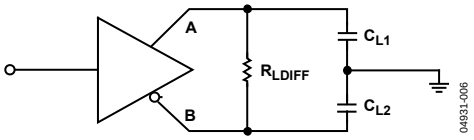

Figure 20. Driver Propagation Delay

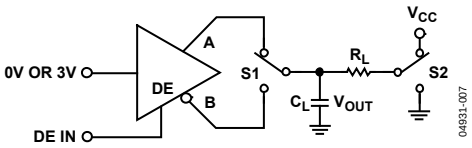

Figure 21. Driver Enable/Disable

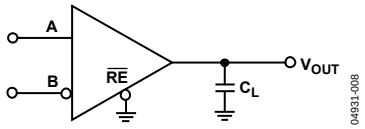

Figure 22. Receiver Propagation Delay

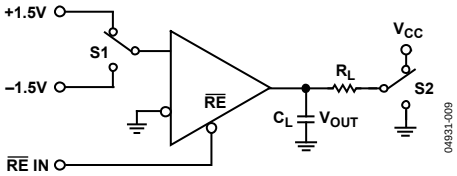

Figure 23. Receiver Enable/Disable

SWITCHING CHARACTERISTICS

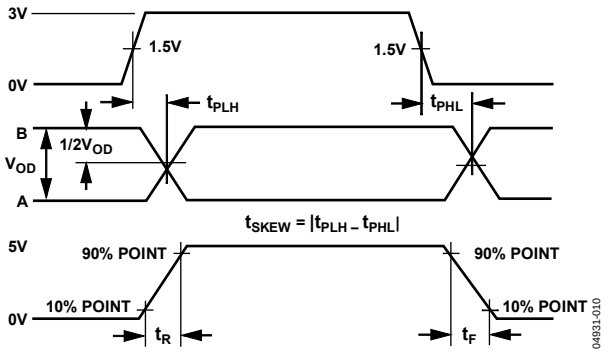

Figure 24. Driver Propagation Delay, Rise/Fall Timing

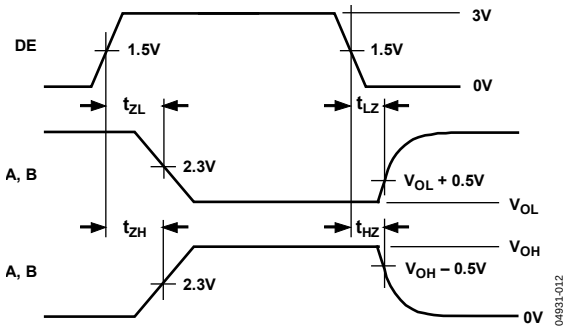

Figure 26. Driver Enable/Disable Timing

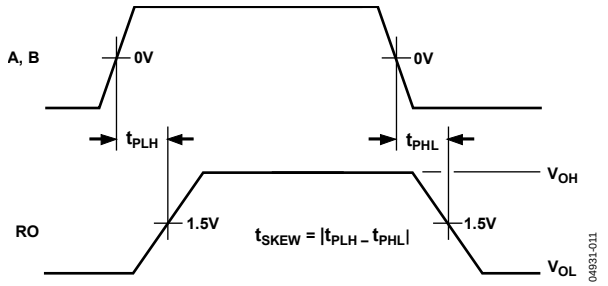

Figure 25. Receiver Propagation Delay

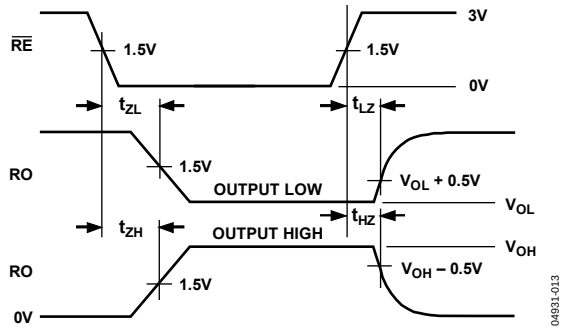

Figure 27. Receiver Enable/Disable Timing

CIRCUIT DESCRIPTION

The ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 are high speed RS-485/RS-422 transceivers offering enhanced performance over industry-standard devices. All devices in the family contain one driver and one receiver, but offer a choice of performance options. The devices feature true fail-safe operation, which means that a logic high receiver output is guaranteed when the receiver inputs are open-circuit or short-circuit, or when they are connected to a terminated transmission line with all drivers disabled (see the Fail-Safe Operation section).

SLEW-RATE CONTROL

The ADM4850 and ADM4854 feature a controlled slew-rate driver that minimizes electromagnetic interference (EMI) and reduces reflections caused by incorrectly terminated cables, allowing error-free data transmission rates up to 115 kbps. The ADM4851 and ADM4855 offer a higher limit on driver output slew rate, allowing data transmission rates up to 500 kbps. The driver slew rates of the ADM4852 and ADM4856 and the ADM4853 and ADM4857 are not limited, offering data transmission rates up to 2.5 Mbps and 10 Mbps, respectively.

RECEIVER INPUT FILTERING

The receivers of all the devices incorporate input hysteresis. In addition, the receivers of the 115 kbps ADM4850 and ADM4854 and the 500 kbps ADM4851 and ADM4855 incorporate input filtering. This enhances noise immunity with differential signals that have very slow rise and fall times. However, it causes the propagation delay to increase by 20%.

HALF-/FULL-DUPLEX OPERATION

Half-duplex operation implies that the transceiver can transmit and receive, but it can do only one of these at any given time. However, with full-duplex operation, the transceiver can transmit and receive simultaneously. The ADM4850/ADM4851/ADM4852/ADM4853 are half-duplex devices in which the driver and the receiver share differential bus terminals. The ADM4854/ADM4855/ADM4856/ADM4857 are full-duplex devices that have dedicated driver output and receiver input pins. Figure 28 and Figure 29 show typical half- and full-duplex topologies.

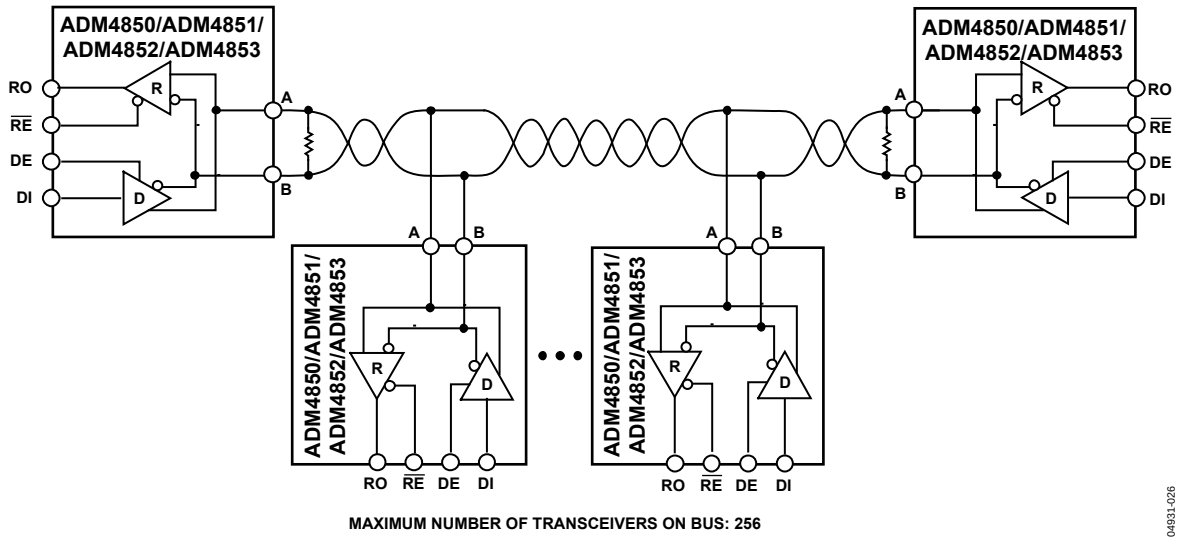

Figure 28. Typical Half-Duplex RS-485 Network Topology

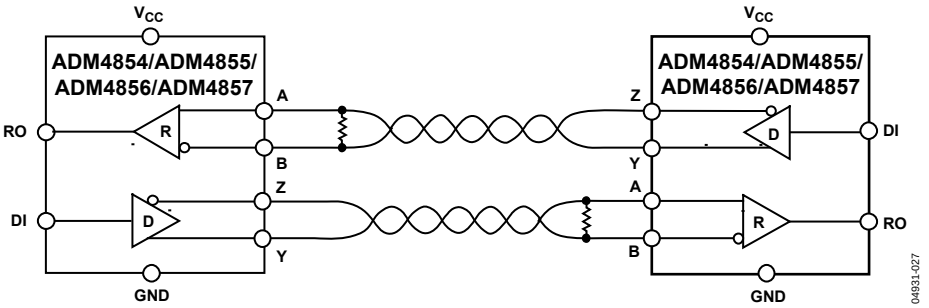

Figure 29. Typical Full-Duplex Point-to-Point RS-485 Network Topology

HIGH RECEIVER INPUT IMPEDANCE

The input impedance of the ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 receivers is 96 kΩ, which is eight times higher than the standard RS-485 unit load of 12 kΩ. This 96 kΩ impedance enables a standard driver to drive 32 unit loads or to be connected to 256 ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 receivers. An RS-485 bus, driven by a single standard driver, can be connected to a combination of ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 devices and standard unit load receivers, up to an equivalent of 32 standard unit loads.

THREE-STATE BUS CONNECTION

The half-duplex parts (ADM4850/ADM4851/ADM4852/ADM4853) have a driver enable (DE) pin that enables the driver outputs when taken high, or puts the driver outputs into a high impedance state when taken low. Similarly, the half-duplex devices have an active low receiver enable ($\overline{RE}$) pin. Taking this pin low enables the receiver, whereas taking it high puts the receiver outputs into a high impedance state. This allows several driver outputs to be connected to an RS-485 bus. Note that only one driver should be enabled at a time, but that many receivers can be enabled.

SHUTDOWN MODE

The ADM4850/ADM4851/ADM4852/ADM4853 have a low power shutdown mode, which is enabled by taking $\overline{RE}$ high and DE low. If shutdown mode is not used, the fact that DE is active high and $\overline{RE}$ is active low offers a convenient way of switching the device between transmit and receive by tying DE and $\overline{RE}$ together.

If DE is driven low and $\overline{RE}$ is driven high for less than 50 ns, the devices are guaranteed not to enter shutdown mode. If DE is driven low and $\overline{RE}$ is driven high for at least 3000 ns, the devices are guaranteed to enter shutdown mode.

FAIL-SAFE OPERATION

The ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 offer true fail-safe operation while remaining fully compliant with the ±200 mV EIA/TIA-485 standard. A logic high receiver output is generated when the receiver inputs are shorted together or open circuit, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver threshold between −30 mV and −200 mV. If the differential receiver input voltage (A − B) is greater than or equal to −30 mV, RO is logic high. If (A − B) is less than or equal to −200 mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the differential input voltage of the receiver is pulled to 0 V by the internal circuitry of the ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857, which results in a logic high with 30 mV minimum noise margin.

CURRENT LIMIT AND THERMAL SHUTDOWN

The ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 incorporate two protection mechanisms to guard the drivers against short circuits, bus contention, or other fault conditions. The first is a current limiting output stage, which protects the driver against short circuits over the entire common-mode voltage range by limiting the output current to approximately 70 mA. Under extreme fault conditions where the current limit is not effective, a thermal shutdown circuit puts the driver outputs into a high impedance state if the die temperature exceeds 150°C, and does not turn them back on until the temperature falls to 130°C.

OUTLINE DIMENSIONS

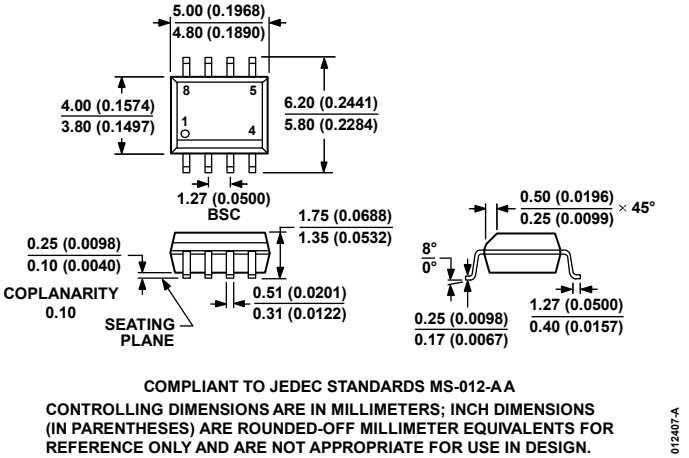

Figure 30. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

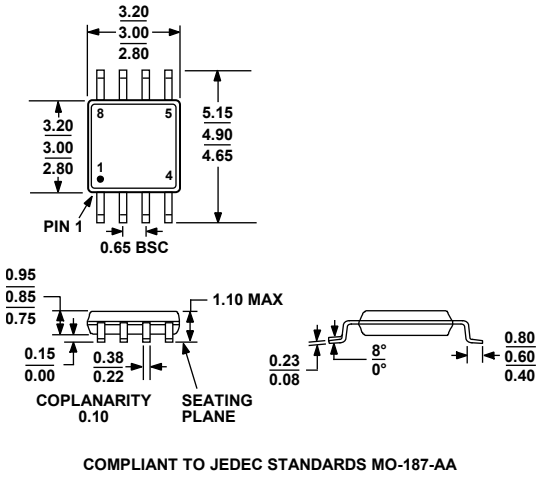

Figure 31. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

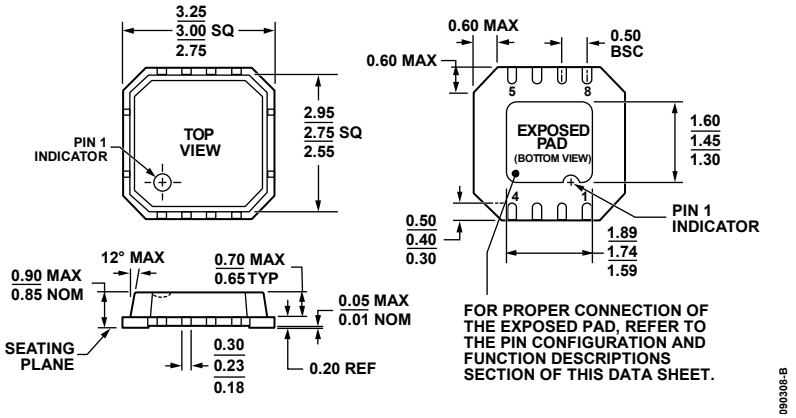

Figure 32. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADM4850ACP-REEL7	−40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	M0R
ADM4850ACPZ-REEL7[1]	−40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	M8Q
ADM4850AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4850ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4850ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4850ARMZ[1]	−40°C to +85°C	8-Lead MSOP	RM-8	MQ8
ADM4850ARMZ-REEL7[1]	−40°C to +85°C	8-Lead MSOP	RM-8	MQ8
ADM4851ACP-REEL7	−40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	M0S
ADM4851AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4851AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4851ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4851ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4852ACP-REEL7	−40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	M0T
ADM4852ACPZ-REEL7[1]	−40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	M9M
ADM4852AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4852AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4852ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4853ACP-REEL7	−40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	M0U
ADM4853ACPZ-REEL7[1]	−40°C to +85°C	8-Lead LFCSP_VD	CP-8-2	F0B
ADM4853AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4853AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4853ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4853ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4854AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4854AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4854ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4855AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4855AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4855ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4856AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4856AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4856ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4856ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4857AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4857AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4857ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
ADM4857ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	

[1] Z = RoHS Compliant Part.

NOTES

D04931-0-7/09(B)