

## MIXED SIGNAL MICROCONTROLLER

Check for Samples: [AFE4110](#)

### FEATURES

- **Ultra Low Supply-Voltage (ULV) Range**
  - 1.1V - 1.55V Unregulated Single Cell Battery Operation (CPU, System Core, and Timers)
  - 3mA 1.85V Internal Charge Pump for External EEPROM (R/W), VDDIO, and Internal LCD Controller
  - 60 $\mu$ A 3.3V Regulated Charge Pump for LCD Drive Pads
- **Low Power Consumption**
  - Active Mode (AM): 45 $\mu$ A/MHz (1.55V)
  - Standby Mode (LPM3, LCD): < 25 $\mu$ A
  - Deep Sleep Mode (LPM5): < 0.4 $\mu$ A
  - 8-Bytes Battery Backed RAM for Calibration Retention
  - Wakeup From Periodic Timer or External Interrupt
  - Wake-Up from LPM5 in 10ms, Wake-Up from LPM4 in 5 $\mu$ s
- **16-Bit RISC Architecture**
  - Extended Instructions
  - 125ns Instruction Cycle Time
- **Compact Clock System**
  - Internal Trimmable High Frequency Clock Oscillator with Discrete Frequency Selections Between 1MHz and 5.4MHz
  - 20kHz Internal low Frequency Clock Oscillator
  - External Clock Input (Upto 8MHz)
  - 32kHz Crystal Oscillator
- **Internal High Frequency Oscillator Frequency Correction**
  - Facilitates Generation and Measurement of Real Time Intervals Without a Clock Crystal
  - Utilizes Factory Calibration (E-Fuse), S/W, and a Single External 1M $\Omega$  Resistor
- **Integrated LCD Controller**
  - Drives 4-Mux, 3-Mux, 2-Mux, or Static Mode LCDs
  - Up to 48 (4x12) LCD Segments
- **Two 16-Bit Timer0\_A3 with Three Capture/Compare Registers**
  - Extended Input Multiplexer for High Accuracy RC Discharge Measurement
- **ULV Analog Pool**
  - 8-Bit Analog-to-Digital Converter (ADC)
  - 8-Bit Digital-to-Analog Converter (DAC)
  - Programmable Comparator (COMP)
  - Supply-Voltage-Monitoring (SVM)
  - Internal Temperature Sensor
  - Internal Voltage Reference
  - 1V Regulated (LDO) Outputs
- **32-Bit Watch-Dog-Timer (WDT-A)**
- **21-Configurable Analog I/O or Digital GPIO Pads,**
  - 2-Power GPIO for 10mA V<sub>DD</sub>/1.85/3.6V Buzzer Load
  - 10-GPIO for VDDIO Operation with V<sub>DD</sub>/1.85/3.6V Internal Level Shifting
  - 11-GPIO for VDD Operation (1.1V - 1.55V)
  - 4-Regulated 1V (LDO) Analog Outputs
  - 1-250mV DAC Analog Output
  - 6-Analog Comparator/ADC Inputs
- **SPI EEPROM Bootstrap Loader (AFE4110A)**
- **Full Four Wire JTAG Debug Interface**
- **Family Members Include:**
  - **AFE4110B:**
    - 512B RAM Memory
    - 16KB ROM (TI PSUC, Custom)
  - **AFE4110A:**
    - 14KB RAM + 512B RAM
    - 16KB ROM (TI DSUC, TI Bootloader)
- **55-Bonding Pads Available as Tested Wafers, See the Ordering Information for Other Options**

### APPLICATIONS

- For any application requiring a full analog signal chain and an LCD display driver such as digital thermometers, pedometers, thermostats, and other portable single alkaline battery devices.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# AFE4110

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[www.ti.com](http://www.ti.com)


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION

The Texas Instruments MSP430 family of low-power mixed signal ASSPs consists of many devices featuring different sets of peripherals targeted for various consumer medical applications. The AFE4110 CPU architecture is based on the popular ultra low power Texas Instruments MSP430 RISC processor.

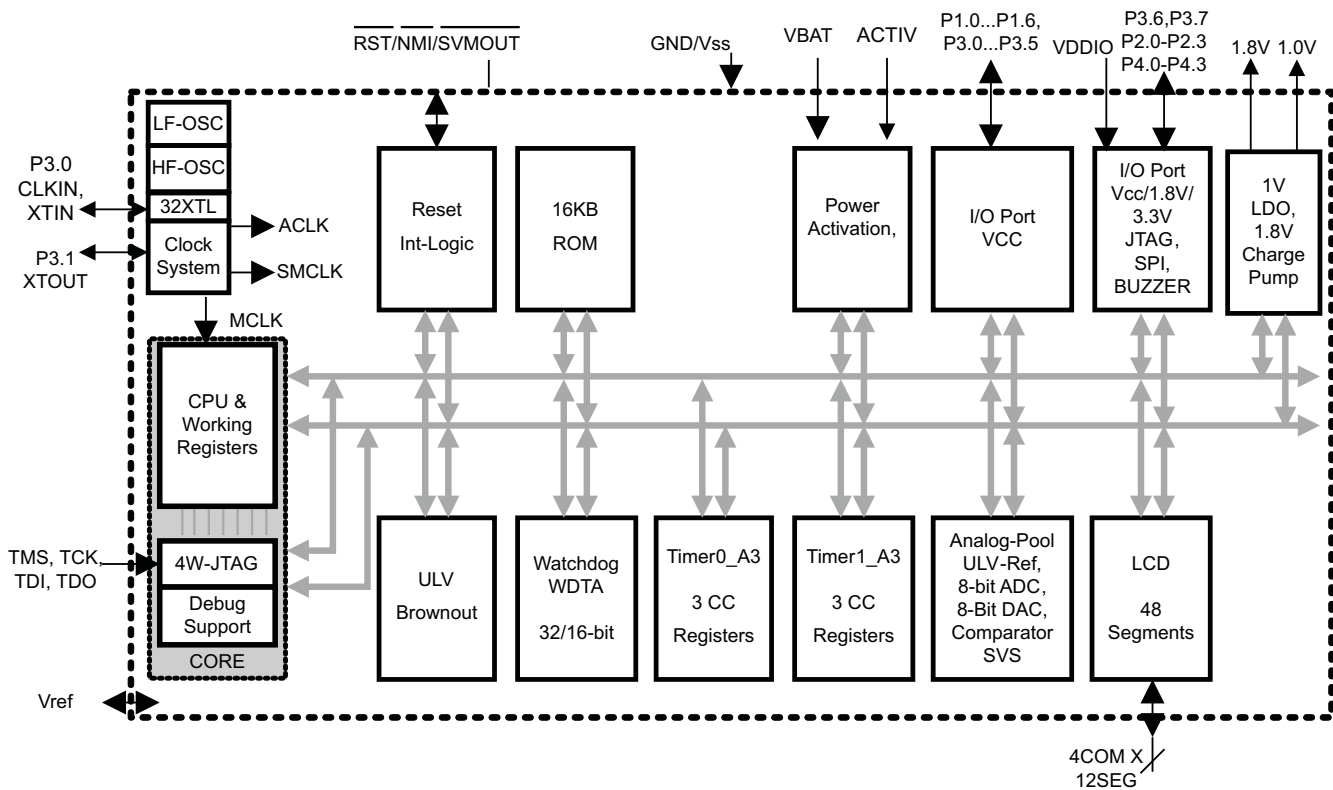
The AFE4110 configuration with two 16-bit timers, integrated 48-segment LCD driver, programmable Analog Pool, supply voltage monitor and internal reference voltage source is particularly well suited for implementation of low cost digital thermometers operating from a single cell SR60 battery. The capability to correct the on chip high frequency oscillator output facilitates the generation and measurement of real time intervals. For many applications, this capability allows system designers to eliminate a clock crystal from the system BOM.

### ORDERING INFORMATION<sup>(1)</sup>

| T <sub>A</sub> | ORDERABLE PART |
|----------------|----------------|
| 0°C to 70°C    | AFE4110B000YS  |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

### FUNCTIONAL BLOCK DIAGRAM, AFE4110



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

|  | VALUE |                | UNIT |
|--|-------|----------------|------|
|  | MIN   | MAX            |      |
| Voltage applied at $V_{DD}$ referenced to $V_{SS}$ ( $V_{AMR}$ ) | -0.3  | 1.8            | V    |
| Voltage applied to any pin (references to $V_{SS}$ )             | -0.3  | $V_{DD} + 0.3$ | V    |
|  | -0.3  | 1.8            | V    |
| Diode current at any device pin <sup>(2)</sup>                   |       | $\pm 2.5$      | mA   |
| Storage temperature range <sup>(3)</sup>                         | -55   | 150            | °C   |
| ESD tolerance HBM  |       | 2000           | V    |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to  $V_{SS}$ .
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## RECOMMENDED OPERATING CONDITIONS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

|                                |   | MIN | TYP | MAX  | UNIT |
|--------------------------------|---|-----|-----|------|------|
| $V_{DD}$                       | Supply voltage during program execution | 1.1 |     | 1.55 | V    |
| $V_{SS}$                       | Supply voltage (GND reference)          |     | 0   |      | V    |
| $T_A$                          | Operating free-air temperature          | 0   |     | 70   | °C   |
| $CV_{DD}$                      | Capacitor on $V_{DD}$                   |     | 470 |      | nF   |
| $f_{SYSTEM}$ <sup>(1)(2)</sup> | $V_{DD} > 1.1$ V                        |     | 1   |      | MHz  |
|                                | $V_{DD} > 1.5$ V                        |     | 4   |      |      |

- (1) The AFE4110 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulsewidth of the specified maximum frequency.
- (2) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.

**Active Mode Supply Current (Into  $V_{CC}$ ) <sup>(1)(2)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           | TEST CONDITIONS  | $V_{DD}$ | $T_A$ | MIN | TYP | MAX | UNIT                     |
|---------------------|--|----------|-------|-----|-----|-----|--------------------------|
| $I_{AM,1MHz}$       | $f_{MCLK} = f_{SMCLK} = 1 \text{ MHz}$ , $f_{ACLK} = 20 \text{ kHz}$ ,<br>Program executes in RAM,<br>CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0             | 1.3 V    | 30°C  | 72  |     |     | $\mu\text{A}$            |
|                     |  | 1.55 V   |       | 86  |     |     |                          |
|                     | $f_{MCLK} = f_{SMCLK} = 1 \text{ MHz}$ , $f_{ACLK} = 20 \text{ kHz}$ ,<br>Program executes in RAM,<br>CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0             | 1.3 V    | 70°C  | 74  |     |     | $\mu\text{A}$            |
|                     |  | 1.55 V   |       | 88  |     |     |                          |
| $I_{AM,125kHz}$     | $f_{MCLK} = f_{SMCLK} = 125 \text{ kHz}$ , $f_{ACLK} = 20 \text{ kHz}$<br>Program executes in RAM<br>CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0              | 1.3 V    | 30°C  | 33  |     |     | $\mu\text{A}$            |
|                     |  | 1.55 V   |       | 37  |     |     |                          |
|                     | $f_{MCLK} = f_{SMCLK} = 125 \text{ kHz}$ , $f_{ACLK} = 20 \text{ kHz}$ ,<br>Program executes in RAM,<br>CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0           | 1.3 V    | 70°C  | 35  |     |     | $\mu\text{A}$            |
|                     |  | 1.55 V   |       | 40  |     |     |                          |
| $I_{AM}/\text{MHz}$ | $f_{MCLK} = f_{SMCLK} : 1 \text{ to } 5 \text{ MHz}$ , $f_{ACLK} = 20 \text{ kHz}$<br>Program executes in RAM, CPUOFF = 0, SCG0 = 0,<br>SCG1 = 0, OSCOFF = 0 | 1.3 V    | 30°C  | 45  |     |     | $\mu\text{A}/\text{MHz}$ |

 (1) All inputs are tied to 0 V or to  $V_{DD}$ . Outputs do not source or sink any current.

(2) Characterized with program executing typical data processing "Type2".

**Low-Power Mode Supply Current (Into  $V_{CC}$ ) <sup>(1)(2)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS  | $V_{DD}$ | $T_A$ | MIN | TYP | MAX | UNIT          |
|------------------|--|----------|-------|-----|-----|-----|---------------|
| $I_{LPM0}$       | $f_{MCLK} = f_{SMCLK} = 1 \text{ MHz}$ , $f_{ACLK} = 20 \text{ kHz}$<br>CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | 1.3 V    | 30°C  | 8.3 | 11  |     | $\mu\text{A}$ |
|                  |  | 1.55 V   |       | 9.5 | 12  |     |               |
|                  |  | 1.3 V    | 70°C  | 11  | 14  |     |               |
|                  |  | 1.55 V   |       | 12  | 17  |     |               |
| $I_{LPM1}$       | $f_{MCLK} = f_{SMCLK} = 1 \text{ MHz}$ , $f_{ACLK} = 20 \text{ kHz}$<br>CPUOFF = 1, SCG0 = 1, SCG1 = 0, OSCOFF = 0 | 1.3 V    | 30°C  | 8.3 | 11  |     | $\mu\text{A}$ |
|                  |  | 1.55 V   |       | 9.5 | 12  |     |               |
|                  |  | 1.3 V    | 70°C  | 11  | 14  |     |               |
|                  |  | 1.55 V   |       | 12  | 17  |     |               |
| $I_{LPM2,1MHz}$  | $f_{MCLK} = f_{SMCLK} = 1\text{MHz}$ , $f_{ACLK} = 1\text{MHz}$<br>CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0      | 1.3 V    | 30°C  | 28  | 32  |     | $\mu\text{A}$ |
|                  |  | 1.55 V   |       | 29  | 33  |     |               |
|                  |  | 1.3 V    | 70°C  | 30  | 35  |     |               |
|                  |  | 1.55 V   |       | 32  | 38  |     |               |
| $I_{LPM2,20kHz}$ | $f_{MCLK} = f_{SMCLK} = f_{ACLK} = 20 \text{ kHz}$<br>CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0                   | 1.3 V    | 30°C  | 8.3 | 12  |     | $\mu\text{A}$ |
|                  |  | 1.55 V   |       | 9.5 | 13  |     |               |
|                  |  | 1.3 V    | 70°C  | 11  | 15  |     |               |
|                  |  | 1.55 V   |       | 12  | 17  |     |               |
| $I_{LPM3}$       | $f_{MCLK} = f_{SMCLK} = f_{ACLK} = 20 \text{ kHz}$<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0                   | 1.3 V    | 30°C  | 8.3 | 11  |     | $\mu\text{A}$ |
|                  |  | 1.55 V   |       | 9.5 | 12  |     |               |
|                  |  | 1.3 V    | 70°C  | 11  | 14  |     |               |
|                  |  | 1.55 V   |       | 12  | 17  |     |               |
| $I_{LPM4}$       | $f_{MCLK} = f_{SMCLK} = f_{ACLK} = 20 \text{ kHz}$<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1                   | 1.3 V    | 30°C  | 6   | 7.9 |     | $\mu\text{A}$ |
|                  |  | 1.55 V   |       | 7.8 | 10  |     |               |
|                  |  | 1.3 V    | 70°C  | 8.6 | 12  |     |               |
|                  |  | 1.55 V   |       | 11  | 16  |     |               |

(1) Current for WDT clocked by ACLK included.

(2) Current for Brownout included.

**Ports P1, P3 (except for P3.6, P3.7),  $\overline{RST}$ ,  $\overline{NMI}$ ,  $\overline{SVMOUT}$** 

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           | CONDITIONS   | MIN                  | TYP | MAX                  | UNIT       |
|---------------------|--|----------------------|-----|----------------------|------------|
| $V_{OH}$            | $V_{DD} = 1.1\text{ V}$ , $I_{OH} = -1\text{ mA}^{(1)}$ for ports P1, P3                                       | $V_{DD}-0.25$        |     |                      | V          |
|                     | $V_{DD} = 1.55\text{ V}$ , $I_{OH} = -1\text{ mA}^{(1)}$ for ports P1, P3                                      | $V_{DD}-0.15$        |     |                      |            |
|                     | $V_{DD} = 1.1\text{ V}$ , $I_{OH} = -300\text{ }\mu\text{A}^{(1)}$ for ports P1, P3                            | $V_{DD}-0.15$        |     |                      |            |
| $V_{OL}$            | $V_{DD} = 1.1\text{ V}$ , $I_{OL} = 2.5\text{ mA}^{(2)}$ for ports P1, P3                                      |                      |     | 0.2                  | V          |
|                     | $V_{DD} = 1.55\text{ V}$ , $I_{OL} = 2.5\text{ mA}^{(2)}$ for ports P1, P3                                     |                      |     | 0.15                 |            |
|                     | $V_{DD} = 1.1\text{ V}$ , $I_{OL} = 300\text{ }\mu\text{A}^{(2)}$ for ports P1, P3                             |                      |     | 0.07                 |            |
| $V_{IL}$            | $V_{DD} = 1.55\text{ V}$   |                      |     | $0.3 \times V_{DD}$  | V          |
|                     | $V_{DD} = 1.1\text{ V}$  |                      |     | $0.25 \times V_{DD}$ | V          |
| $V_{IH}$            | $V_{DD} = 1.55\text{ V}$   | $0.7 \times V_{DD}$  |     |                      | V          |
|                     | $V_{DD} = 1.55\text{ V}$   | $0.75 \times V_{DD}$ |     |                      | V          |
| $V_{HYS}$           | Intrinsic Hysteresis   |                      | 150 |                      | mV         |
| $\Delta t/\Delta v$ | $V_{DD} = 1.1\text{ V}$ , $C_L = 15\text{ pF}$    $R_L = 750\Omega$ to $V_{SS}$ on $V_{OH}$ for ports P1, P3   |                      |     | 75                   | ns/V       |
|                     | $V_{DD} = 1.1\text{ V}$ , $C_L = 15\text{ pF}$    $R_L = 320\Omega$ to $V_{CC}$ on $V_{OL}$ for ports P1, P3   |                      |     | 75                   |            |
|                     | $V_{DD} = 1.55\text{ V}$ , $C_L = 25\text{ pF}$    $R_L = 1600\Omega$ to $V_{SS}$ on $V_{OH}$ for ports P1, P3 |                      |     | 75                   |            |
|                     | $V_{DD} = 1.55\text{ V}$ , $C_L = 25\text{ pF}$    $R_L = 600\Omega$ to $V_{SS}$ on $V_{OL}$ for ports P1, P3  |                      |     | 75                   |            |
| $I_{OH}$            | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$ for ports P1, P3   | -1                   |     |                      | mA         |
| $I_{OL}$            | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$ for ports P1, P3   | 2.5                  |     |                      | mA         |
| $I_{LKG}$           | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$  |                      |     | $\pm 100$            | nA         |
| $t_{INT}$           | P0.x; $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$  |                      | 200 |                      | ns         |
| $R_{PULL}$          | For pullup: $V_{IN} = V_{SS}$ ; For pulldown: $V_{IN} = V_{DD}$ for ports P1, P3                               | 30                   | 35  | 40                   | k $\Omega$ |
| $R_{RST}$           | Pullup on $\overline{RST}$ , $\overline{NMI}$ , $\overline{SVMOUT}$  | 30                   | 35  | 40                   | k $\Omega$ |
| $R_{EXT}$           | External pull up resistor on RST terminal (optional)   | 680                  |     |                      | k $\Omega$ |
| $C_I$               | $V_{IN} = V_{SS}$ or $V_{DD}$  |                      | 7   |                      | pF         |

- (1) The maximum total current  $I_{OH}$ , for all outputs combined should not exceed 5mA to hold the maximum voltage drop specified  
(2) The maximum total current  $I_{OL}$ , for all outputs combined should not exceed 15mA to hold the maximum voltage drop specified

**Ports P2, P4 and Port 3.7, Port 3.6**

1.1V &lt; VDDIO &lt; 3.3V over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER         | CONDITIONS   | MIN                                   | TYP         | MAX                                   | UNIT |
|-------------------|--|---------------------------------------|-------------|---------------------------------------|------|
| V <sub>OH</sub>   | VDDIO = 1.1 V, I <sub>OH</sub> = -1 mA <sup>(1)</sup>  | VDDIO - 0.25                          |             |                                       | V    |
|                   | VDDIO = 3.3 V, I <sub>OH</sub> = -1 mA <sup>(1)</sup>  | VDDIO - 0.15                          |             |                                       |      |
|                   | VDDIO = 1.1 V, I <sub>OH</sub> = -300 μA <sup>(1)</sup>  | VDDIO - 0.15                          |             |                                       |      |
| V <sub>OL</sub>   | VDDIO = 1.1 V, I <sub>OL</sub> = 2.5 mA <sup>(2)</sup>   |                                       |             | 0.2                                   | V    |
|                   | VDDIO = 3.3 V, I <sub>OL</sub> = 2.5 mA <sup>(2)</sup>   |                                       |             | 0.15                                  |      |
|                   | VDDIO = 1.1 V, I <sub>OL</sub> = 300 μA <sup>(2)</sup>   |                                       |             | 0.07                                  |      |
| V <sub>IL</sub>   | VDDIO = 3.3 V  |                                       | 0.3 x VDDIO |                                       | V    |
|                   | VDDIO = 1.1 V  |                                       |             | 0.25 x VDDIO                          | V    |
| V <sub>IH</sub>   | VDDIO = 3.3 V  | 0.7 x VDDIO                           |             |                                       | V    |
|                   | VDDIO = 1.1 V  | 0.75 x VDDIO                          |             |                                       | V    |
| V <sub>IT+</sub>  | VDDIO = 1.1 V – 3.3 V (positive going input threshold)   | V <sub>ILmax</sub> + V <sub>HYS</sub> |             | V <sub>IHmin</sub>                    | V    |
| V <sub>IT-</sub>  | VDDIO = 1.1 V – 3.3 V (negative going input threshold)   | V <sub>ILmax</sub>                    |             | V <sub>IHmin</sub> - V <sub>HYS</sub> | V    |
| V <sub>HYS</sub>  | Intrinsic Hysteresis   |                                       | 150         |                                       | mV   |
| Δt/Δv             | VDDIO = 1.1 V, C <sub>L</sub> = 15 pF    R <sub>L</sub> = 750Ω to V <sub>SS</sub> on V <sub>OH</sub> for ports P1,P2,P3  |                                       |             | 75                                    | ns/V |
|                   | VDDIO = 1.1 V, C <sub>L</sub> = 15 pF    R <sub>L</sub> = 320Ω to V <sub>DD</sub> on V <sub>OL</sub> for ports P1,P2,P3  |                                       |             | 75                                    |      |
|                   | VDDIO = 3.3 V, C <sub>L</sub> = 25 pF    R <sub>L</sub> = 1600Ω to V <sub>SS</sub> on V <sub>OH</sub> for ports P1,P2,P3 |                                       |             | 75                                    |      |
|                   | VDDIO = 3.3 V, C <sub>L</sub> = 25 pF    R <sub>L</sub> = 600Ω to V <sub>SS</sub> on V <sub>OL</sub> for ports P1,P2,P3  |                                       |             | 75                                    |      |
| I <sub>OH</sub>   | VDDIO = 1.1 V – 3.3 V for ports P1,P2,P3   | -1                                    |             |                                       | mA   |
| I <sub>OL</sub>   | VDDIO = 1.1 V – 3.3 V for ports P1,P2,P3   | 2.5                                   |             |                                       | mA   |
| I <sub>LKG</sub>  | VDDIO = 1.1 V – 3.3 V  |                                       |             | ±100                                  | nA   |
| t <sub>INT</sub>  | P0.x; V <sub>DD</sub> = 1.1 V – 3.3 V  |                                       | 200         |                                       | ns   |
| R <sub>PULL</sub> | For pullup: V <sub>IN</sub> = V <sub>SS</sub> ; For pulldown: V <sub>IN</sub> = VDDIO for ports P1,P2,P3                 | 30                                    | 35          | 40                                    | kΩ   |
| R <sub>RST</sub>  | Pullup on RST/NMI/SVMOUT   | 30                                    | 35          | 40                                    | kΩ   |
| C <sub>I</sub>    | V <sub>IN</sub> = V <sub>SS</sub> or VDDIO   |                                       | 7           |                                       | pF   |

 (1) The maximum total current I<sub>OH</sub>, for all outputs combined should not exceed 5mA to hold the maximum voltage drop specified

 (2) The maximum total current I<sub>OL</sub>, for all outputs combined should not exceed 15mA to hold the maximum voltage drop specified

**Ports P3.6, P3.7 (High Current Buzzer)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER         | CONDITIONS   | MIN        | TYP | MAX  | UNIT |
|-------------------|--|------------|-----|------|------|
| V <sub>OH</sub>   | VDDIO = 1.1 V, I <sub>OH</sub> = -10 mA  | VDDIO-0.15 |     |      | V    |
|                   | VDDIO = 3.3 V, I <sub>OH</sub> = -10 mA  | VDDIO-0.15 |     |      |      |
| V <sub>OL</sub>   | VDDIO = 1.1 V, I <sub>OL</sub> = 10 mA   |            |     | 0.2  | V    |
|                   | VDDIO = 3.3 V, I <sub>OL</sub> = 10 mA   |            |     | 0.15 |      |
| Δt/Δv             | VDDIO = 1.1V, C <sub>L</sub> = 15 pF    R <sub>L</sub> = 750Ω to V <sub>SS</sub> on V <sub>OH</sub>  |            |     | 75   | ns/V |
|                   | VDDIO = 1.1 V, C <sub>L</sub> = 15 pF    R <sub>L</sub> = 320Ω to V <sub>DD</sub> on V <sub>OL</sub> |            |     | 75   |      |
|                   | VDDIO = 1.55 V, C <sub>L</sub> = 25 pF    R <sub>L</sub> = 1600Ω to V <sub>SS</sub> on               |            |     | 75   |      |
|                   | VDDIO = 1.55 V, C <sub>L</sub> = 25 pF    R <sub>L</sub> = 600Ω to V <sub>SS</sub> on                |            |     | 75   |      |
| I <sub>OH</sub>   | VDDIO = 1.1 V – 3.3 V  | -10        |     |      | mA   |
| I <sub>OL</sub>   | VDDIO = 1.1 V – 3.3 V  | 10         |     |      | mA   |
| I <sub>LKG</sub>  | VDDIO = 1.1 V – 3.3 V  |            |     | ±100 | nA   |
| t <sub>INT</sub>  | P0.x; V <sub>DD</sub> = 1.1 V – 3.3 V  |            | 200 |      | ns   |
| R <sub>PULL</sub> | Only pulldown implemented: V <sub>IN</sub> = VDDIO   | 30         | 35  | 40   | kΩ   |
| C <sub>I</sub>    | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>DD</sub>   |            | 7   |      | pF   |

## High Frequency – OSCILLATOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                       | CONDITIONS  | MIN | TYP        | MAX | UNIT                  |
|---------------------------------|---|-----|------------|-----|-----------------------|
| $f_{HFOSC}$                     | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$ (untrimmed)   | 4   | 5          | 7   | MHz                   |
| $f_{HFOSC}$                     | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$ (trimmed)   | 4.1 | 4.5        | 4.8 | MHz                   |
| Duty Cycle                      | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$   | 45% | 50%        | 55% |                       |
| $t_{START}$                     | $V_{DDC} = 1.1\text{ V} - 1.55\text{ V}$  |     |            | 20  | $\mu\text{s}$         |
| $\Delta f_{DCO}/\Delta T$       | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$ ; $f_{DCO} = 4\text{ MHz}$                              |     | $\pm 0.07$ |     | $\%/^{\circ}\text{C}$ |
| $\Delta f_{DCO}/V_{DD}$         | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$ ; $f_{DCO} = 4\text{ MHz}$                              |     | $\pm 1$    |     | $\%/V$                |
| $\Delta f_{DCO}/\text{CALSTEP}$ | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$ ; $f_{DCO} = 4\text{ MHz}$ ; $\pm 64$ calibration steps | 0.1 | 1          | 4   | $\%/Step$             |
| $I_{OP}$                        | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$ ; $f_{DCO} = 4\text{ MHz}$                              |     | 25         |     | $\mu\text{A}$         |
| $I_{OP}$                        | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$ ; $f_{DCO} = 1\text{ MHz}$                              |     | 22         |     | $\mu\text{A}$         |

## Low Frequency – OSCILLATOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER   | CONDITIONS   | MIN | TYP | MAX | UNIT          |
|-------------|--|-----|-----|-----|---------------|
| $f_{LFO}$   | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$                              | 6   | 20  | 45  | kHz           |
| Duty Cycle  | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$                              | 45% | 50% | 55% |               |
| $t_{START}$ | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$                              |     |     | 500 | $\mu\text{s}$ |
| $I_{OP}$    | $V_{DDC} = 1.1\text{ V} - 1.55\text{ V}$ ; $f_{LFO} = 20\text{ kHz}$ |     | 600 |     | nA            |

## 32 kHz Crystal – OSCILLATOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER   | CONDITIONS                               | MIN | TYP | MAX | UNIT          |
|-------------|--|-----|-----|-----|---------------|
| $f_{LFO}$   | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$  |     | 32  |     | kHz           |
| Duty Cycle  | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$  | 45% | 50% | 55% |               |
| $t_{START}$ | $V_{DDC} = 1.1\text{ V} - 1.55\text{ V}$ |     | 200 |     | mS            |
| $I_{OP}$    | $V_{DD} = 1.1\text{ V} - 1.55\text{ V}$  |     | 2   |     | $\mu\text{A}$ |

## CP\_1P8 Specifications

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                    | TEST CONDITIONS           | MIN  | TYP                  | MAX  | UNIT |
|------------------------------|---------------------------|------|----------------------|------|------|
| Start-up time                |                           |      | 5mS                  |      |      |
| Supply voltage battery input |                           | 1.1  |                      | 1.55 | V    |
| Output voltage, $V_O$        |                           |      | $1.8 \times V_{BAT}$ |      |      |
| No load voltage              | $V_{BAT} = 1.55\text{ V}$ |      |                      | 3    | V    |
| Max load voltage             | $V_{BAT} = 1.2\text{ V}$  | 1.85 |                      |      | V    |
| Max load                     | CP18 = 10 nF              | 0.01 |                      | 3    | mA   |
| Charge pump efficiency       |                           |      | 70%                  |      |      |
| Clocking frequency           |                           |      | 4                    |      | MHz  |

## Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER               | CONDITIONS  | MIN  | TYP | MAX                 | UNIT |
|-------------------------|---|------|-----|---------------------|------|
| V <sub>BOR(Start)</sub> |   | 490  |     |                     | mV   |
| V <sub>(BOR_IT+)</sub>  | V <sub>DD</sub> rising; dV <sub>DD</sub> / dt < 3V/s                          | 1095 |     | 1150                | mV   |
| V <sub>(BOR_IT-)</sub>  | V <sub>DD</sub> falling; dV <sub>DD</sub> / dt < 3V/s                         | 860  |     | 900                 | mV   |
| V <sub>hys(BOR)</sub>   |   |      | 200 |                     | mV   |
| V <sub>MARGIN</sub>     | V <sub>MARGIN</sub> = V <sub>(BOR-IT-)</sub> - V <sub>CRIT</sub> ; T = 0-70°C | 40   |     |                     | mV   |
| t <sub>dBOR</sub>       |   |      |     | 3000 <sup>(1)</sup> | µs   |
| I <sub>OP</sub>         | V <sub>DD</sub> = 1.1 V – 1.55 V  |      | 500 |                     | nA   |

(1) Depends on the voltage ramp in the system (actually a maximum typical value).

## A-POOL, External Reference Source

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER        | CONDITIONS   | MIN | TYP | MAX             | UNIT |
|------------------|--|-----|-----|-----------------|------|
| V <sub>REF</sub> | V <sub>DD</sub> = 1.1 V – 1.55 V for ADC / DAC operation   | 100 |     | 475             | mV   |
|                  | V <sub>DD</sub> = 1.1 V – 1.55 V ADC / DAC not operational | 0   |     | V <sub>DD</sub> | V    |
| I <sub>REF</sub> | V <sub>DD</sub> = 1.1 V – 1.55 V                           |     | 3   |                 | µA   |
| C <sub>REF</sub> | REFON = 0  | 20  |     | 50              | pF   |

## A-POOL, Built-In Reference Source

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           | CONDITIONS  | MIN | TYP     | MAX | UNIT   |
|---------------------|---|-----|---------|-----|--------|
| V <sub>REF</sub>    | V <sub>DD</sub> = 1.1 V – 1.55 V (±1.5%; overall 3%)                                  |     | 256 ±3% |     | mV     |
| I <sub>REF</sub>    | V <sub>DD</sub> = 1.1 V – 1.55 V  |     | 10      |     | µA     |
| C <sub>REF</sub>    | REFON = 1   | 20  |         | 50  | pF     |
| T <sub>REF</sub>    | V <sub>DD</sub> = 1.1 V – 1.55 V ( ΔV/ΔT × V <sub>REF</sub> referenced to 25°C)       |     | ±250    |     | ppm/°C |
| t <sub>settle</sub> | V <sub>DD</sub> = 1.1 V – 1.55 V; REFON = 1; C <sub>REF</sub> = C <sub>REF(max)</sub> |     | 900     |     | µs     |
| I <sub>OP</sub>     | V <sub>DD</sub> = 1.1 V – 1.55 V; REFON = 1; C <sub>REF</sub> = C <sub>REF(max)</sub> | 50  |         |     | µA     |

## A-POOL, Temperature Sensor

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                          | CONDITIONS   | MIN | TYP | MAX | UNIT  |
|------------------------------------|--|-----|-----|-----|-------|
| I <sub>SENSOR</sub>                | V <sub>CC</sub> = 1.1 V – 1.55 V                                     |     | 2   |     | µA    |
| TC <sub>SENSOR</sub>               | V <sub>CC</sub> = 1.1 V – 1.55 V; 0-70°C ( ΔV/ΔT referenced to 30°C) |     | 464 |     | µV/°C |
| V <sub>OFFSET25</sub>              | V <sub>CC</sub> = 1.1 V – 1.55 V at T <sub>A</sub> = 30°C            |     | 179 |     | mV    |
| t <sub>SETTLE</sub>                | V <sub>CC</sub> = 1.1 V – 1.55 V (before start of conversion)        |     |     | 15  | µs    |
| V <sub>SENSOR</sub> <sup>(1)</sup> | V <sub>CC</sub> = 1.1 V – 1.55 V; 0-70°C                             |     | 179 |     | mV    |

(1) The following formula can be used to calculate the temperature sensor output voltage

$$V_{\text{SENSOR}} = V_{\text{OFFSET25}} + TC_{\text{SENSOR}} \times (T_A - 30^\circ\text{C})$$



## A-POOL, Input Voltage Dividers

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER        | CONDITIONS  | MIN   | TYP | MAX | UNIT       |
|------------------|---|-------|-----|-----|------------|
| $\Delta R_x/R_x$ | any Rx in dividers  | ±1.5% |     |     |            |
|                  | any Rx across switches and internal supply voltage divider (by 4, by 8)         | ±2%   |     |     |            |
| $R_{IN}$         | on A0/A1 ; $V_{A0}/V_{A1} = 0.5$ V; ADIV0/ADIV1 = 1 (500 mV range)              | 120   | 200 | 300 | k $\Omega$ |
|                  | on A2/A3 ; $V_{A2}/V_{A3} = 0.5$ V; ADIV2/ADIV4 = 1 (1 V range)                 | 80    | 133 | 190 |            |
|                  | on A2/A3 ; $V_{A2}/V_{A3} = 0.5$ V; ADIV2 + ADIV3/ADIV4 + ADIV5 = 1 (2 V range) | 70    | 114 | 150 |            |
| $\Delta I_{VDD}$ | ADIV7 = 1 (supply voltage divider on)   | 2     |     |     | $\mu$ A    |

## A-POOL, DAC-8

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER    | CONDITIONS   | MIN | TYP | MAX | UNIT    |     |
|--------------|--|-----|-----|-----|---------|-----|
| $V_{REFEXT}$ | $V_{DD} = 1.1$ V – 1.55 V  | 256 |     |     | mV      |     |
| $t_{SETTLE}$ | On $\pm 1$ LSB steps (6 $\tau$ ); $V_{DD} = 1.1$ V – 1.55 V; $V_{REFEXT}(typ)$ ; $C_{VREF}(min)$                       | 2   |     |     | $\mu$ s |     |
|              | Between all codes >20 on $A_{OUT}$ (6 $\tau$ ); $V_{DD} = 1.1$ V – 1.55 V; $V_{REFEXT}(typ)$ ; $C_{VREF}(min)$         | 14  |     |     | $\mu$ s |     |
| $E_I$        | $V_{DD} = 1.1$ V – 1.55 V; $V_{REFEXT}(typ)$ ; $C_{VREF}(min)$ ; (add $\pm 7$ mV for $V_{OUT}$ offset <sup>(1)</sup> ) |     |     |     | ±3      | LSB |
| $E_D$        |  |     |     |     | ±1      | LSB |

(1) This offset can be compensated using proper software.

## A-POOL, Comparator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | CONDITIONS                | MIN | TYP | MAX | UNIT |         |
|-----------|---------------------------|-----|-----|-----|------|---------|
| $V_{IN}$  | $V_{DD} = 1.1$ V – 1.55 V | 0   |     | 275 | mV   |         |
| $t_{pd}$  | Overdrive = 20 mV         |     |     |     | 0.5  | $\mu$ s |
|           | Overdrive = 5 mV          |     |     |     | 0.5  |         |
|           | Overdrive = 1 mV          |     |     |     | 1    |         |

## A-POOL, AOUT Pin

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER    | CONDITIONS   | MIN | TYP | MAX | UNIT    |         |
|--------------|--|-----|-----|-----|---------|---------|
| $ I_{LOAD} $ | $V_{DD} = 1.1$ V – 1.55 V; $C_{LOAD} = 25$ pF; $V_{OUT} > 50$ mV                               | 5   |     |     | $\mu$ A |         |
| $ I_{LOAD} $ | $V_{DD} = 1.1$ V – 1.55 V; $C_{LOAD} = 25$ pF; $V_{OUT} > 20$ mV                               | 2   |     |     | $\mu$ A |         |
| $t_{SETTLE}$ | $V_{DD} = 1.1$ V – 1.55 V; $C_{LOAD} = 25$ pF; $\pm 1\%$ (6 $\tau$ ) (for $A_{OUT}$ 20-256 mV) |     |     |     | 4       | $\mu$ s |

## A-POOL, ADC-8 Counter

over operating free-air temperature range (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS                                  | MIN | TYP | MAX | UNIT |         |
|------------|--|-----|-----|-----|------|---------|
| $f_{CNT}$  | $V_{DD} = 1.1$ V – 1.55 V                        |     |     |     | 1    | MHz     |
| $t_{CONV}$ | Full conversion (all codes) at $f_{CNT} = 1$ MHz | 256 |     |     |      | $\mu$ s |

## RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

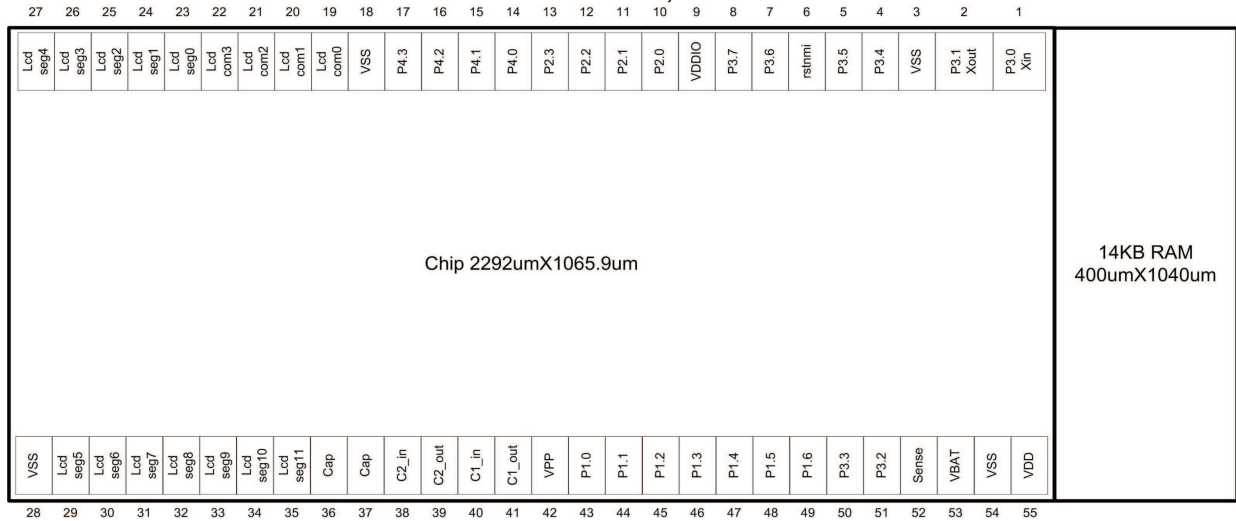
| PARAMETER | CONDITIONS                                      | MIN | TYP | MAX | UNIT |
|-----------|---|-----|-----|-----|------|
| $V_{OP}$  | Operating temperature 0-70°C, $f_{CPU} = 1$ MHz | 1.1 |     |     | V    |
| $V_{RET}$ | Operating temperature 0-70°C (tracks BOL level) | 700 |     |     | mV   |

# AFE4110

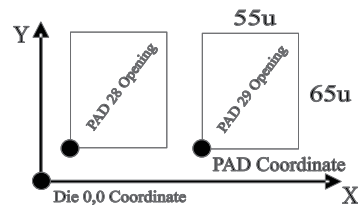
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## PIN DESIGNATION, AFE4110



| PAD# | PAD X [ $\mu$ ] | PAD Y [ $\mu$ ] | PAD# | PAD X [ $\mu$ ] | PAD Y [ $\mu$ ] |
|------|-----------------|-----------------|------|-----------------|-----------------|
| 1    | 2108.3          | 987.3           | 28   | 96.0            | 23.6            |
| 2    | 1994.6          | 987.3           | 29   | 171.0           | 23.6            |
| 3    | 1908.6          | 987.3           | 30   | 246.0           | 23.6            |
| 4    | 1824.2          | 987.3           | 31   | 321.0           | 23.6            |
| 5    | 1749.2          | 987.3           | 32   | 396.0           | 23.6            |
| 6    | 1674.2          | 987.3           | 33   | 471.0           | 23.6            |
| 7    | 1599.2          | 987.3           | 34   | 546.0           | 23.6            |
| 8    | 1521.8          | 987.3           | 35   | 621.0           | 23.6            |
| 9    | 1446.8          | 987.3           | 36   | 696.0           | 23.6            |
| 10   | 1371.8          | 987.3           | 37   | 771.0           | 23.6            |
| 11   | 1296.8          | 987.3           | 38   | 846.0           | 23.6            |
| 12   | 1221.8          | 987.3           | 39   | 921.0           | 23.6            |
| 13   | 1146.8          | 987.3           | 40   | 996.0           | 23.6            |
| 14   | 1071.8          | 987.3           | 41   | 1071.0          | 23.6            |
| 15   | 996.8           | 987.3           | 42   | 1146.0          | 23.6            |
| 16   | 921.8           | 987.3           | 43   | 1221.0          | 23.6            |
| 17   | 846.8           | 987.3           | 44   | 1296.0          | 23.6            |
| 18   | 771.8           | 987.3           | 45   | 1371.0          | 23.6            |
| 19   | 696.8           | 987.3           | 46   | 1446.0          | 23.6            |
| 20   | 621.8           | 987.3           | 47   | 1521.0          | 23.6            |
| 21   | 546.8           | 987.3           | 48   | 1596.0          | 23.6            |
| 22   | 471.8           | 987.3           | 49   | 1671.0          | 23.6            |
| 23   | 396.8           | 987.3           | 50   | 1746.0          | 23.6            |
| 24   | 321.8           | 987.3           | 51   | 1821.0          | 23.6            |
| 25   | 246.8           | 987.3           | 52   | 1896.0          | 23.6            |
| 26   | 171.8           | 987.3           | 53   | 1971.0          | 23.6            |
| 27   | 96.8            | 987.3           | 54   | 2046.0          | 23.6            |
|      |                 |                 | 55   | 2121.0          | 23.6            |



**PIN FUNCTIONS**

| PIN   |     | I/O <sup>(1)</sup> | DESCRIPTION  |
|---|-----|--------------------|--|
| NAME  | NO. |                    |  |
| P3.0/XTI/EXCLK/TA1.CCI1A1   | 1   | I/O                | General-purpose digital I/O<br>32 kHz Crystal Input<br>External Clock Input<br>Timer1_A3 CCR1A1 capture: CCI1A1 input, compare   |
| P3.1/XTO/TCLK/TA1.CCI1A2/<br>ACTSEN/CMP   | 2   | I/O                | General-purpose digital I/O<br>32 kHz Crystal Out<br>Test Clock Input<br>Timer1_A3 CCR1A2 capture: CCI1A2 input, compare<br>Activation Sense Output<br>Comparator Out  |
| VSS/GND   | 3   | Power              | Analog and Digital Power Supply Ground Reference   |
| P3.4/TA0.1/TA1.1/TA1.0/TA1.CCI2A2   | 4   | I/O                | General-purpose digital I/O<br>Timer0_A3 Out1 output<br>Timer1_A3 Out1 output<br>Timer1_A3 Out0 output<br>Timer1_A3 CCR2A2 capture: CCI2A2 input, compare  |
| P3.5/TA0.1/TA1.1/TA1.0/TA1.CCI2A3   | 5   | I/O                | General-purpose digital I/O<br>Timer0_A3 Out1 output<br>Timer1_A3 Out1 output<br>Timer1_A3 Out0 output<br>Timer1_A3 CCR2A3 capture: CCI2A3 input, compare  |
| RST/NMI/SVMOUT  | 6   | I/O                | Reset input active low<br>Non-maskable interrupt input<br>SVM Output   |
| P3.6/<br>TA0.0/TA0.1/TA0.2/TA0.0N/TA0.1N/TA0.2N/<br>TA1.CCI1A3/<br>TA1.1/BOR/ACTSEN/LFOSC/CP18OK        | 7   | I/O                | 10mA General-purpose digital I/O<br>Timer0_A3 Out0 output<br>Timer0_A3 Out1 output<br>Timer0_A3 Out2 output<br>Timer0_A3 Out0# output<br>Timer0_A3 Out1# output<br>Timer0_A3 Out2# output<br>Timer1_A3 CCR1A3 capture: CCI1A3 input, compare<br>Timer1_A3 Out1 output<br>BOR Out<br>Activation Sense Output<br>LFOSC Out<br>CP 1.8V OK Out                   |
| P3.7/<br>TA0.0/TA0.1/TA0.2/TA0.0N/TA0.1N/TA0.2N/<br>TA1.CCI2A1/HFOSC/LCDCPCLK/<br>LCDFCLK/ 1KCLK/LCDCMP | 8   | I/O                | 10mA General-purpose digital I/O<br>Timer0_A3 Out0 output<br>Timer0_A3 Out1 output<br>Timer0_A3 Out2 output<br>Timer0_A3 Out0# output<br>Timer0_A3 Out1# output<br>Timer0_A3 Out2# output<br>Timer1_A3 CCR2A1 capture: CCI2A1 input, compare<br>LCD Charge Pump Clock Out<br>LCD Frame Clock Out<br>1 kHz Activation Clock Out<br>LCD Voltage Comparator Out |
| VDDIO   | 9   | Power              | Port2.x, Port4.x, Port3.6 and Port3.7 Positive Power supply 1.1V-3.3V  |
| TCK/P2.0/TA1.2/TA1.1/CxOUT  | 10  | I/O                | JTAG Test clock<br>General-purpose digital I/O<br>Timer1_A3 Out2 output<br>Timer1_A3 Out1 output<br>CxOUT digital out from A-Pool  |

(1) I = input, O = output, N/A = not available on this package offering.

**PIN FUNCTIONS (continued)**

| PIN                                |     | I/O <sup>(1)</sup> | DESCRIPTION  |
|------------------------------------|-----|--------------------|--|
| NAME                               | NO. |                    |  |
| TMS/P2.1/ EXT_CLK/TA0.1/TA0.2      | 11  | I/O                | JTAG Test mode select<br>General-purpose digital I/O<br>Timer0_A3 Out2 output<br>Timer0_A3 Out1 output<br>XTAL_CLK or EXT_CLK monitor out      |
| TDI/P2.2/HF_CLK/CxOUT/TA1.0/       | 12  | I/O                | JTAG Test data input<br>General-purpose digital I/O<br>Timer1_A3 Out0 output<br>CxOUT digital out from A-Pool<br>HF_CLK out                    |
| TDO/P2.3/LF_CLK/TA0.2              | 13  | I/O                | JTAG Test data output<br>General-purpose digital I/O<br>Timer0_A3 Out2 output<br>LF_CLK Out  |
| P4.0/TA0.2/TA1.2/ACLK/ATEST/SPI_CS | 14  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out2 output<br>Timer1_A3 Out2 output<br>ACLK output<br>Analog Test Multiplexer Out<br>SPI Chip Select |
| P4.1/TA0.2/TA1.2/SMCLK/SPI_MOSI    | 15  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out2 output<br>Timer1_A3 Out2 output<br>SMCLK output<br>SPI Serial IN                                 |
| P4.2/ TA0.2/TA1.2/MCLK/SPI_CLK     | 16  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out2 output<br>Timer1_A3 Out2 output<br>MCLK output<br>SPI Clock Out                                  |
| P4.3/ TA0.2/TA1.2/1KOSC//SPI_MISO  | 17  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out2 output<br>Timer1_A3 Out2 output<br>1 kHz Activation Oscillator Out<br>SPI Serial Out             |
| GNDIO                              | 18  | Power              | PX.X GND   |
| LCD_ECOM.0                         | 19  | Analog             | LCD_E Common-0 , 0V – 3.4V   |
| LCD_ECOM.1                         | 20  | Analog             | LCD_E Common-1 , 0V – 3.4V   |
| LCD_ECOM.2                         | 21  | Analog             | LCD_E Common-2 , 0V – 3.4V   |
| LCD_ECOM.3                         | 22  | Analog             | LCD_E Common-3 , 0V – 3.4V   |
| LCD_ESEG.0                         | 23  | Analog             | LCD_E Segment-0 , 0V – 3.4V  |
| LCD_ESEG.1                         | 24  | Analog             | LCD_E Segment-1 , 0V – 3.4V  |
| LCD_ESEG.2                         | 25  | Analog             | LCD_E Segment-2 , 0V – 3.4V  |
| LCD_ESEG.3                         | 26  | Analog             | LCD_E Segment-3 , 0V – 3.4V  |
| LCD_ESEG.4                         | 27  | Analog             | LCD_E Segment-4 , 0V – 3.4V  |
| VSS/GND                            | 28  | Power              | Analog and Digital Power Supply Ground Reference   |
| LCD_ESEG.5                         | 29  | Analog             | LCD_E Segment-5 , 0V – 3.4V  |
| LCD_ESEG.6                         | 30  | Analog             | LCD_E Segment-6 , 0V – 3.4V  |
| LCD_ESEG.7                         | 31  | Analog             | LCD_E Segment-7 , 0V – 3.4V  |
| LCD_ESEG.8                         | 32  | Analog             | LCD_E Segment-8 , 0V – 3.4V  |
| LCD_ESEG.9                         | 33  | Analog             | LCD_E Segment-9 , 0V – 3.4V  |
| LCD_ESEG.10                        | 34  | Analog             | LCD_E Segment-10 , 0V – 3.4V   |
| LCD_ESEG.11                        | 35  | Analog             | LCD_E Segment-11 , 0V – 3.4V   |

**PIN FUNCTIONS (continued)**

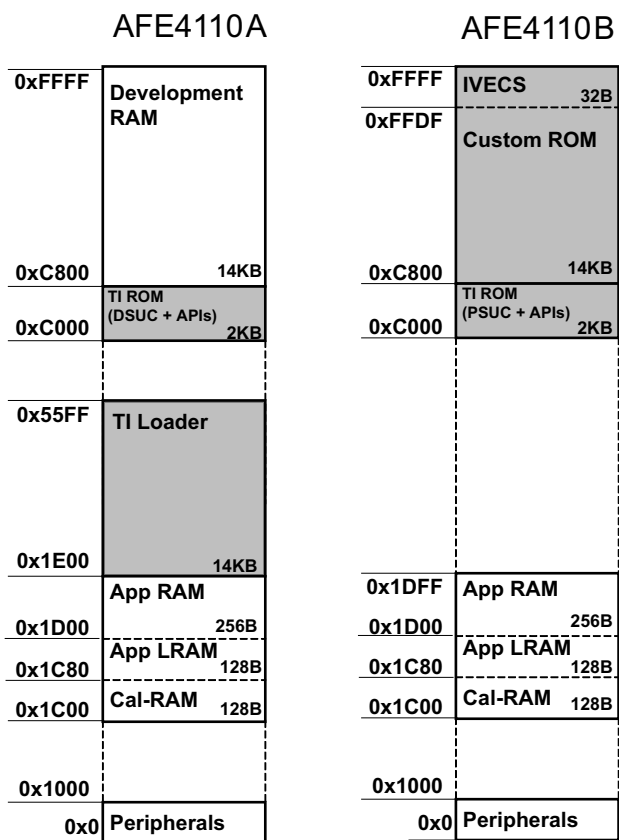
| PIN  |     | I/O <sup>(1)</sup> | DESCRIPTION   |
|--|-----|--------------------|---|
| NAME   | NO. |                    |   |
| LCD_EHVCAP   | 36  | Analog             | LCD_E HV Charge Pump Ext Capacitor to GND, 3.4V   |
| CP18CAP  | 37  | Analog             | Minimum 1.8V Charge pump Ext capacitor C to VSS   |
| CP1P8_C2_IN  | 38  | Analog             | 1.8V Charge pump Ext capacitor B for 2mA drive  |
| CP1P8_C2_OUT   | 39  | Analog             | 1.8V Charge pump Ext capacitor B for 2mA drive  |
| CP1P8_C1_IN  | 40  | Analog             | 1.8V Charge pump Ext capacitor A for 2mA drive  |
| CP1P8_C1_OUT   | 41  | Analog             | 1.8V Charge pump Ext capacitor A for 2mA drive  |
| VPP  | 42  | Power              | Factory programming voltage. VPP must be tied to VDD in normal use mode.  |
| P1.0/TA0.2/TA0.1/TA1.2/LDO1/TA0.CCI1B0/<br>TA0.CCI2B0/A2   | 43  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out2 output<br>Timer0_A3 Out1 output<br>Timer1_A3 Out2 output<br>LDO 1V Out<br>Timer0_A3 CCR1B0 capture: CCI1B0 input, compare<br>Timer0_A3 CCR2B0 capture: CCI2B0 input, compare<br>Analog input A2 – A-Pool          |
| P1.1/TA0.2/TA0.1/TA1.2/LDO1/TA0.CCI1A1/<br>TA0.CCI2A1/A1   | 44  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out2 output<br>Timer0_A3 Out1 output<br>Timer1_A3 Out2 output<br>LDO 1V Out<br>Timer0_A3 CCR1A1 capture: CCI1A1 input, compare<br>Timer0_A3 CCR2A1 capture: CCI2A1 input, compare<br>Analog input A1 – A-Pool          |
| P1.2/TA0.2/TA0.1/TA1.2/AOUT/<br>TA0.CCI1A2/TA0.CCI2A2/A3   | 45  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out2 output<br>Timer0_A3 Out1 output<br>Timer1_A3 Out2 output<br>Analog Out - A-Pool<br>Timer0_A3 CCR1A2 capture: CCI1A2 input, compare<br>Timer0_A3 CCR2A2 capture: CCI2A2 input, compare<br>Analog input A3 – A-Pool |
| P1.3/TA0.2/TA0.1/TA1.2/REFOUT/<br>TA0.CCI1A3/TA0.CCI2A3/A3 | 46  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out2 output<br>Timer0_A3 Out1 output<br>Timer1_A3 Out2 output<br>Vref Out – A-Pool<br>Timer0_A3 CCR1A3 capture: CCI1A3 input, compare<br>Timer0_A3 CCR2A3 capture: CCI2A3 input, compare<br>Analog input A3 – A-Pool   |
| P1.4/TA0.2/TA0.1/TA1.2/LDO1/<br>TA0.CCI1B1/TA0.CCI2B1/A0   | 47  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out2 output<br>Timer0_A3 Out1 output<br>Timer1_A3 Out2 output<br>LDO 1V Out<br>Timer0_A3 CCR1B1 capture: CCI1B1 input, compare<br>Timer0_A3 CCR2B1 capture: CCI2B1 input, compare<br>Analog input A0 – A-Pool          |
| P1.5/TA0.2/TA0.1/TA1.2/LDO1/TA0.CCI1B2/<br>TA0.CCI2B2      | 48  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out2 output<br>Timer0_A3 Out1 output<br>Timer1_A3 Out2 output<br>Timer0_A3 CCR1B2 capture: CCI1B2 input, compare<br>Timer0_A3 CCR2B2 capture: CCI2B2 input, compare  |

**PIN FUNCTIONS (continued)**

| PIN  |     | I/O <sup>(1)</sup> | DESCRIPTION  |
|--|-----|--------------------|--|
| NAME   | NO. |                    |  |
| P1.6/TA0.2/TA0.1/TA1.2/TA1.CCI1B0/<br>TA1.CCI2B0 | 49  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out2 output<br>Timer0_A3 Out1 output<br>Timer1_A3 Out2 output<br>Timer1_A3 CCR1B0 capture: CCI1B0 input, compare<br>Timer1_A3 CCR2B0 capture: CCI2B0 input, compare |
| P3.3/ TA0.1/TA1.1/TA1.0/A0/LDO1                  | 50  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out1 output<br>Timer1_A3 Out1 output<br>Timer1_A3 Out0 output<br>LDO 1V Out<br>Analog input A0 – A-Pool   |
| P3.2/ TA0.1/TA1.1/TA1.0                          | 51  | I/O                | General-purpose digital I/O<br>Timer0_A3 Out1 output<br>Timer1_A3 Out1 output<br>Timer1_A3 Out0 output   |
| ACTIVE   | 52  | I                  | Sleep Mode (LPM5) activation pin   |
| VBAT   | 53  | Power              | Battery Power, Switched from VDD   |
| VSS/GND  | 54  | Power              | Analog and Digital Power Supply Ground Reference   |
| VDD  | 55  | Power              | Analog and Digital Power Supply  |

## Memory Organization

- AFE4110 manufactured in 2 memory configurations
- AFE4110A – Application Development Device
  - 14KB Development RAM
  - 512B Application RAM
  - 2KB Development Start Up Code ROM
  - 14KB Boot Loader ROM
- AFE4110B – Custom Masked ROM Device
  - 512B Application RAM
  - 2KB Production Start Up Code ROM
  - 14KB Custom Masked ROM



## SHORT-FORM DESCRIPTION

### CPU

The AFE4110 is based on an MSP430 CPU core with a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

## INSTRUCTION SET

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. [Table 1](#) shows examples of the three types of instruction formats; the address modes are listed in [Table 2](#).

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC;R0     |
| Stack Pointer            | SP;R1     |
| Status Register          | SR;CG1;R2 |
| Constant Generator       | CG2;R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

**Table 1. Instruction Word Formats**

|                                   |                 |   |
|-----------------------------------|-----------------|---|
| Dual operands, source-destination | e.g. ADD R4, R5 | $R4 + R5 \rightarrow R5$                  |
| Single operands, destination only | e.g. CALL R8    | $PC \rightarrow (TOS), R8 \rightarrow PC$ |
| Relative jump, un/conditional     |                 | Jump-on-equal bit = 0                     |

**Table 2. Address Mode Descriptions**

| ADDRESS MODE           | S <sup>(1)</sup> | D <sup>(2)</sup> | SYNTAX               | EXAMPLE            | OPERATION   |
|------------------------|------------------|------------------|----------------------|--------------------|---|
| Register               | •                | •                | MOV Rs,Rd            | MOV R10, R11       | $R10 \rightarrow R11$                                 |
| Indexed                | •                | •                | MOV X(Rn), Y(Rm)     | MOV 2(R5), 6(R6)   | $M(2+R5) \rightarrow M(6+R6)$                         |
| Symbolic (PC relative) | •                | •                | MOV EDE, TONI        |                    | $M(EDE) \rightarrow M(TONI)$                          |
| Absolute               | •                | •                | MOV & MEM, and TCDAT |                    | $M(MEM) \rightarrow M(TCDAT)$                         |
| Indirect               | •                |                  | MOV at Rn, Y(Rm)     | MOV at R10,Tab(R6) | $M(R10) \rightarrow M(Tab+R6)$                        |
| Indirect autoincrement | •                |                  | MOV at Rn+,Rm        | MOV at R10+, R11   | $M(R10) \rightarrow R11$<br>$R10 + 2 \rightarrow R10$ |
| Immediate              | •                |                  | MOV at 45,TONI       | MOV #45, TONI      | $\#45 \rightarrow M(TONI)$                            |

(1) S = source

(2) D = destination



## Operation Modes

The AFE4110 has one active mode and six software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled
  - ACLK and SMCLK remain active for all sources
  - MCLK is disabled
- Low-power mode 1 (LPM1);
  - CPU is disabled
  - ACLK and SMCLK remain active (for LF-Osc and CLKIN as source; HF-Osc is mapped to LF-Osc as source)
  - MCLK is disabled
- Low-power mode 2 (LPM2);
  - CPU is disabled
  - MCLK is disabled
  - SMCLK is disabled
  - ACLK remains active for all sources
- Low-power mode 3 (LPM3);
  - CPU is disabled
  - MCLK is disabled
  - SMCLK is disabled
  - ACLK remains active (for LF-Osc and CLKIN as source; HF-Osc is mapped to LF-Osc as source)
- Low-power mode 4 (LPM4);
  - CPU is disabled
  - ACLK is disabled
  - MCLK is disabled
  - Oscillators are stopped (exclude Activation Block 1kHz local oscillator)
- Low-power mode 5 (LPM5);
  - CPU core and peripherals are powered off (Application and Calibration RAM contents are not retained.)
  - Activation Block, 1kHz local oscillator, and 8 bytes RAM remain active

## Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 3. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE   | INTERRUPT FLAG  | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY    |
|--|---|------------------|--------------|-------------|
| <b>System Reset</b><br>Power-Up<br>External Reset<br>Watchdog      | WDTIFG <sup>(1)</sup>                                       | Reset            | 0x0FFFE      | 14, highest |
| <b>System NMI</b><br>Vacant memory access                          | SVMIFG, VMAIFG <sup>(1)</sup>                               | (Non)maskable    | 0x0FFFC      | 13          |
| <b>User NMI</b><br>NMI   | NMIIFG <sup>(1) (2)</sup>                                   | (Non)maskable    | 0x0FFFA      | 12          |
| Timer1_A3  | TA1CCR0 CCIFG <sup>(3)</sup>                                | Maskable         | 0x0FFF8      | 11          |
| Timer1_A3  | TA1CCR1 CCIFG<br>TA1CCR2 CCIFG<br>TA1IFG <sup>(1) (3)</sup> | Maskable         | 0x0FFF6      | 10          |
| Watchdog Timer_A Interval Timer Mode                               | WDTIFG  | Maskable         | 0x0FFF4      | 9           |
| A-Pool   | CxIFG   | Maskable         | 0x0FFF2      | 8           |
| I/O Port P1  | P1IFG.0 to P1IFG.6 <sup>(1) (3)</sup>                       | Maskable         | 0x0FFF0      | 7           |
| Timer0_A3  | TA0CCR0 CCIFG <sup>(3)</sup>                                | Maskable         | 0x0FFEE      | 6           |
| Timer0_A3  | TA0CCR1 CCIFG<br>TA0CCR2 CCIFG<br>TA0IFG <sup>(1) (3)</sup> | Maskable         | 0x0FFEC      | 5           |
| I/O Port P2  | P2IFG.0 to P2IFG.3 <sup>(1) (3)</sup>                       | Maskable         | 0x0FFE8      | 4           |
| I/O Port P3  | P3IFG.0 to P3IFG.7 <sup>(1)(3)</sup>                        | Maskable         | 0x0FFE8      | 3           |
| I/O Port P4  | P4IFG.0 to P4IFG.3 <sup>(1) (3)</sup>                       | Maskable         | 0x0FFE6      | 2           |
| LCD Controller   | LCDFRMIFG,<br>LCDBLKOFFIFG,<br>LCDBLKONIFG,<br>LCDNOCAPIFG  | Maskable         | 0x0FFE4      | 1           |
| The Following Interrupts are multiplexed on I/O Port P3 interrupts |   |                  |              |             |
| Activation Sense <sup>(4) (5)</sup>                                | Muxed with P3.6   | Maskable         | 0x0FFE8      | 3           |
| CP 1p8 Valid <sup>(4) (5)</sup>                                    | Muxed with P3.7   | Maskable         | 0x0FFE8      | 3           |
| Activation sleep counter timeout <sup>(4) (5)</sup>                | Muxed with P3.4   | Maskable         | 0x0FFE8      | 3           |
| CP 1p8 comparator out <sup>(4)(5)</sup>                            | Muxed with P3.5   | Maskable         | 0x0FFE8      | 3           |
| LCD CP comparator out <sup>(4)(5)</sup>                            | Muxed with P3.2   | Maskable         | 0x0FFE8      | 3           |
| APOOL comparator out <sup>(4)</sup>                                | Muxed with P3.3   | Maskable         | 0x0FFE8      | 3           |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.


(3) Interrupt flags are located in the module.

(4) No additional synchronization mechanisms beyond standard MSP430 interrupt synchronization

(5) Interrupt Signal is directly connoted without a de-glitcher mechanism.

## Special Function Registers (SFRs)

The AFE4110 SFRs are located in the lowest address space and can be accessed via word or byte formats. Other SFR registers documented in Texas Instruments MSP430x5xx "**Compact SYS Module User's Guide**" ([SLAU321](#)).

|               |   |   |
|---------------|---|---|
| <b>Legend</b> | <b>rw:</b>  | Bit can be read and written.                            |
|               | <b>rw-0,1:</b>  | Bit can be read and written. It is reset or set by PUC  |
|               | <b>rw-(0,1):</b>  | Bit can be read and written. It is reset or set by POR. |
|               | <b>rw-[0,1]:</b>  | Bit can be read and written. It is reset or set by BOR. |
|               |  | SFR bit is not present in device                        |

### SFRIE1, SFRIE1\_L, SFRIE1\_H, Interrupt Enable Register

|                 |                |    |              |              |    |             |              |
|-----------------|----------------|----|--------------|--------------|----|-------------|--------------|
| 15              | 14             | 13 | 12           | 11           | 10 | 9           | 8            |
| –               | –              | –  | –            | –            | –  | –           | <b>SVMIE</b> |
| r0              | r0             | r0 | r0           | r0           | r0 | r0          | rw-0         |
| 7               | 6              | 5  | 4            | 3            | 2  | 1           | 0            |
| <b>JMBOUTIE</b> | <b>JMBINIE</b> | –  | <b>NMIIE</b> | <b>VMAIE</b> | –  | <b>OFIE</b> | <b>WDTIE</b> |
| rw-0            | rw-0           | r0 | rw-0         | rw-0         | r0 | rw-0        | rw-0         |

|                 |             |  |
|-----------------|-------------|--|
| <b>Reserved</b> | Bits 15 – 9 | Reserved. Read back as 0   |
| <b>SVMIE</b>    | Bit 8       | SVM interrupt enable flag.<br>0 interrupts disabled<br>1 interrupts enabled  |
| <b>JMBOUTIE</b> | Bit 7       | JTAG mailbox output interrupt enable flag.<br>0 interrupts disabled<br>1 interrupts enabled  |
| <b>JMBINIE</b>  | Bit 6       | JTAG mailbox input interrupt enable flag.<br>0 interrupts disabled<br>1 interrupts enabled   |
| <b>Reserved</b> | Bit 5       | Reserved. Reads back as 0  |
| <b>NMIIE</b>    | Bit 4       | NMI pin interrupt enable flag.<br>0 interrupts disabled<br>1 interrupts enabled  |
| <b>VMAIE</b>    | Bit 3       | Vacant memory access interrupt enable flag.<br>0 interrupts disabled<br>1 interrupts enabled   |
| <b>Reserved</b> | Bit 2       | Reserved. Reads back as 0  |
| <b>OFIE</b>     | Bit 1       | Oscillator fault interrupt enable flag. 0 interrupts disabled 1 interrupts enabled   |
| <b>WDTIE</b>    | Bit 0       | Watchdog timer interrupt enable. This bit enables the WDTIFG interrupt for interval timer mode. It is not necessary to set this bit for watchdog mode. Because other bits in –IE1 may be used for other modules, it is recommended to set or clear this bit using BIS.B or BIC.B instructions, rather than MOV.B or CLR.B instruction<br>0 interrupts disabled<br>1 interrupts enabled |

**SFRIFG1, SFRIFG1\_L, SFRIFG1\_H, Interrupt Flag Register**

|                  |                 |    |               |               |    |              |               |
|------------------|-----------------|----|---------------|---------------|----|--------------|---------------|
| 15               | 14              | 13 | 12            | 11            | 10 | 9            | 8             |
| –                | –               | –  | –             | –             | –  | –            | <b>SVMIFG</b> |
| r0               | r0              | r0 | r0            | r0            | r0 | r0           | rw-0          |
| 7                | 6               | 5  | 4             | 3             | 2  | 1            | 0             |
| <b>JMBOUTIFG</b> | <b>JMBINIFG</b> | –  | <b>NMIIFG</b> | <b>VMAIFG</b> | –  | <b>OFIFG</b> | <b>WDTIFG</b> |
| rw-0             | rw-0            | r0 | rw-0          | rw-0          | r0 | rw-0         | rw-0          |

|                  |             |   |
|------------------|-------------|---|
| <b>Reserved</b>  | Bits 15 – 9 | Reserved. Read back as 0  |
| <b>SVMIFG</b>    | Bit 8       | SVM interrupt flag. This bit signals that the A-POOL comparator signaled an SVM event either low voltage or high voltage depending on setup<br>0 no interrupt pending<br>1 interrupt pending  |
| <b>JMBOUTIFG</b> | Bit 7       | JTAG mailbox output interrupt flag<br>0 no interrupt pending. When in 16-bit mode (JMBMODE = 0), this bit is cleared automatically when JMBO0 has been written by the CPU. When in 32-bit mode (JMBMODE = 1), this bit is cleared automatically when both JMBO0 and JMBO1 have been written by the CPU. This bit is also cleared when the associated vector in SYSSNIV has been read<br>1 interrupt pending, JMBO registers are ready for new messages. In 16-bit mode (JMBMODE=0) JMBO0 has been received by JTAG. In 32-bit mode (JMBMODE=1) , JMBO0 and JMBO1 have been received by JTAG |
| <b>JMBINIFG</b>  | Bit 6       | JTAG mailbox input interrupt flag<br>0 no interrupt pending. When in 16-bit mode (JMBMODE = 0), this bit is cleared automatically when JMBIO is read by the CPU. When in 32-bit mode (JMBMODE = 1), this bit is cleared automatically when both JMBIO and JMBI1 have been read by the CPU. This bit is also cleared when the associated vector in SYSSNIV has been read<br>1 interrupt pending, a message is waiting in the JMBIN registers. In 16-bit mode (JMBMODE = 0) when JMBIO has been written by JTAG. In 32 bit mode (JMBMODE = 1) when JMBIO and JMBI1 have been written by JTAG  |
| <b>Reserved</b>  | Bit 5       | Reserved. Reads back as 0   |
| <b>NMIIFG</b>    | Bit 4       | NMI pin interrupt flag<br>0 no interrupt pending<br>1 interrupt pending   |
| <b>VMAIFG</b>    | Bit 3       | Vacant memory access interrupt flag<br>0 no interrupt pending<br>1 interrupt pending  |
| <b>Reserved</b>  | Bit 2       | Reserved. Reads back as 0   |
| <b>OFIFG</b>     |             | Oscillator fault interrupt flag<br>0 no interrupt pending<br>1 interrupt pending  |
| <b>WDTIFG</b>    | Bit 0       | Watchdog timer interrupt flag. In watchdog mode, WDTIFG remains set until reset by software. In interval mode, WDTIFG is reset automatically by servicing the interrupt, or can be reset by software.<br>Because other bits in ~IFG1 may be used for other modules, it is recommended to clear WDTIFG by using BIS.B or BIC.B instructions, rather than MOV.B or CLR.B instructions.<br>0 no interrupt pending<br>1 interrupt pending   |

**SFRRPCR, SFRRPCR\_H, SFRRPCR\_L, Reset Pin Control Register**

|    |    |    |    |                 |                 |                 |               |
|----|----|----|----|-----------------|-----------------|-----------------|---------------|
| 15 | 14 | 13 | 12 | 11              | 10              | 9               | 8             |
| –  | –  | –  | –  | –               | –               | –               | –             |
| r0 | r0 | r0 | r0 | r0              | r0              | r0              | r0            |
| 7  | 6  | 5  | 4  | 3               | 2               | 1               | 0             |
| –  | –  | –  | –  | <b>SYSRSTRE</b> | <b>SYSRSTUP</b> | <b>SYSNMIES</b> | <b>SYSNMI</b> |
| r0 | r0 | r0 | r0 | r1              | r1              | r1              | rw-0          |

|                 |           |   |
|-----------------|-----------|---|
| <b>Reserved</b> | Bits 15–9 | Reserved. Read back as 0  |
| <b>SYSRSTRE</b> | Bit 3     | Reset Pin resistor enable<br>0 Pullup / pulldown resistor at the RST/NMI pin is disabled<br>1 Pullup / pulldown resistor at the RST/NMI pin is enabled  |
| <b>SYSRSTUP</b> | Bit 2     | Reset resistor pin pullup / pulldown<br>0 Pulldown is selected<br>1 Pullup is selected  |
| <b>SYSNMIES</b> | Bit 1     | NMI edge select. This bit selects the interrupt edge for the NMI interrupt when SYSNMI = 1. Modifying this bit can trigger an NMI. Modify this bit when SYSNMI = 0 to avoid triggering an accidental NMI<br>0 NMI on rising edge<br>1 NMI on falling edge |
| <b>SYSNMI</b>   | Bit 0     | NMI select. This bit selects the function for the RST/NMI pin<br>0 Reset function<br>1 NMI function   |

**Table 4. Memory Organization**

|                              | TYPE      | AFE4110A (Dev RAM)                     | Type      | AFE4110B (Custom ROM)                  |
|------------------------------|-----------|--|-----------|--|
| Interrupt Vectors            | RAM       | 32 B<br>0xFFE0 <sup>(1)</sup> – 0xFFFF | ROM       | 32 B<br>0xFFE0 <sup>(1)</sup> – 0xFFFF |
| Development RAM              | RAM       | 14KB<br>0xC800 – 0xFFFF                | —         | —                                      |
| Application ROM              | —         | —                                      | ROM       | 14KB<br>0xC800 – 0xFFFF                |
| TI Start Up Code (DSUC/PSUC) | ROM       | 2KB<br>0xC000 – 0xC7FF                 | ROM       | 2KB<br>0xC000 – 0xC7FF                 |
| TI Boot Loader Code          | ROM       | 14KB<br>0x1E0 – 0x55FF                 | —         | —                                      |
| Application RAM              | RAM       | 256B<br>0x1D00 – 0x1DFF                | RAM       | 256B<br>0x1D00 – 0x1DFF                |
| Application LRAM (lockable)  | RAM       | 128B<br>0x1C80 – 0x1CFF                | RAM       | 128B<br>0x1C80 – 0x1CFF                |
| Calibration RAM (lockable)   | RAM       | 128B<br>0x1C00 – 0x1C7F                | RAM       | 128B<br>0x1C00 – 0x1C7F                |
| Peripherals                  | Registers | 4 kB<br>0x0000 – 0x0FFF                | Registers | 4 kB<br>0x0000 – 0x0FFF                |

(1) not the whole interrupt vector range of CSYS is used on AFE4110 devices

## Start-Up Code (SUC)

The AFE4110A Development Start-Up Code (DSUC) supports system debug via a JTAG connection to an external emulator. After the release of RST/NMI, the DSUC checks for the presence of a JTAG emulator by reading the contents of the JTAG Mailbox Register. If the emulation password is present in the JTAG Mailbox, the DSUC unlocks full access to the on chip emulation features, then enters LPM4 while waiting for to enter the debug session. If the emulation password is not present in the JTAG Mailbox, the DSUC initiates execution of the Loader Code.

The AFE4110B Production Start-Up Code (PSUC) also supports system debug via a JTAG connection to an external emulator. The difference is that the PSUC checks for the contents of the JTAG Mailbox Register for a confidential password. If the confidential password is present in the JTAG Mailbox, the PSUC unlocks full access to the on chip emulation features, then enters LPM4 while waiting for to enter the debug session. If the confidential password is not present in the JTAG Mailbox when RST/NMI is released, the PSUC initiates execution of the custom ROM code.

## Loader Code (Loader)

The AFE4110A Loader checks for the presence of an external SPI memory device containing a valid data/code package. The Loader transfers a validated data/code package into Development RAM. During validation and transfer, the on chip 1.85V charge pump is enabled to supply power to VDDIO and the external SPI memory device. (PCB level connections are required.) Once the transfer of the data/code package is complete, the charge pump is disabled, the AFE4110 registers are returned to their default contents, and execution of the code loaded in Development RAM is initiated.

## RAM Memory

The RAM memory is split into three ranges for different purposes: Application memory, lockable application memory and calibration memory.

Lockable application memory and calibration memory can be protected against accidental erasure by setting a dedicated lock bit in the special functions register (System Maintenance Register).

Note: The lockable memory is locked by default after release of RST/NMI or exit from LPM5. The user code must clear the lock bits in the Special Function Register after release of RST/NMI or exit from LPM5 to enable writing lockable memory.

## Peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, see the MSP430x5xx Family User's Guide (SLAU208) and the MSP430x09x Family User's Guide (SLAU321).

## Digital I/O

There are 4 I/O ports implemented: P1 (7 I/O lines), P2 (4 I/O lines), P3 (6 I/O lines) and P4 (4 I/O lines)

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on P1 and P3(0-5) ports.
- Programmable pullup on P2, P4 and P3(6,7) ports.
- External VDD (VDDIO) supply (1.1-3.3V range) to P2, P4 and P3(6,7) ports.
- Edge-selectable interrupt input capability for all ports.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1, P2, P3 and P4) or word-wise in pairs (P1/P2 combo).

## Oscillator and System Clock

The clock system in the AFE4110 family of devices is supported by the Compact Clock System (CCS) module that includes an internal 20kHz current controlled low frequency oscillator (LF-OSC), an internal adjustable (1-5.4MHz) current controlled high frequency oscillator (HF-OSC), a 1KHz ultra low power oscillator for the activation block, an external clock input from CLKIN, and a 32kHz crystal oscillator. The CCS module is designed to meet the requirements of both low system cost and low-power consumption. The CCS provides a fast turn-on of the oscillators in less than 1 ms.

The CCS module provides the following clock signals:

- Auxiliary clock (ACLK) is software selectable for individual peripheral modules. ACLK is sourced from the internal LF-OSC, the internal HF-OSC, an external source via CLKIN, or the crystal oscillator.
- Main clock (MCLK) is the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem master clock is software selectable by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- VLOCLK this is a low frequency clock sourced by LF-OSC that is constantly available.

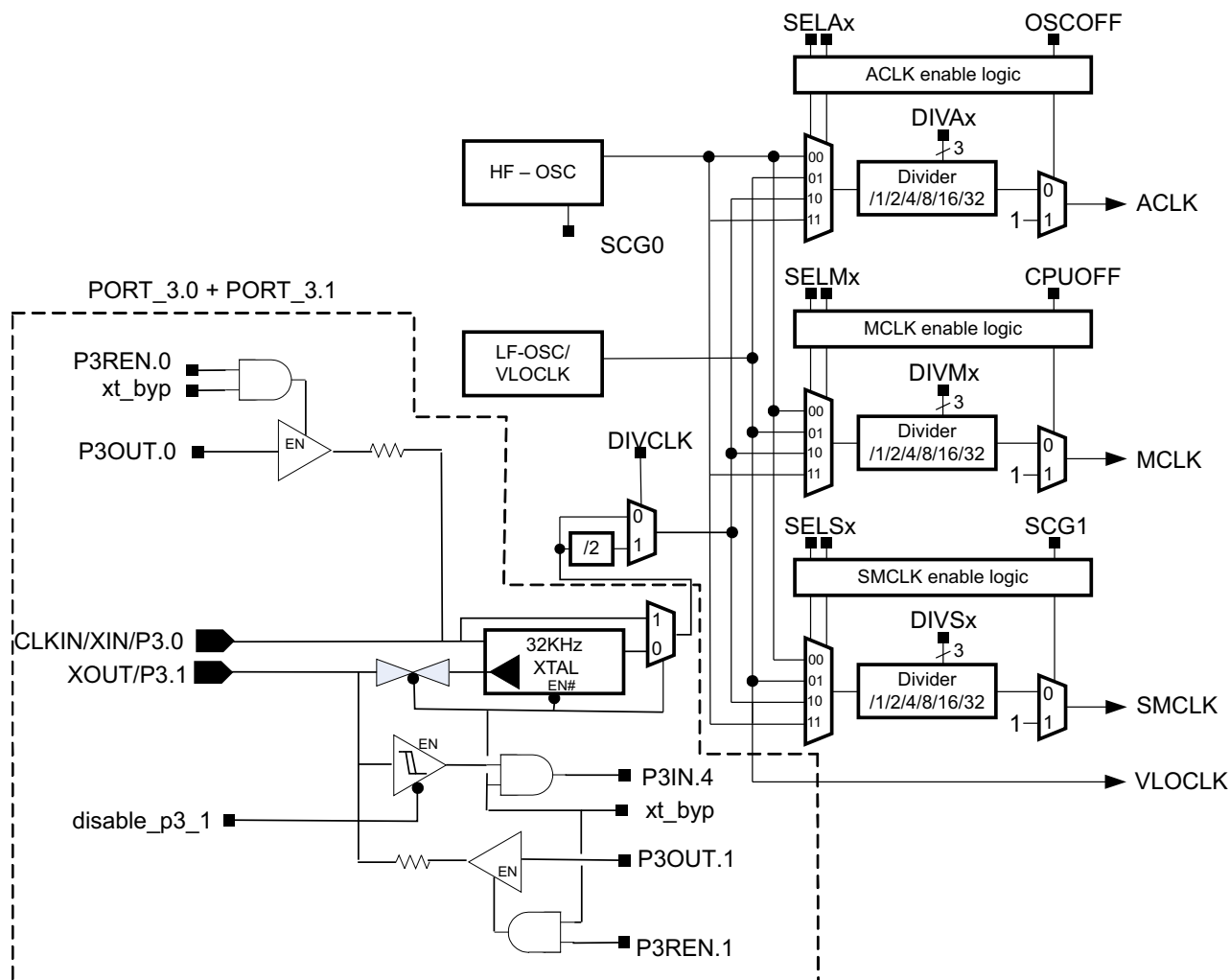


Figure 1. Block Diagram of Compact Clock System (CCS)

## Watchdog Timer (WDT\_A)

The primary function of the watchdog timer (WDT\_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals. For a complete description of WDT\_A, see the Watchdog Timer (WDT\_A) section of the MSP430x09x Family Users Guide (SLAU321).

**Table 5. WDT\_A Signal Connections**

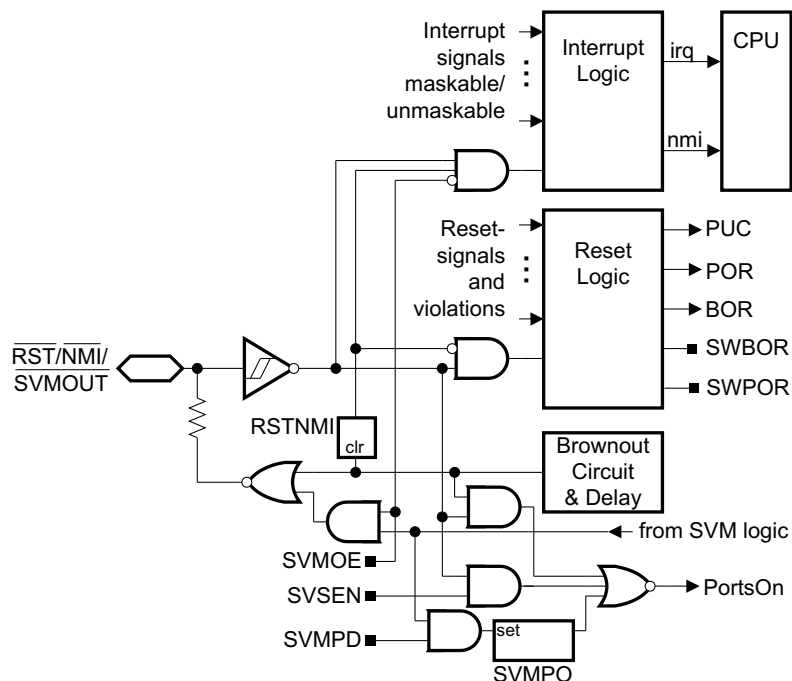
| DEVICE CLOCK SIGNAL | MODULE CLOCK SIGNAL |
|---------------------|---------------------|
| ACLK                | ACLK                |
| SMCLK               | SMCLK               |
| LF-OSC-CLK          | VLOCLK              |
| HF-OSC-CLK          | X-CLK               |

## Compact System Module (C-SYS)

The Compact SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, as well as, configuration management. It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application. For a complete description of C-SYS, see the Compact System chapter of the MSP430x09x Family Users Guide (SLAU321).

## Reset/NMI/SVMOUT System

The Reset system of the MSP430x09x family features the function Reset input, Reset output, NMI input, SVM output and SVS input.



**Figure 2. Block Diagram of Reset/NMI/SVM and PortsOn logic**



**Table 6. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | INTERRUPT VECTOR            | WORD ADDRESS | OFFSET  | PRIORITY |
|---------------------------|-----------------------------|--------------|---------|----------|
| SYSRSTIV, System Reset    | No interrupt pending        | 019Eh        | 00h     | Highest  |
|                           | Brownout (BOR)              |              | 02h     |          |
|                           | SVMBOR (BOR)                |              | 04h     |          |
|                           | RST/NMI (BOR)               |              | 06h     |          |
|                           | DoBOR (BOR)                 |              | 08h     |          |
|                           | Security violation (BOR)    |              | 0Ah     |          |
|                           | DoPOR(POR)                  |              | 0Ch     |          |
|                           | WDT timeout (PUC)           |              | 0Eh     |          |
|                           | WDT key violation (PUC)     |              | 10h     |          |
|                           | CCS key violation           |              | 12h     |          |
|                           | PMM key violation           |              | 14h     |          |
|                           | Peripheral area fetch (PUC) |              | 16h     |          |
|                           | Reserved                    |              | 18h-3Eh |          |
| SYSSNIV, System NMI       | No interrupt pending        | 019Ch        | 00h     | Highest  |
|                           | SVMIFG                      |              | 02h     |          |
|                           | VMAIFG                      |              | 04h     |          |
|                           | JMBINIFG                    |              | 06h     |          |
|                           | JMBOUTIFG                   |              | 08h     |          |
|                           | Reserved                    |              | 0Ah-3Eh |          |
| SYSUNIV, User NMI         | No interrupt pending        | 019Ah        | 00h     | Highest  |
|                           | NMIFG                       |              | 02h     |          |
|                           | OFIFG                       |              | 04h     |          |
|                           | BERR                        |              | 06h     |          |
|                           | Reserved                    |              | 08h-3Eh |          |
| SYSBERRIV, Bus Error      | No interrupt pending        | 0198h        | 00h     | Lowest   |
|                           | Reserved                    |              | 02h-3Eh |          |

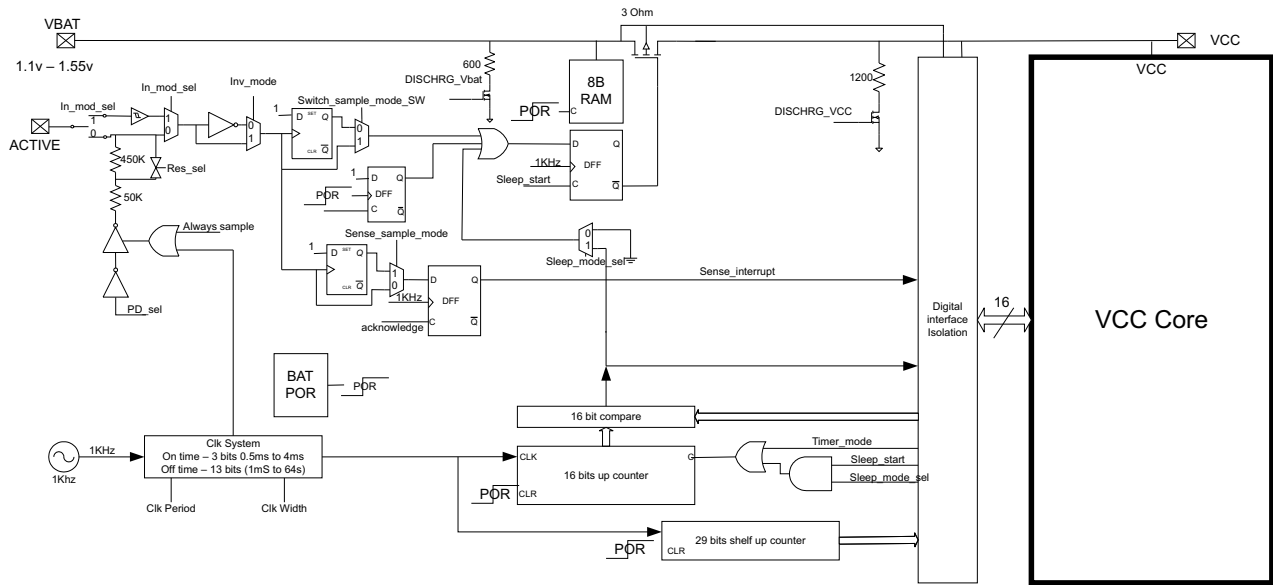
# AFE4110

SLLSE48 – JANUARY 2012

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## Activation Block

The AFE4110 Activation Block controls entry and exit from "deep-sleep" (LPM5) mode. When the device is in LPM5, power is disconnected from AFE4110 CPU and all peripherals (including RAM, LCD and I/O) other than the Activation block. When exiting LPM5, power is reapplied to the CPU core and peripherals. Exiting "deep-sleep" (LPM5) mode is termed "wake up". The Activation block wakes up the CPU core and peripherals based on how it was configured prior to entering LPM5. Wake up takes place based either on a transition on the Activation Sense (ACTIVE) input or after a number of Activation Clock cycles have been counted. The ACTIVE input can be configured to respond to either LOW-to-HIGH or HIGH-to-LOW transitions. The number of Activation clock cycles to be counted prior to exiting LPM5 is configurable.



**Activation Block Hardware Status and Control Registers:**

The Activation Block hardware registers control the method of entry and exit from deep sleep (LPM5) mode. Additional features of the Activation Block registers include the following:

- VBAT Power On Reset (POR) Circuit – The VBAT POR is designed to reset the Activation block during initial system power up that is typical of installation of a battery into the final product.
- 4-16bit words (8B) RAM – This RAM is implemented in hardware registers. The contents of these registers is cleared at initial system power up by VBAT POR. The fact that these registers are cleared at initial system power up allow them to be used to determine whether the CPU is being powered up by battery insertion or exit from LPM5.
- 16bit Sleep Counter – The Activation block can be configured to exit LPM5 after the number of Activation clock cycles that are selected. The counter can also be used as a general purpose down counter without entering LPM5.
- 28bit Shelf Counter – This counter starts incrementing after the first time the device enters LPM5. After the first exit from LPM5 this counter stops and its outputs remain static until VBAT power is removed. The intent is for this counter to record number of Activation clock periods between initial insertion of a battery in to the final product and the first usage of the final product. In other words, this counter indicates the length of time that the final product is on the shelf prior to being used by a consumer.
- ACTIVE Sample Clock – To minimize the power required for determining transitions on the ACTIVE pad, the state of the ACTIVE pad is sampled only at intervals which are set by the duty cycle of the ACTIVE Sample Clock. The period between samples and the duration of the sample interval are configurable.

The Activation Block 'strobe' registers are not memory mapped and require a multi-step procedure for Reads and Writes of their contents from the CPU. The Activation register strobe refers to the hardware signal used to capture data into the bank of hardware registers. The strobe number (strobe address) indicates the bank of 16-hardware registers to be accessed. Only 16-bit (word) accesses are supported.

**Activation Strobe Register Read Procedure:**

The steps to Read a particular Activation strobe register follows:

1. Write the strobe address of the Activation register to be Read to the ACTIVATION\_RD\_ADDR register
2. Wait 10-MCLK clock cycles for the transfer of selected data to the ACTIVATION\_DATAIN register
3. Read to contents of the ACTIVATION\_DATAIN register

**Activation Strobe Register Write Procedure:**

The steps to Write Activation strobe registers follows:

1. Write to data value to be transferred to the Activation hardware register to the ACTIVATION\_DATAOUT register
2. Wait 10-MCLK clock cycles for data to transfer to the Activation block
3. Write a '1' to the bit corresponding to the Activation hardware register to be written into the ACTIVATION\_STROBES register.

Note: If multiple bits are written in the ACTIVATION\_STROBES register, multiple Activation hardware registers will be written

The table below describes the function of the Activation strobe registers.

**Table 7. Activation Strobe Register Function Table**

| data in #  | strobe0   | strobe1   | strobe2   | strobe3   | strobe4       | strobe5                  | strobe6               | strobe 7             |
|------------|-----------|-----------|-----------|-----------|---------------|--------------------------|-----------------------|----------------------|
| data in 0  | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | Res_sel               | ACTCLK_Freq_Sel<2:0> |
| data in 1  | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | PD_sel                |                      |
| data in 2  | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | Always_sample         |                      |
| data in 3  | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | Inv_mode              | Reserved             |
| data in 4  | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | Switch_sample_mode_SW | Reserved             |
| data in 5  | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | Switch_sample_mode    | Reserved             |
| data in 6  | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | In_mod_sel            | Reserved             |
| data in 7  | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | Sleep_mode_sel        | Reserved             |
| data in 8  | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | Reserved              | Reserved             |
| data in 9  | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | Sleep_start           | Reserved             |
| data in 10 | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | Timer_mode            | Reserved             |
| data in 11 | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | Reserved              | Reserved             |
| data in 12 | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Period | Reserved              | Reserved             |
| data in 13 | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Width  | DISCHRG_Vbat          | Reserved             |
| data in 14 | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Width  | DISCHRG_VCC           | Reserved             |
| data in 15 | RAM reg 0 | RAM reg 1 | RAM reg 2 | RAM reg 3 | sleep counter | ACTIVE Sample Clk Width  | Reserved              | Reserved             |

**Strobe0 - Strobe3:** Activation Block RAM Registers

**RAM Reg0 - RAM Reg3** - Bits 15 - 0 - Constantly powered registers for used as RAM (Cleared by assertion of VBAT POR)

**Strobe4:** Sleep Counter Register

**Sleep\_counter** - Bits 15 - 0 - Sleep counter output value

**Strobe5:** ACTIVE Sample Clock Configuration Register

**ACTIVE\_Sample\_Clock\_Period** - Bits 12 - 0 - Number of ACTCLK cycles per period of the ACTIVE sample clock

0x0000 sets the sampling period to ~8192ms

0x0001 sets the sampling period to ~1ms...

0x0009 sets the sampling period to ~9ms ...

0x1FFF sets the sampling frequency to ~8192ms

**ACTIVE\_Sample\_Clock\_Width** - Bits 15 - 13 - Number of ACTCLK half-cycles per sample interval of the ACTIVE sample clock

**Strobe6:** LPM5 Configuration Register

**Res\_sel** - Bit 0 - PU/PD Resistor Select

1 - 500KΩ resistor selected

0 - 50KΩ resistor selected

**PD\_sel** - Bit 1 - Pull Down Select

- 1 - PMOS sensing - internal PU is connected
- 0 - NMOS sensing – internal PD is connected

**Always\_sample** - Bit 1 ACTIVE Sampling Select

- 1 - Continuous ACTIVE input sensing
- 0 - ACTIVE input sensing at sampled intervals

**Inv\_mode** - Bit 3 - Inverted Mode

- 1 - Low to high transition sensing
- 0 - High to low transition sensing

**Switch\_sample\_mode\_SW** - Bit 4 - Switch Sample Mode Switch

- 1 - Edge sensing for external switch closure selected
- 0 - Level sensing for external switch closure selected

**Switch\_sample\_mode** - Bit 5 - Switch Sample Mode

- 1 - Edge sensing for the sense\_interrupt
- 0 - Level sensing for the sense\_interrupt

**In\_mod\_sel** - Bit 6 - Input Mode Select

- 1 - Low current hysteresis sense inverter selected
- 0 - Standard input selected

**Sleep\_mode\_sel** - Bit 7 - Sense Mode Select

- 1 - high selects power down with counter;
- 0 - low selects power down without counter

**Sleep\_start** - Bit 9 - Sleep Start

- 1 - Start power down
- 0 - Normal operating mode (This bit must be cleared by TI start up code.)

**Timer\_mode** - Bit 10 - Timer Mode

- 1- Start sleep counter without entering LPM5
- 0 - Sleep counter is starting when entering LPM5 if sleep counter mode is selected

**DISCHRG\_Vbat** - Bit 13 - Discharge VBAT Power

- 1 - Discharge Vbat voltage through 600  $\Omega$  resistor
- 0 - No VBAT discharging selected

**DISCHRG\_VCC** - Bit 14 - Discharge VCC Core

- 1- Discharge Vcc voltage through 1200  $\Omega$  resistor
- 0 - No discharge of VCC Core voltage select

**Strobe7:** Activation Clock Frequency Select Register

ACTCLK\_Freq\_Sel - Bits 2 - 0 - Trims the ACT oscillator to set the frequency

**Table 8. ACTIVE Sample Clock Width**

| SETTING | ACTIVE Sample Clock Interval |
|---------|------------------------------|
| 000     | 0.5 ACTCLK Period            |
| 001     | 1 ACTCLK Period              |
| 010     | 1.5 Clock Period             |
| 011     | 2 Clock Period               |
| 100     | 2.5 Clock Period             |
| 101     | 3 Clock Period               |
| 110     | 3.5 Clock Period             |
| 111     | 4 Clock Period               |

**Table 9. Activation Clock Frequency Selections**

| SETTING | CAP SETTING | FREQUENCY |
|---------|-------------|-----------|
| 000     | 60 fF       | 1 kHz     |
| 001     | 120 fF      | 0.75 kHz  |
| 010     | 180 fF      | 0.35 kHz  |
| 011     | 240 fF      | 250 Hz    |
| 100     | 150 fF      | 400 kHz   |
| 101     | 210 fF      | 280 Hz    |
| 110     | 270 fF      | 220 Hz    |

**Activation Registers**
**SHELF\_CNT\_LO: Shelf counter low**

| 15                       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|--------------------------|----|----|----|----|----|----|----|
| <b>s_cnt_low (cont.)</b> |    |    |    |    |    |    |    |
| r0                       | r0 | r0 | r0 | r0 | r0 | r0 | r0 |
| 7                        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>s_cnt_low</b>         |    |    |    |    |    |    |    |
| r0                       | r0 | r0 | r0 | r0 | r0 | r0 | r0 |

**s\_cnt\_low** Bits 0-15 Lower 16 bits of Shelf counter

This is a read only Register

**SHELF\_CNT\_HI: Shelf counter high**

| 15                | 14 | 13 | 12                        | 11 | 10 | 9  | 8  |
|-------------------|----|----|---------------------------|----|----|----|----|
| –                 | –  | –  | <b>s_cnt_high (cont.)</b> |    |    |    |    |
| r0                | r0 | r0 | r0                        | r0 | r0 | r0 | r0 |
| 7                 | 6  | 5  | 4                         | 3  | 2  | 1  | 0  |
| <b>s_cnt_high</b> |    |    |                           |    |    |    |    |
| r0                | r0 | r0 | r0                        | r0 | r0 | r0 | r0 |

**s\_cnt\_high** Bits 0-12 Upper 13 bits of Shelf counter

This is a read only Register

**ACTIVATION\_DATAIN: Activation data in**

| 15                      | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------------------|----|----|----|----|----|---|---|
| <b>act_d_in (cont.)</b> |    |    |    |    |    |   |   |
| 7                       | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| <b>act_d_in</b>         |    |    |    |    |    |   |   |

**act\_d\_in** Bits 0-15 Activation Data In - Value of the Strobe7-0 register which is selected by the ACTIVATION\_RD\_ADDR register

This is a read only Register

**ACTIVATION\_DATAOUT: Activation data out**

|                          |           |      |  |      |      |      |      |  |
|--------------------------|-----------|------|--|------|------|------|------|--|
| 15                       | 14        | 13   | 12   | 11   | 10   | 9    | 8    |  |
| <b>act_d_out (cont.)</b> |           |      |  |      |      |      |      |  |
| rw-0                     | rw-0      | rw-0 | rw-0   | rw-0 | rw-0 | rw-0 | rw-0 |  |
| 7                        | 6         | 5    | 4  | 3    | 2    | 1    | 0    |  |
| <b>act_d_out</b>         |           |      |  |      |      |      |      |  |
| rw-0                     | rw-0      | rw-0 | rw-0   | rw-0 | rw-0 | rw-0 | rw-0 |  |
| <b>act_d_out</b>         | Bits 0-15 |      | Activation Data Out - The data value to be written into the Strob1-0 register which is selected by the ACTIVATION_STROBES register |      |      |      |      |  |

**ACTIVATION\_STROBES: Activation strobes**

|                 |              |              |   |              |              |              |              |  |
|-----------------|--------------|--------------|---|--------------|--------------|--------------|--------------|--|
| 15              | 14           | 13           | 12  | 11           | 10           | 9            | 8            |  |
| <b>Password</b> |              |              |   |              |              |              |              |  |
| rw-1            | rw-0         | rw-0         | rw-1  | rw-0         | rw-1         | rw-1         | rw-0         |  |
| 7               | 6            | 5            | 4   | 3            | 2            | 1            | 0            |  |
| <b>strb7</b>    | <b>strb6</b> | <b>strb5</b> | <b>strb4</b>  | <b>strb3</b> | <b>strb2</b> | <b>strb1</b> | <b>strb0</b> |  |
| rw-0            | rw-0         | rw-0         | rw-0  | rw-0         | rw-0         | rw-0         | rw-0         |  |
| strbx           | Bits 0-15    |              | Activation Strobe - These bits are 'one-hot' coded to select the Strob7-0 register to be written with the contents of the ACTIVATION_DATAOUT register |              |              |              |              |  |

|          |           |  |
|----------|-----------|--|
| strb0    | Bit 0     | Activation strobe 0  |
| strb1    | Bit 1     | Activation strobe 1  |
| strb2    | Bit 2     | Activation strobe 2  |
| strb3    | Bit 3     | Activation strobe 3  |
| strb4    | Bit 4     | Activation strobe 4  |
| strb5    | Bit 5     | Activation strobe 5  |
| strb6    | Bit 6     | Activation strobe 6  |
| strb7    | Bit 7     | Activation strobe 7  |
| Password | Bits 8-15 | Write 0xA5 to initiate Strobex register Write - Always reads back 0x96 |

Strb0-7 are self clearing bits

**ACTIVATION\_RD\_ADDR: Activation read address**

|                 |          |     |   |      |                 |      |      |  |
|-----------------|----------|-----|---|------|-----------------|------|------|--|
| 15              | 14       | 13  | 12  | 11   | 10              | 9    | 8    |  |
| –               | –        | –   | –   | –    | –               | –    | –    |  |
| r-0             | r-0      | r-0 | r-0   | r-0  | r-0             | r-0  | r-0  |  |
| 7               | 6        | 5   | 4   | 3    | 2               | 1    | 0    |  |
| –               | –        | –   | –   | –    | <b>read_add</b> |      |      |  |
| r-0             | r-0      | r-0 | r-0   | rw-0 | rw-0            | rw-0 | rw-0 |  |
| <b>read_add</b> | Bits 0-2 |     | Register Read Address - Decimal coded index of Strobe7-0 register to be read back in ACTIVATION_DATAIN register |      |                 |      |      |  |

**ACTIVATION\_STATUS: Activation Status**

|     |     |     |     |     |                 |                  |                  |
|-----|-----|-----|-----|-----|-----------------|------------------|------------------|
| 15  | 14  | 13  | 12  | 11  | 10              | 9                | 8                |
| –   | –   | –   | –   | –   | –               | –                | –                |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0             | r-0              | r-0              |
| 7   | 6   | 5   | 4   | 3   | 2               | 1                | 0                |
| –   | –   | –   | –   | –   | <b>act_test</b> | <b>act_sleep</b> | <b>act_sense</b> |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0             | r-0              | r-0              |

This is a read only register.

act\_sense Bit 0 Logic high signal indicate sense button changed state (pushed)  
 act\_sleep Bit 1 Sleep Comparator OUT. Can be configured like MSP Timer\_0 out (INT\_rise, INT fall, Level Latch High, Level latch Low)  
 act\_test Bit 2 Counter out for testing

### ACTIVATION\_SENSE: Activation Sense

|     |     |     |     |     |     |     |                      |
|-----|-----|-----|-----|-----|-----|-----|----------------------|
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8                    |
| –   | –   | –   | –   | –   | –   | –   | –                    |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0                  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0                    |
| –   | –   | –   | –   | –   | –   | –   | <b>Act_sense_cir</b> |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0                  |

This is a self clearing register

**activation\_sense\_cir** Bit 0 Acknowledge for clearing the sense\_interrupt signal (should be a high pulse that can comes from SW or HW)

### Timer0\_A3

Timer0\_A3 is a 16-bit timer/counter with three capture/compare registers. Timer0\_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer0\_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. AFE4110 Timer-0 has different Clocks Sources and CCx input multiplexing, compared to MSP430x5 documentation. Timer-0 Clock sources and the CCx input signals described in this document.



Timer0\_A3 Signal Connections and Block Diagrams

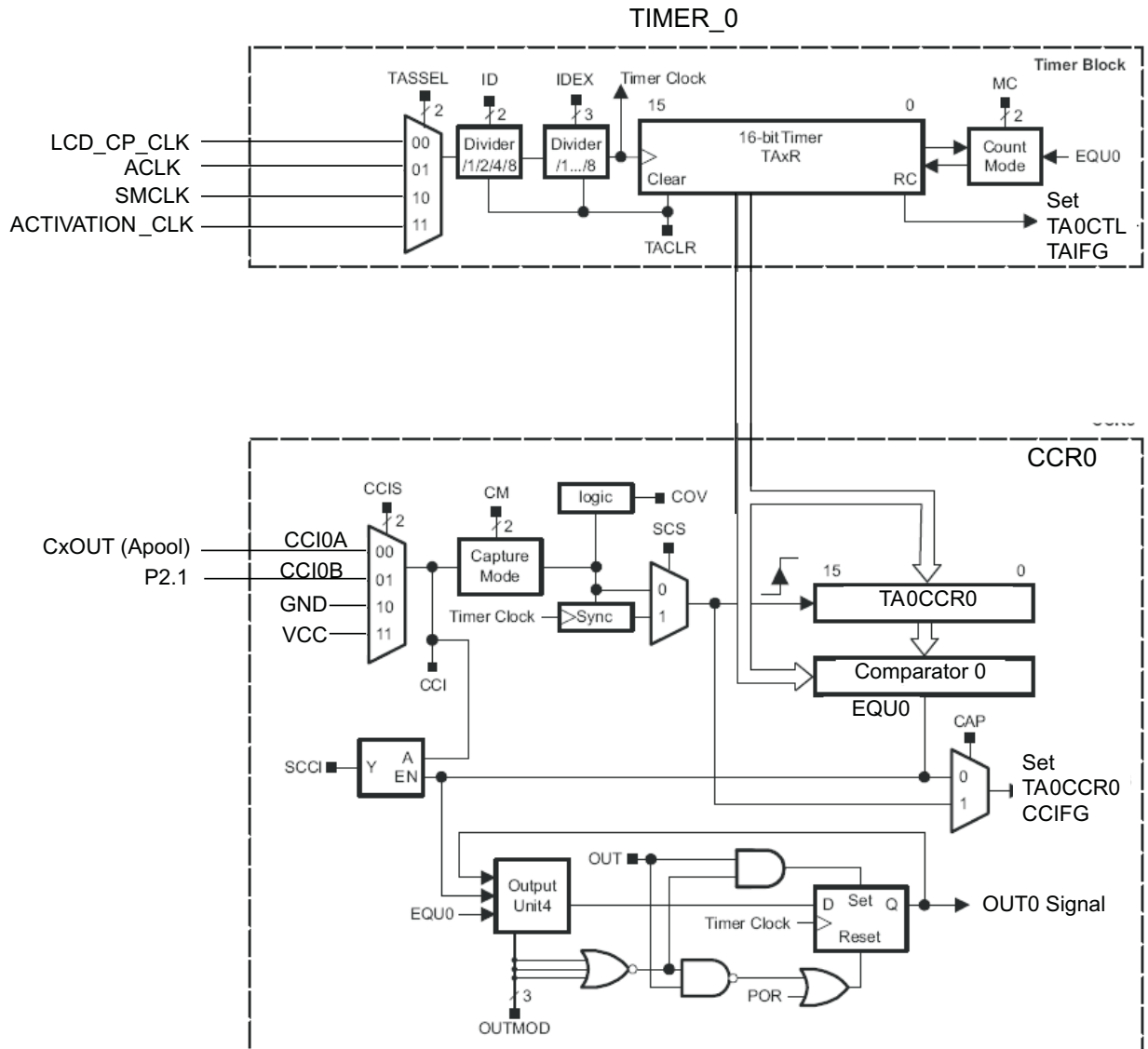


Figure 3. Timer0\_CCR0 Block Diagram

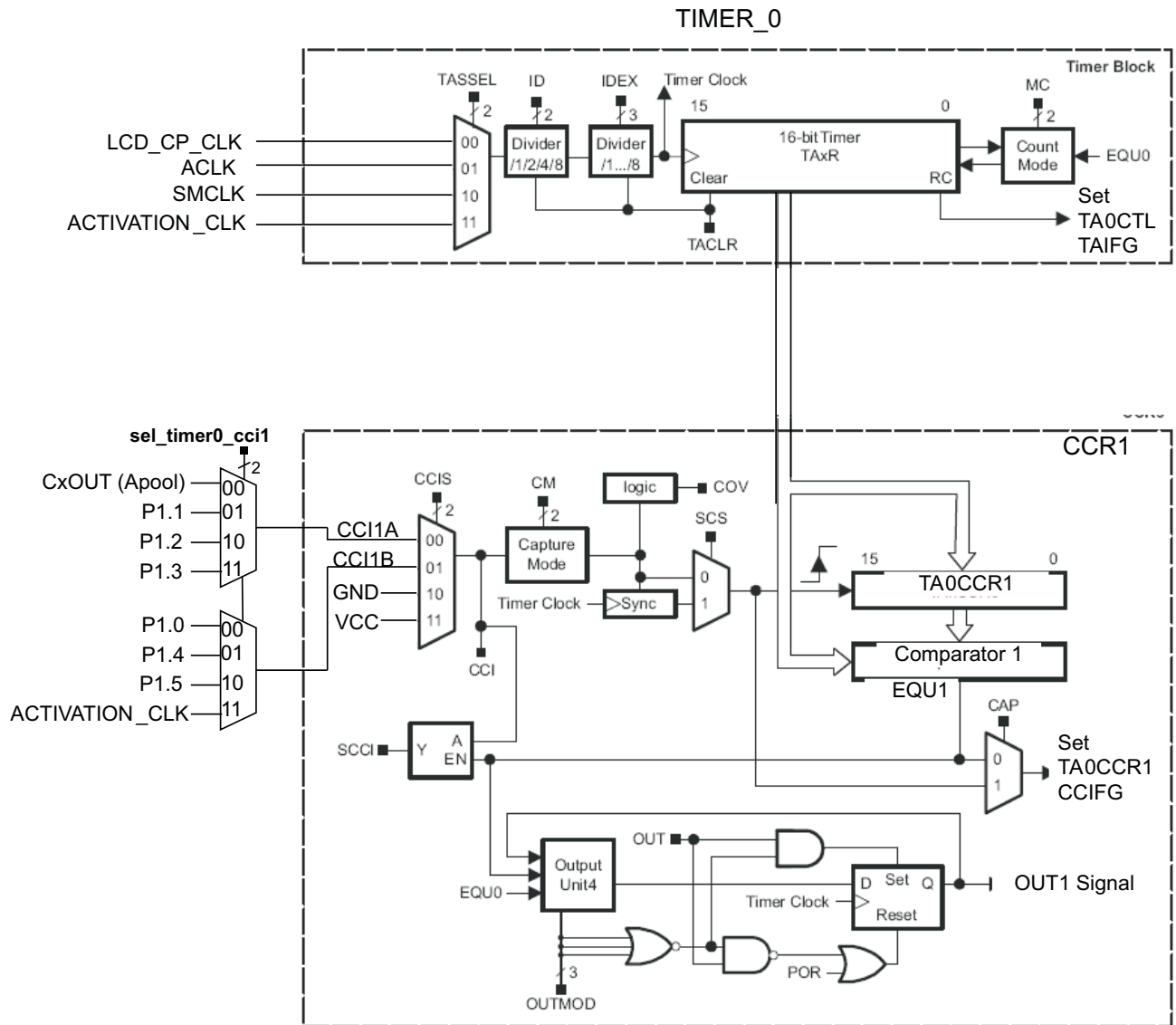


Figure 4. Timer0\_CCR1 Block Diagram

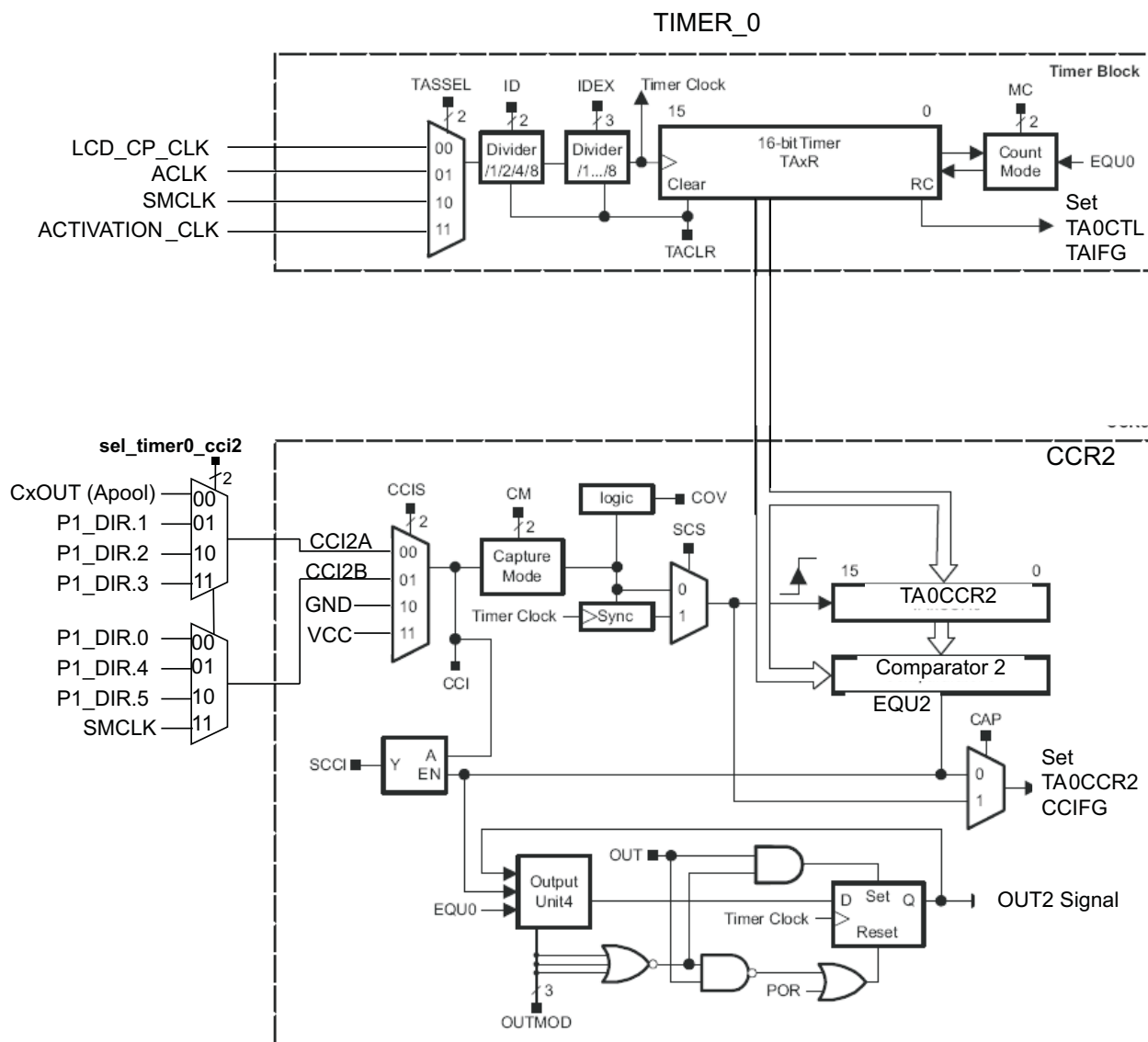


Figure 5. Timer0\_CCR2 Block Diagram

### Timer1\_A3

Timer1\_A3 is a 16-bit timer/counter with three capture/compare registers. Timer1\_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer1\_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. AFE4110 Timer-1 has different Clock Sources and CCx input multiplexing, compared to MSP430x5 documentation. Timer-1 Clock sources and the CCx input signals described in this document.

Timer1\_A3 Signal Connections and Block Diagrams

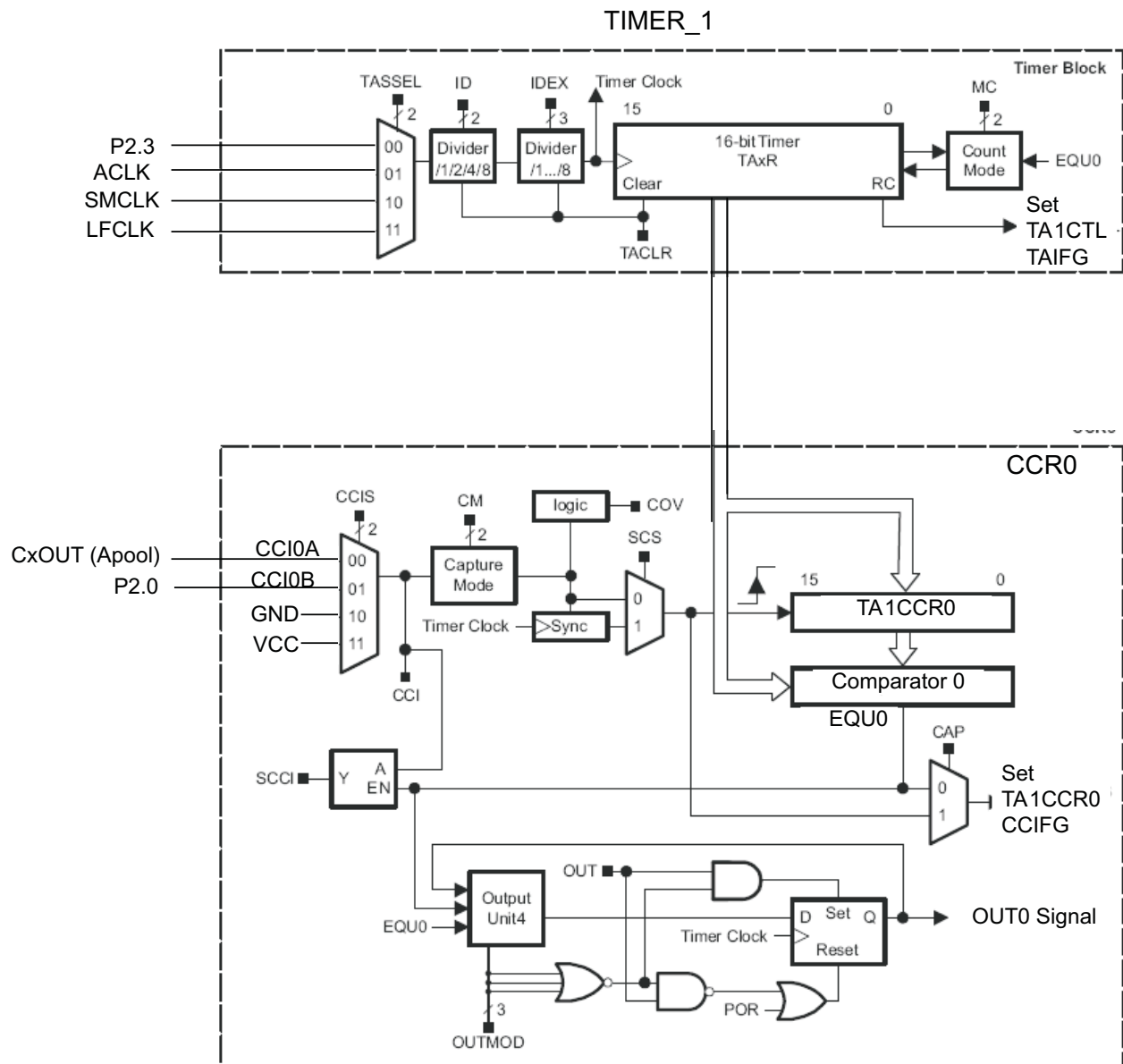


Figure 6. Timer1\_CCR0 Block Diagram

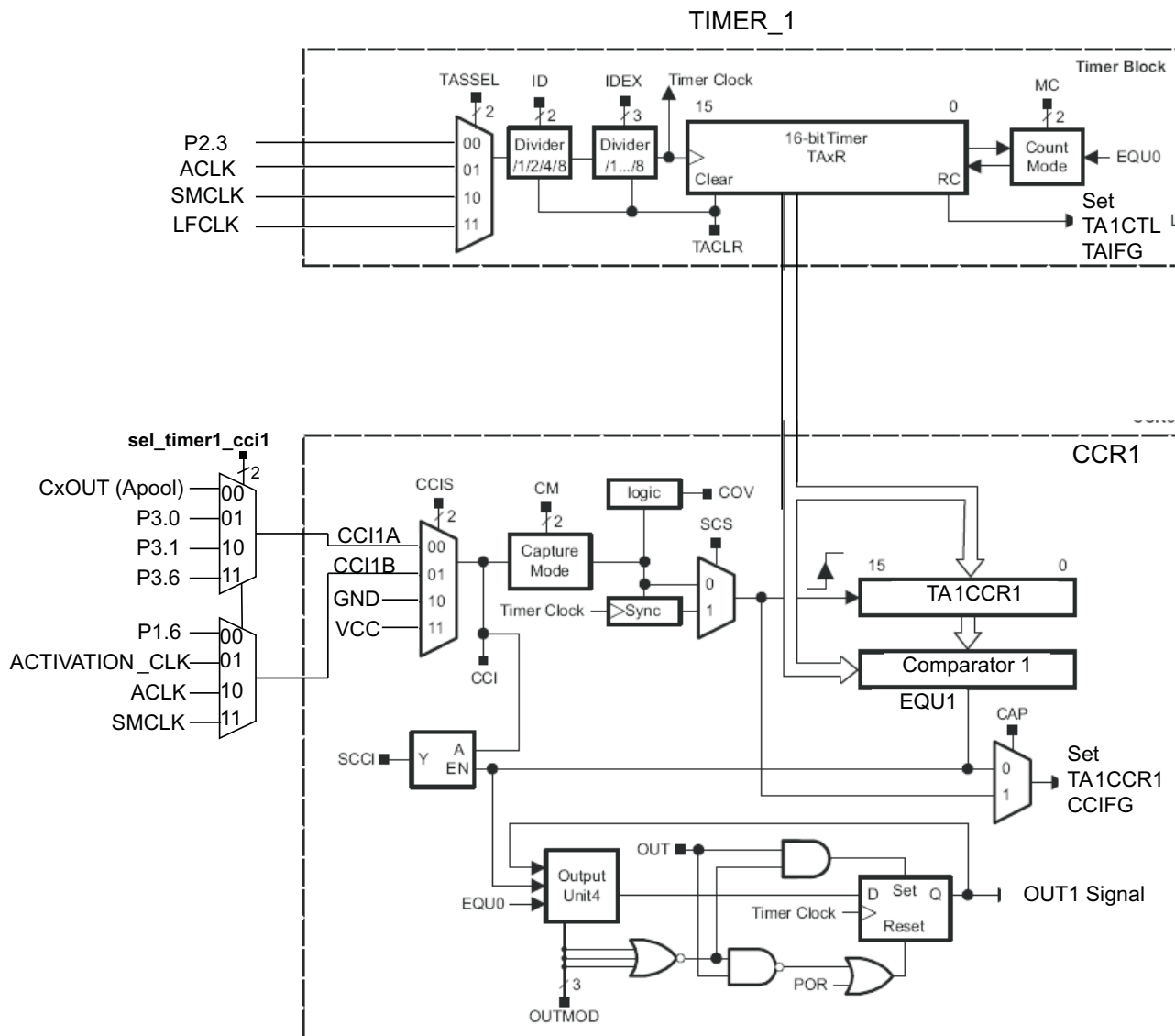
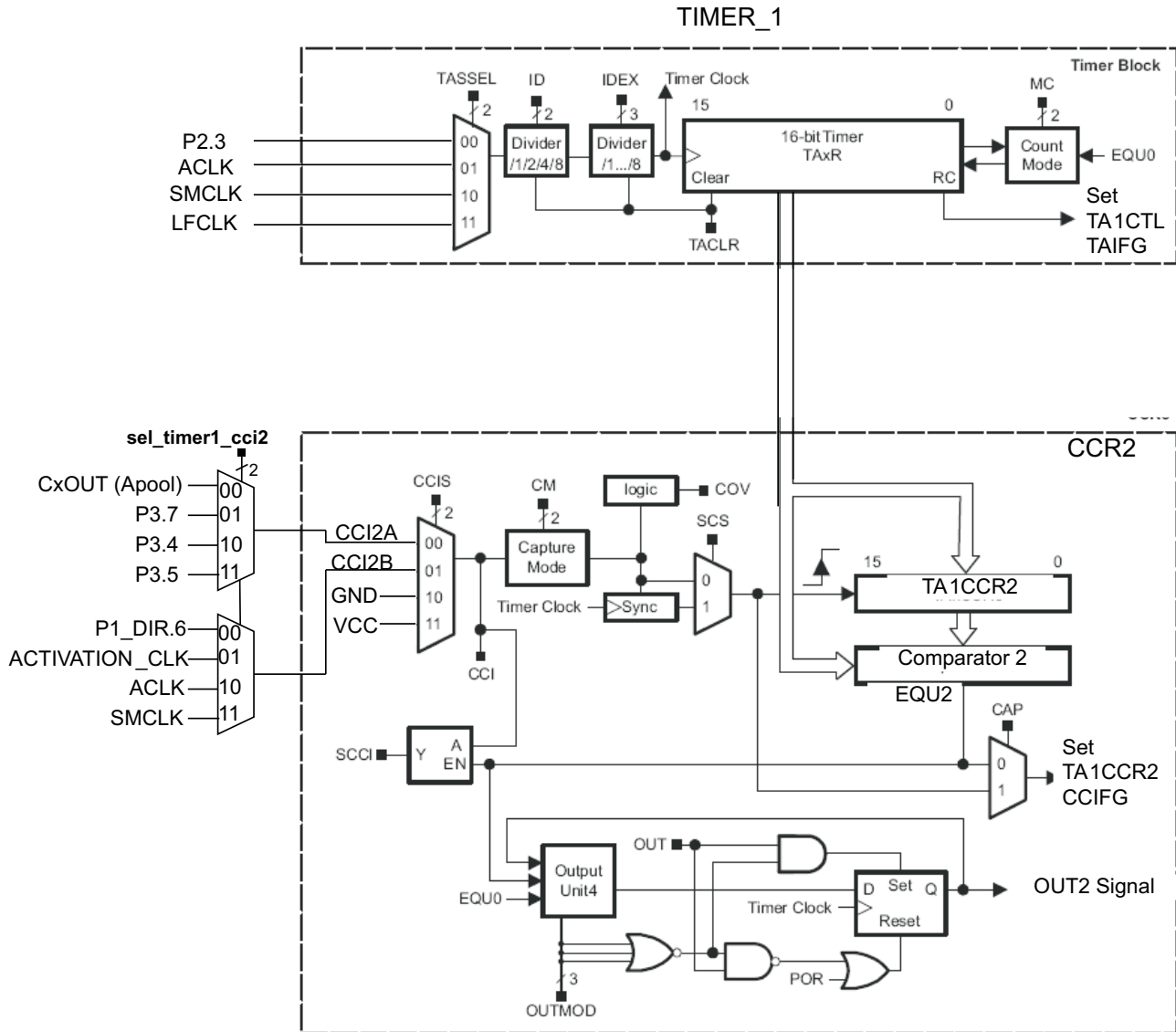


Figure 7. Timer1\_CCR1 Block Diagram



**Figure 8. Timer1\_CCR2 Block Diagram**

**LCD\_E**

The LCD\_E is equivalent to TI LCD-B (MSP430x4 family) driver that generates the segment and common signals required to drive an LCD display. The LCD\_E controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump.

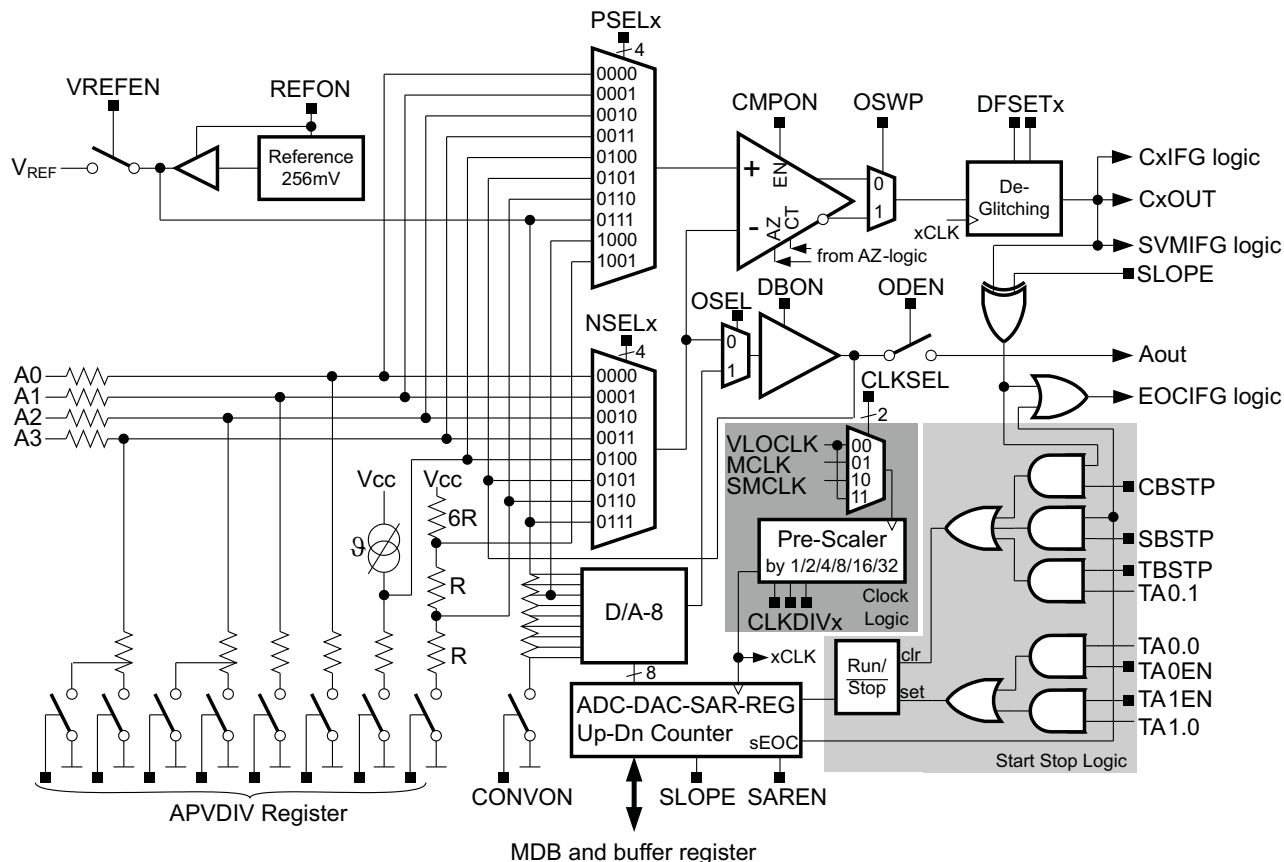
Furthermore it is possible to control the level of the LCD voltage and, thus, contrast by software.

**The LCD\_E operating voltage is minimum 2V**, therefore the user must verify a 2V voltage is available on pin 37 either by activating the CP\_1P8 or using external power supply.

The LCD\_CP is using the CP\_OSC as the reference oscillator for boosting the 2V to LCD operating voltage. The CP\_OSC is working from battery voltage (minimum 1.1V) and is shared with CP\_1P8 which also using it for generating the 2V from the battery voltage internally.

**A-Pool**

The analog functions pool (A-Pool) provides a series of function that can be configured to a Digital to Analog converter (DAC), multi channel Analog to Digital converter (ADC), Supply voltage supervisor SVS and Comparator, input voltage dividers and an internal reference source allow wide range of combined analog functions. For a complete description of A-Pool, see the Analog Pool chapter of the MSP430x09x Family Users Guide (SLAU321)



**Figure 9. Block Diagram of A-Pool**

**Table 10. A-Pool Analog inputs Connection Table**

| A-POOL ANALOG INPUT | PAD  | PSEL | NSEL | A3PSEL | A0_port_sel |
|---------------------|------|------|------|--------|-------------|
| A3a                 | P1.2 | 0011 | 0011 | 0      | X           |
| A3b                 | P1.3 | 0011 | 0011 | 1      | X           |
| A2                  | P1.0 | 0010 | 0010 | X      | X           |
| A1                  | P1.1 | 0001 | 0001 | X      | X           |
| A0a                 | P1.4 | 0000 | 0000 | X      | 0           |
| A0b                 | P3.3 | 0000 | 0000 | X      | 1           |

**Versatile I/O Port P1, P2, P3, P4**

The versatile I/O ports P1, P2, P3 and P4 feature device dependent reset values. The reset values for the AFE4110 devices are shown in below.

**Table 11. Versatile Port Reset Values**

| PORT NUMBER | PxOUT | PxDIR | PxREN | PxSEL0 | PxSEL1 | RESET | Ports ON | COMMENT     | I/O POWER DOMAIN |
|-------------|-------|-------|-------|--------|--------|-------|----------|-------------|------------------|
| P1.0        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P1.0, input | V <sub>DD</sub>  |
| P1.1        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P1.1, input | V <sub>DD</sub>  |
| P1.2        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P1.2, input | V <sub>DD</sub>  |
| P1.3        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P1.3, input | V <sub>DD</sub>  |
| P1.4        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P1.4, input | V <sub>DD</sub>  |
| P1.5        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P1.5, input | V <sub>DD</sub>  |
| P1.6        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P1.6, input | V <sub>DD</sub>  |
| P1.7        | –     | –     | –     | –      | –      | –     | –        | –           |                  |
| P2.0        | 1     | 0     | 1     | 1      | 1      | BOR   | no       | JTAG TCK    | VDDIO            |
| P2.1        | 1     | 0     | 1     | 1      | 1      | BOR   | no       | JTAG TMS    | VDDIO            |
| P2.2        | 1     | 0     | 1     | 1      | 1      | BOR   | no       | JTAG TDI    | VDDIO            |
| P2.3        | 0     | 1     | 0     | 1      | 1      | BOR   | no       | JTAG TDO    | VDDIO            |
| P3.0        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P3.0, input | V <sub>DD</sub>  |
| P3.1        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P3.1, input | V <sub>DD</sub>  |
| P3.2        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P3.2, input | V <sub>DD</sub>  |
| P3.3        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P3.3, input | V <sub>DD</sub>  |
| P3.4        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P3.4, input | V <sub>DD</sub>  |
| P3.5        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P3.5, input | V <sub>DD</sub>  |
| P3.6        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P3.6, input | VDDIO            |
| P3.7        | 0     | 0     | 0     | 0      | 0      | PUC   | yes      | P3.7, input | VDDIO            |
| P4.0        | 0     | 0     | 0     | 0      | 0      | PUC   | Yes      | P4.0, input | VDDIO            |
| P4.1        | 0     | 0     | 0     | 0      | 0      | PUC   | Yes      | P4.1, input | VDDIO            |
| P4.2        | 0     | 0     | 0     | 0      | 0      | PUC   | Yes      | P4.2, input | VDDIO            |
| P4.3        | 0     | 1     | 0     | 0      | 0      | PUC   | yes      | P4.3, input | VDDIO            |



**Table 12. Peripherals**

| MODULE NAME              | REGISTER DESCRIPTION                  | REGISTER  | BASE ADDRESS | OFFSET  |
|--------------------------|---------------------------------------|---|--------------|---------|
| <b>AREGS</b>             | Analog e-fuse                         | ANALOG_FUSETRIM   | 04A0h        | 16h     |
|                          | Analog timer control                  | ANALOG_TIMERCTL   |              | 14h     |
|                          | Analog port control 2                 | ANALOG_PORTCTL2   |              | 12h     |
|                          | Analog port control 1                 | ANALOG_PORTCTL1   |              | 10h     |
|                          | Analog ana control                    | ANALOG_ANACTL   |              | 0Eh     |
|                          | Analog bias current control           | ANALOG_IBIASCTL   |              | 0Ch     |
|                          | Analog LDO control                    | ANALOG_LDOCTL   |              | 0Ah     |
|                          | Analog LDO configuration              | ANALOG_LDOCFG   |              | 08h     |
|                          | Analog LCDP control                   | ANALOG_LCDPCTL  |              | 06h     |
|                          | Analog LCD charge pump control        | ANALOG_LCDPCFG  |              | 04h     |
|                          | Analog charge pump 1.8V control       | ANALOG_CP1P8CTL   |              | 02h     |
|                          | Analog charge pump 1.8V configuration | ANALOG_CP1P8CFG   |              | 00h     |
| <b>Activation</b>        | Activation Sense                      | ACTIVATION_SENSE  | 0480h        | 0Eh     |
|                          | Activation Status                     | ACTIVATION_STATUS   |              | 0Ch     |
|                          | Activation read address               | ACTIVATION_RD_ADDR  |              | 0Ah     |
|                          | Activation strobes                    | ACTIVATION_STROBES  |              | 08h     |
|                          | Activation data out                   | ACTIVATION_DATAOUT  |              | 06h     |
|                          | Activation data in                    | ACTIVATION_DATAIN   |              | 04h     |
|                          | Shelf counter high                    | SHELF_CNT_HI  |              | 02h     |
|                          | Shelf counter low                     | SHELF_CNT_LO  |              | 00h     |
| <b>LCD</b>               | Reserved                              | LCDB1-6<br><br>LCDB1-6<br>LCDBIV<br><br>LCDBCPCTL<br><br>LCDBVCTL<br>LCDBMEMCTL<br>LCDBBLKCTL<br>LCDBCTL1<br>LCDBCTL0 | 0400h        | 46h-5Fh |
|                          | LCD Blinking 1–6 <sup>(1)</sup>       |   |              | 40h-45h |
|                          | Reserved                              |   |              | 26h-3Fh |
|                          | LCD memory 1–6 <sup>(1)</sup>         |   |              | 20h-25h |
|                          | LCD_B interrupt vector                |   |              | 1Eh     |
|                          | Reserved                              |   |              | 14h-1Ch |
|                          | LCD_B charge pump control             |   |              | 12h     |
|                          | Reserved                              |   |              | 0Ah-11h |
|                          | LCD_B voltage control register        |   |              | 08h     |
|                          | LCD_B memory control register         |   |              | 06h     |
|                          | LCD_B blinking control register       |   |              | 04h     |
|                          | LCD B control register 1              |   |              | 02h     |
| LCD B control register 0 | 00h                                   |   |              |         |
| <b>Timer1_A3</b>         | Timer1_A interrupt vector             | TA1IV   | 0380h        | 2Eh     |
|                          | Capture/compare register 2            | TA1CCR2   |              | 16h     |
|                          | Capture/compare register 1            | TA1CCR1   |              | 14h     |
|                          | Capture/compare register 0            | TA1CCR0   |              | 12h     |
|                          | Timer1_A register                     | TA1R  |              | 10h     |
|                          | Capture/compare control 2             | TA1CCTL2  |              | 06h     |
|                          | Capture/compare control 1             | TA1CCTL1  |              | 04h     |
|                          | Capture/compare control 0             | TA1CCTL0  |              | 02h     |
|                          | Timer1_A control                      | TA1CTL  |              | 00h     |

(1) Six 8 bit registers, but the LCD blinking and memory registers can also be accessed as word

**Table 12. Peripherals (continued)**

| MODULE NAME                    | REGISTER DESCRIPTION           | REGISTER               | BASE ADDRESS | OFFSET |
|--------------------------------|--------------------------------|------------------------|--------------|--------|
| <b>Timer0_A3</b>               | Timer0_A interrupt vector      | TA0IV                  | 0340h        | 2Eh    |
|                                | Capture/compare register 2     | TA0CCR2                |              | 16h    |
|                                | Capture/compare register 1     | TA0CCR1                |              | 14h    |
|                                | Capture/compare register 0     | TA0CCR0                |              | 12h    |
|                                | Timer1_A register              | TA0R                   |              | 10h    |
|                                | Capture/compare control 2      | TA0CCTL2               |              | 06h    |
|                                | Capture/compare control 1      | TA0CCTL1               |              | 04h    |
|                                | Capture/compare control 0      | TA0CCTL0               |              | 02h    |
|                                | Timer1_A control               | TA0CTL                 |              | 00h    |
| <b>Port P4</b>                 | Port P4 interrupt Flag         | P4IFG                  | 0220h        | 1Dh    |
|                                | Port P4 interrupt enable       | P4IE                   |              | 1Bh    |
|                                | Port P4 interrupt edge select  | P4IES                  |              | 19h    |
|                                | Port P4 interrupt vector word  | P4IV                   |              | 1Eh    |
|                                | Port P4 selection 1            | P4SEL1                 |              | 0Dh    |
|                                | Port P4 selection 0            | P4SEL0                 |              | 0Bh    |
|                                | Port P4 pullup/pulldown enable | P4REN                  |              | 07h    |
|                                | Port P4 direction              | P4DIR                  |              | 05h    |
|                                | Port P4 outout                 | P4OUT                  |              | 03h    |
|                                | Port P4 input                  | P4IN                   |              | 01h    |
|                                | <b>Port P3</b>                 | Port P3 interrupt Flag |              | P3IFG  |
| Port P3 interrupt enable       |                                | P3IE                   | 1Ah          |        |
| Port P3 interrupt edge select  |                                | P3IES                  | 18h          |        |
| Port P3 interrupt vector word  |                                | P3IV                   | 0Eh          |        |
| Port P3 selection 1            |                                | P3SEL1                 | 0Ch          |        |
| Port P3 selection 0            |                                | P3SEL0                 | 0Ah          |        |
| Port P3 pullup/pulldown enable |                                | P3REN                  | 06h          |        |
| Port P3 direction              |                                | P3DIR                  | 04h          |        |
| Port P3 outout                 |                                | P3OUT                  | 02h          |        |
| Port P3 input                  |                                | P3IN                   | 00h          |        |
| <b>Port P2</b>                 |                                | Port P2 interrupt Flag | P2IFG        | 0200h  |
|                                | Port P2 interrupt enable       | P2IE                   | 1Bh          |        |
|                                | Port P2 interrupt edge select  | P2IES                  | 19h          |        |
|                                | Port P2 interrupt vector word  | P2IV                   | 0Eh          |        |
|                                | Port P2 selection 1            | P2SEL1                 | 0Dh          |        |
|                                | Port P2 selection 0            | P2SEL0                 | 0Bh          |        |
|                                | Port P2 pullup/pulldown enable | P2REN                  | 07h          |        |
|                                | Port P2 direction              | P2DIR                  | 05h          |        |
|                                | Port P2 outout                 | P2OUT                  | 03h          |        |
|                                | Port P2 input                  | P2IN                   | 01h          |        |
|                                | <b>Port P1</b>                 | Port P1 interrupt Flag | P1IFG        |        |
| Port P1 interrupt enable       |                                | P1IE                   | 1Ah          |        |
| Port P1 interrupt edge select  |                                | P1IES                  | 18h          |        |
| Port P1 interrupt vector word  |                                | P1IV                   | 0Eh          |        |
| Port P1 selection 1            |                                | P1SEL1                 | 0Ch          |        |
| Port P1 selection 0            |                                | P1SEL0                 | 0Ah          |        |
| Port P1 pullup/pulldown enable |                                | P1REN                  | 06h          |        |
| Port P1 direction              |                                | P1DIR                  | 04h          |        |

**Table 12. Peripherals (continued)**

| MODULE NAME              | REGISTER DESCRIPTION                             | REGISTER | BASE ADDRESS | OFFSET |
|--------------------------|--|----------|--------------|--------|
|                          | Port P1 outout                                   | P1OUT    |              | 02h    |
|                          | Port P1 input                                    | P1IN     |              | 00h    |
| <b>A-POOL</b>            | Analog pool interrupt vector register            | APIV     | 01A0h        | 1Eh    |
|                          | Analog pool interrupt enable register register   | APIE     |              | 1Ch    |
|                          | Analog pool interrupt flag register              | APIFG    |              | 1Ah    |
|                          | Analog pool fractional value buffer              | APFRACTB |              | 16h    |
|                          | Analog pool fractional value register            | APFRACT  |              | 14h    |
|                          | Analog pool integer value buffer                 | APINTB   |              | 12h    |
|                          | Analog pool integer value register               | APINT    |              | 10h    |
|                          | Analog pool voltage divider register             | APVDIV   |              | 06h    |
|                          | Analog pool operation mode register              | APOMR    |              | 04h    |
|                          | Analog pool control register                     | APCTL    |              | 02h    |
|                          | Analog pool configuration register               | APCNF    |              | 00h    |
| <b>CSYS</b>              | Reset vector generator                           | SYRSTIV  | 0180h        | 1Eh    |
|                          | System NMI vector generator                      | SYSSNIV  |              | 1Ch    |
|                          | User NMI vector generator                        | YSUNIV   |              | 1Ah    |
|                          | Bus error vector generator                       | YSBERRIV |              | 18h    |
|                          | System Configuration register                    | SYSCNF   |              | 10h    |
|                          | JTAG mailbox output register #1                  | SYSJMBO1 |              | 0Eh    |
|                          | JTAG mailbox output register #0                  | SYSJMBO0 |              | 0Ch    |
|                          | JTAG mailbox input register #1                   | SYSJMBI1 |              | 0Ah    |
|                          | JTAG mailbox input register #0                   | SYSJMBI0 |              | 08h    |
|                          | JTAG mailbox control register                    | SYSJMBC  |              | 06h    |
|                          | System control register                          | SYCTL    |              | 00h    |
| <b>CCS</b>               | CCS control 8 register                           | CCSCTL8  | 0160h        | 10h    |
|                          | CCS control 7 register                           | CCSCTL7  |              | 0Eh    |
|                          | CCS control 6 register                           | CCSCTL6  |              | 0Ch    |
|                          | CCS control 5 register                           | CCSCTL5  |              | 0Ah    |
|                          | CCS control 4 register                           | CCSCTL4  |              | 08h    |
|                          | CCS control 2 register                           | CCSCTL2  |              | 04h    |
|                          | CCS control 1 register                           | CCSCTL1  |              | 02h    |
|                          | CCS control 0 register                           | CCSCTL0  |              | 00h    |
| <b>WDT_A</b>             | WDT_A Watchdog timer control                     | WDTCTL   | 0150h        | 0Ch    |
| <b>PMM</b>               | PMM PMM control 0                                | PMMCTL0  | 0120h        | 00h    |
| <b>ET-WRAPPER</b>        | ET-Wrapper ET Key and select                     | ETKEYSEL | 0110h        | 00h    |
| <b>Special Functions</b> | Special Functions SFR Reset pin control register | SFRRPCR  | 0100h        | 04h    |
|                          | SFR interrupt flag register                      | SFRIFG1  |              | 02h    |
|                          | SFR interrupt enable register                    | SFRIE1   |              | 00h    |

**Legend**

- rw: Bit can be read and written.  
**rw-0,1**: Bit can be read and written. It is reset or set by PUC.<sup>(1)</sup>  
**rw-(0,1)**: Bit can be read and written. It is reset or set by POR.<sup>(2)</sup>  
**rw-[0,1]**: Bit can be read and written. It is reset or set by BOR.<sup>(3)</sup>  
– bit is not present in device

(1) PUC is for "normal" registers which should be reset at all time

(2) POR is used for registers, which should not be reset by a WDT event (like status information)

(3) BOR is used for registers, which are configured during boot code execution and should not be reset during normal reset events

## Analog Control Registers

### ANALOG\_CP1P8CFG: Analog charge pump 1.8V configuration

|                        |      |                         |                  |                |                       |                 |                  |
|------------------------|------|-------------------------|------------------|----------------|-----------------------|-----------------|------------------|
| 15                     | 14   | 13                      | 12               | 11             | 10                    | 9               | 8                |
| –                      | –    | –                       | <b>1p8_valid</b> | <b>clk_sel</b> | <b>force_clk</b>      | <b>mode_sel</b> | <b>cp_1p8_pd</b> |
| r-0                    | r-0  | r-0                     | r-0              | rw-0           | rw-0                  | rw-0            | rw-1             |
| 7                      | 6    | 5                       | 4                | 3              | 2                     | 1               | 0                |
| <b>cp_1p8_hyst_set</b> |      | <b>cp_1p8_out_level</b> |                  |                | <b>cp_1p8_clk_div</b> |                 |                  |
| rw-0                   | rw-0 | rw-0                    | rw-0             | rw-0           | rw-0                  | rw-0            | rw-0             |

|                            |          |  |
|----------------------------|----------|--|
| <b>cp_1p8_clk_div</b>      | Bits 2-0 | Select the clock divider (see table below)   |
| <b>cp_1p8_out_level</b>    | Bits 5-3 | Set the CP valid threshold voltage (see table below)   |
| <b>cp_1p8_hyst_set</b>     | Bits 7-6 | Set the comparator hysteresis (inside the CP loop) – 000 means close hysteresis, and 111 means wide hysteresis. When using fast clock (high current) the user must use close hysteresis 000. |
| <b>cp_1p8_pd</b>           | Bit 8    | Powers Down the charge pump circuitries  |
| <b>cp_1p8_clk_mode_sel</b> | Bit 9    | Test mode of the CP loop, break the loop to control by the signal fram_force_clk   |
| <b>cp_1p8_force_clk</b>    | Bit 10   | Force a continuous clock to the Charge Pump (in test mode)   |
| <b>cp_1p8_clk_sel</b>      | Bit 11   | Select which clock to use (internal or external)   |
| <b>cp_1p8_valid</b>        | Bit 12   | Valid 1.8v indication output   |

### ANALOG\_CP1P8CTL: Analog charge pump 1.8V control

|                           |      |                         |      |                   |              |                 |                   |
|---------------------------|------|-------------------------|------|-------------------|--------------|-----------------|-------------------|
| 15                        | 14   | 13                      | 12   | 11                | 10           | 9               | 8                 |
| <b>Reserved</b>           |      |                         |      |                   |              |                 |                   |
| rw-0                      | rw-0 | rw-0                    | rw-0 | rw-0              | rw-0         | rw-0            | rw-0              |
| 7                         | 6    | 5                       | 4    | 3                 | 2            | 1               | 0                 |
| <b>cp_1p8_valid_level</b> |      | <b>clk_refresh_freq</b> |      | <b>ext_cap_en</b> | <b>clamp</b> | <b>clamp_en</b> | <b>quiet_mode</b> |
| rw-0                      | rw-0 | rw-0                    | rw-0 | rw-0              | rw-0         | rw-1            | rw-0              |

|                                  |             |  |
|----------------------------------|-------------|--|
| <b>cp_1p8_quiet_mode</b>         | Bit 0       | Inhibits charge pump clocking  |
| <b>cp_1p8_force_out_clamp_en</b> | Bit 1       | Controls the output clamp switch to AVDD_BAT (0 - clamp according to control; 1 - clamp according to PD control) |
| <b>cp_1p8_force_out_clamp</b>    | Bit 2       | Force the output clamp to AVDD_BAT   |
| <b>cp_1p8_ext_cap_en</b>         | Bit 3       | Set to high when high current is required  |
| <b>cp_1p8_clk_refresh_freq</b>   | Bits 4-5    | Set the frequency for refreshing the rdiv cap (see table below)  |
| <b>cp_1p8_valid_level</b>        | Bits 6-7    | Set the CP valid threshold voltage (see table below)   |
| Reserved                         | Bits 8 - 15 |  |

| cp_1p8_out_level |         | cp_1p8_clk_div table: |           |
|------------------|---------|-----------------------|-----------|
| Setting          | Freq    | Setting               | Freq      |
| 000              | 2.075 V | 000                   | FS (4MHz) |
| 001              | 2.05 V  | 001                   | 001 FS/2  |
| 010              | 2.025 V | 010                   | FS/4      |
| 011              | 2 V     | 011                   | FS/8      |
| 100              | 1.975 V | 100                   | FS/16     |
| 101              | 1.95 V  | 101                   | FS/32     |
| 110              | 1.925 V | 110                   | FS/64     |
| 111              | 1.9 V   | 111                   | FS/128    |

| cp_1p8_clk_refresh_freq table: |           |  | cp_1p8_clk_valid_level table: |        |
|--------------------------------|-----------|--|-------------------------------|--------|
| Setting                        | Freq      |  | Setting                       | Freq   |
| 00                             | 156.25 Hz |  | 00                            | 1.75 V |
| 01                             | 312.5 Hz  |  | 01                            | 1.8 V  |
| 10                             | 312.5 Hz  |  | 10                            | 1.85 V |
| 11                             | 625 Hz    |  | 11                            | 1.9 V  |

The clock output is a single 50  $\mu$ s pulse

### ANALOG\_LCDPCFG: Analog LCD charge pump controlR

|     |     |     |                  |     |     |     |                |
|-----|-----|-----|------------------|-----|-----|-----|----------------|
| 15  | 14  | 13  | 12               | 11  | 10  | 9   | 8              |
| –   | –   | –   | –                | –   | –   | –   | –              |
| r-0 | r-0 | r-0 | r-0              | r-0 | r-0 | r-0 | r-0            |
| 7   | 6   | 5   | 4                | 3   | 2   | 1   | 0              |
| –   | –   | –   | <b>Force_clk</b> | –   | –   | –   | <b>clk_sel</b> |
| r-0 | r-0 | r-0 | rw-0             | r-0 | r-0 | r-0 | rw-0           |

lcd\_cp\_clk\_sel Bit 0 NC (Not connected)

lcd\_cp\_force\_clk Bit 4 NC

### ANALOG\_LCDPCTL: Analog LCDP control

|                 |                 |                |                |                |                |                |                |
|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| 15              | 14              | 13             | 12             | 11             | 10             | 9              | 8              |
| <b>seg11_en</b> | <b>seg10_en</b> | <b>seg9_en</b> | <b>seg8_en</b> | <b>seg7_en</b> | <b>seg6_en</b> | <b>seg5_en</b> | <b>seg4_en</b> |
| rw-1            | rw-1            | rw-1           | rw-1           | rw-1           | rw-1           | rw-1           | rw-1           |
| 7               | 6               | 5              | 4              | 3              | 2              | 1              | 0              |
| <b>seg3_en</b>  | <b>seg2_en</b>  | <b>seg1_en</b> | <b>seg0_en</b> | <b>com3_en</b> | <b>com2_en</b> | <b>com1_en</b> | <b>com0_en</b> |
| rw-1            | rw-1            | rw-1           | rw-1           | rw-1           | rw-1           | rw-1           | rw-1           |

|                 |        |  |
|-----------------|--------|--|
| <b>com0_en</b>  | Bit 0  | Enable LCD pin common 0. "1" – enable, "0" – disable   |
| <b>com1_en</b>  | Bit 1  | Enable LCD pin common 1. "1" – enable, "0" – disable   |
| <b>com2_en</b>  | Bit 2  | Enable LCD pin common 2. "1" – enable, "0" – disable   |
| <b>com3_en</b>  | Bit 3  | Enable LCD pin common 3. "1" – enable, "0" – disable   |
| <b>seg0_en</b>  | Bit 4  | Enable LCD pin segment 0. "1" – enable, "0" – disable  |
| <b>seg1_en</b>  | Bit 5  | Enable LCD pin segment 1. "1" – enable, "0" – disable  |
| <b>seg2_en</b>  | Bit 6  | Enable LCD pin segment 2. "1" – enable, "0" – disable  |
| <b>seg3_en</b>  | Bit 7  | Enable LCD pin segment 3. "1" – enable, "0" – disable  |
| <b>seg4_en</b>  | Bit 8  | Enable LCD pin segment 4. "1" – enable, "0" – disable  |
| <b>seg5_en</b>  | Bit 9  | Enable LCD pin segment 5. "1" – enable, "0" – disable  |
| <b>seg6_en</b>  | Bit 10 | Enable LCD pin segment 6. "1" – enable, "0" – disable  |
| <b>seg7_en</b>  | Bit 11 | Enable LCD pin segment 7. "1" – enable, "0" – disable  |
| <b>seg8_en</b>  | Bit 12 | Enable LCD pin segment 8. "1" – enable, "0" – disable  |
| <b>seg9_en</b>  | Bit 13 | Enable LCD pin segment 9. "1" – enable, "0" – disable  |
| <b>seg10_en</b> | Bit 14 | Enable LCD pin segment 10. "1" – enable, "0" – disable |
| <b>seg11_en</b> | Bit 15 | Enable LCD pin segment 11. "1" – enable, "0" – disable |

To enable the LCD both the relevant ANALOG\_LCDPCTL bit should be set to 1 and the LCDON bit in LCD register LCDCTL0 should be set to 1.

# AFE4110

SLLSE48 – JANUARY 2012

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## ANALOG\_LDOCFG: Analog LDO configuration

|                    |                   |                    |               |     |                      |                       |      |
|--------------------|-------------------|--------------------|---------------|-----|----------------------|-----------------------|------|
| 15                 | 14                | 13                 | 12            | 11  | 10                   | 9                     | 8    |
| –                  | –                 | <b>ldo_out_mux</b> |               | –   | –                    | <b>cap_sw_general</b> |      |
| r-0                | r-0               | rw-0               | rw-0          | r-0 | r-0                  | rw-0                  | rw-0 |
| 7                  | 6                 | 5                  | 4             | 3   | 2                    | 1                     | 0    |
| <b>high_cap_sw</b> | <b>low_cap_sw</b> | <b>ldo_bypass</b>  | <b>ldo_pd</b> | –   | <b>ldo_trim_bits</b> |                       |      |
| rw-0               | rw-0              | rw-0               | rw-1          | r-0 | rw-0                 | rw-0                  | rw-0 |

|                       |           |   |
|-----------------------|-----------|---|
| <b>ldo_trim_bits</b>  | Bits 0-2  | LDO voltage trimming (see table below)                                      |
| <b>ldo_pd</b>         | Bit 4     | "1" LDO Shut down. Vout=open  |
| <b>ldo_bypass</b>     | Bits 5    | "1" Bypass the LDO, shorts LDO Vout to VDD                                  |
| <b>low_cap_sw</b>     | Bit 6     | "1" Connect the low calibration capacitor (20pF)                            |
| <b>high_cap_sw</b>    | Bit 7     | "1" Connect the high calibration capacitor (40pF)                           |
| <b>cap_sw_general</b> | Bit 8-9   | NC  |
| <b>ldo_out_mux</b>    | Bit 12-13 | "00" set the LDO output switch to "off". "11" set LDO output switch to "on" |

| ldo_trim_bits table: |         |
|----------------------|---------|
| Setting              | Vout[V] |
| 000                  | 1.045   |
| 001                  | 10.72   |
| 010                  | 1.1     |
| 011                  | 1.125   |
| 100                  | 0.96    |
| 101                  | 0.98    |
| 110                  | 1       |
| 111                  | 1.02    |

## ANALOG\_LDOCTL Analog LDO control

|                        |      |                    |      |                   |      |      |      |
|------------------------|------|--------------------|------|-------------------|------|------|------|
| 15                     | 14   | 13                 | 12   | 11                | 10   | 9    | 8    |
| <b>ldo_ctl (cont.)</b> |      |                    |      |                   |      |      |      |
| rw-0                   | rw-0 | rw-0               | rw-0 | rw-0              | rw-0 | rw-0 | rw-0 |
| 7                      | 6    | 5                  | 4    | 3                 | 2    | 1    | 0    |
| <b>ldo_ctl</b>         |      | <b>a0_port_sel</b> |      | <b>LDO_IO_sel</b> |      |      |      |
| rw-0                   | rw-0 | rw-0               | rw-1 | r-0               | rw-0 | rw-0 | rw-0 |

|                    |           |  |
|--------------------|-----------|--|
| <b>LDO_IO_sel</b>  | Bit 0-3   | Used to mux the LDO to IOs in the following order:<br><0> – port 1.0;<br><1> – port 1.1;<br><2> – port 1.4;<br><3> – port 3.3; |
| <b>a0_port_sel</b> | Bit 4     | Select which IO goes to A0 input of the A-Pool – ,0. selects port 1.4  |
| <b>ldo_ctl</b>     | Bits 5-15 | NC   |

**ANALOG\_IBIASCTL: Analog bias current control**

|                 |      |               |              |                |      |                 |      |
|-----------------|------|---------------|--------------|----------------|------|-----------------|------|
| 15              | 14   | 13            | 12           | 11             | 10   | 9               | 8    |
| spare           |      | lf_force_mode | hfos_current | osc_6m current |      | ctl_ref_current |      |
| rw-0            | rw-0 | rw-0          | rw-1         | rw-0           | rw-0 | rw-0            | rw-0 |
| 7               | 6    | 5             | 4            | 3              | 2    | 1               | 0    |
| <b>ibias_pd</b> |      |               |              |                |      |                 |      |
| rw-0            | rw-0 | rw-0          | rw-0         | rw-0           | rw-0 | rw-0            | rw-0 |

|                        |            |  |
|------------------------|------------|--|
| <b>ibias_pd</b>        | Bits 0-7   | Powering down the bias currents Not used   |
| <b>ctl_ref_current</b> | Bits 8-9   | Select main reference current:<br>00 – 10nA (Default)<br>01 – 6nA<br>10 – 12nA<br>11 – 8nA                   |
| <b>osc_6m current</b>  | Bits 10-11 | Controls the HF_OSC current setting:<br>00 – 1 $\mu$ A<br>01 – 3 $\mu$ A<br>10 – 2 $\mu$ A<br>11 – 4 $\mu$ A |
| <b>hfos_current</b>    | Bit 12     | 1 – Setting the HF_OSC to low frequency/low current mode (1MHz/10 $\mu$ A)                                   |
| <b>lf_mode_force</b>   | Bit 13     | 0 – lf_mode is forced on hf_osc ;<br>1 – lf_mode is working only of I_trim is 00                             |
| <b>spare</b>           | Bits 14-15 | Not Used   |

**HF\_OSC LF Mode - Typical frequency after HF-OSC calibrated to 4.4MHz**

| hfos_current<12> | lf_mode_force<13> | osc_6m current<11,10> | HF-OSC Frq [MHz] |
|------------------|-------------------|-----------------------|------------------|
| 0                | x                 | 00                    | 1.87             |
|                  |                   | 01                    | 4.44             |
|                  |                   | 10                    | 3.27             |
|                  |                   | 11                    | 5.4              |
| 1                | 0                 | 00                    | 1                |
|                  |                   | 01                    |                  |
|                  |                   | 10                    |                  |
|                  |                   | 11                    |                  |
| 1                | 1                 | 00                    | 1                |
|                  |                   | 01                    | 3.9              |
|                  |                   | 10                    | 2.6              |
|                  |                   | 11                    | 5                |

# AFE4110

SLLSE48 –JANUARY 2012

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## ANALOG\_ANACTL: Analog ana control

|                           |      |      |      |                              |      |                    |      |
|---------------------------|------|------|------|------------------------------|------|--------------------|------|
| 15                        | 14   | 13   | 12   | 11                           | 10   | 9                  | 8    |
| <b>ana_ctl (not used)</b> |      |      |      | <b>lpm5_en_lcd_ana_shell</b> |      | <b>Cp_osc_trim</b> |      |
| rw-0                      | rw-0 | rw-0 | rw-0 | rw-0                         | rw-1 | rw-0               | rw-0 |
| 7                         | 6    | 5    | 4    | 3                            | 2    | 1                  | 0    |
| <b>Reserved</b>           |      |      |      |                              |      |                    |      |
| rw-0                      | rw-0 | rw-0 | rw-0 | rw-0                         | rw-0 | rw-0               | rw-0 |

|                     |            |   |
|---------------------|------------|---|
| Reserved            | Bits 0-7   |   |
| Ana_ctl_cp_osc_trim | Bits 8-9   | Course trimming of the 2 charge pumps oscillator (current trimming) |
| lpm5_lcd_ana_shell  | Bit 10     | "1" powers down (~40nA) the max_detect block inside the LCD Block   |
| ana_ctl             | Bits 11-15 | Not used  |

## ANALOG\_PORTCTL1: Analog Analog port control 1

|                    |     |                    |                    |                    |                    |                    |                    |
|--------------------|-----|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| 15                 | 14  | 13                 | 12                 | 11                 | 10                 | 9                  | 8                  |
| <b>bp_dir_sync</b> |     | <b>irq_on_p3_7</b> | <b>irq_on_p3_6</b> | <b>irq_on_p3_5</b> | <b>irq_on_p3_4</b> | <b>irq_on_p3_3</b> | <b>irq_on_p3_2</b> |
| rw-0               | r-0 | rw-0               | rw-0               | rw-0               | rw-0               | rw-0               | rw-0               |
| 7                  | 6   | 5                  | 4                  | 3                  | 2                  | 1                  | 0                  |
|                    |     | <b>sel_port3_7</b> |                    | –                  | –                  | <b>sel_port3_6</b> |                    |
| r-0                | r-0 | rw-0               | rw-0               | r-0                | r-0                | rw-0               | rw-0               |

## sel\_port3\_6, sel\_port3\_7: PORT3.6 and PORT3.7 Input multiplexer control

| sel_port3_6     | Bits 1,0      | 0,0   | 0,1              | 1,0        | 1,1                 |
|-----------------|---------------|---|------------------|------------|---------------------|
|                 | P3SEL1/0 = 01 | TA0.0   | TA0.1            | TA0.2      | TA1.1               |
|                 | P3SEL1/0 = 10 | NEG(TA0.0)  | NEG(TA0.1)       | NEG(TA0.2) | NEG(TA1.1)          |
|                 | P3SEL1/0 = 11 | BROWNOUT  | ACTIVATION_SENSE | LFCLK      | CP_1P8_COMP         |
| sel_port3_7     | Bits 5,4      | 0,0   | 0,1              | 1,0        | 1,1                 |
|                 | P3SEL1/0 = 01 | TA0.0   | TA0.1            | TA0.2      | LCD_COMP            |
|                 | P3SEL1/0 = 10 | NEG(TA0.0)  | NEG(TA0.1)       | NEG(TA0.2) | NEG(LCD_COMP)       |
|                 | P3SEL1/0 = 11 | LCD_CP_CLK  | LCD_FCLK         | HFCLK      | ACTIVATION_OSC_1KHZ |
| sel_irq_on_p3_2 | Bit 8         | force '0' when test_atpg_en_i = '1'   |                  |            |                     |
| sel_irq_on_p3_3 | Bit 9         |   |                  |            |                     |
| sel_irq_on_p3_4 | Bit 10        |   |                  |            |                     |
| sel_irq_on_p3_5 | Bit 11        |   |                  |            |                     |
| sel_irq_on_p3_6 | Bit 12        |   |                  |            |                     |
| sel_irq_on_p3_7 | Bit 13        |   |                  |            |                     |
| bypass_dir_sync | Bit 15        | "1" Enable Portx.y direct DIR signal connection to TiMERx CCx (No Dithering). "0" Enable Portx.y DIR signal (sync to LFCLK) connection to TiMERx CCx .Dithering enabled when HF-CLK or EXCLK selected as Timer Clock source. <sup>(1)</sup> |                  |            |                     |

(1) force '1' when test\_atpg\_en\_i = '1'



**ANALOG\_PORTCTL2: Analog Analog port control 2**

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| 15           | 14           | 13           | 12           | 11           | 10           | 9            | 8            |
| –            | –            | –            | –            | –            | –            | –            | –            |
| r-0          | r-0          | r-0          | r-0          | r-0          | r-0          | r-0          | r-0          |
| 7            | 6            | 5            | 4            | 3            | 2            | 1            | 0            |
| <b>dp1_6</b> | <b>dp1_5</b> | <b>dp3_5</b> | <b>dp3_4</b> | <b>dp3_3</b> | <b>dp3_2</b> | <b>dp3_1</b> | <b>dp3_0</b> |
| rw-0         | rw-0         | rw-0         | rw-0         | rw-0         | rw-0         | rw-0         | rw-0         |

|                     |       |  |
|---------------------|-------|--|
| <b>disable_p3_0</b> | Bit 0 | "1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage <sup>(1)</sup> |
| <b>disable_p3_1</b> | Bit 1 | "1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage <sup>(1)</sup> |
| <b>disable_p3_2</b> | Bit 2 | "1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage <sup>(1)</sup> |
| <b>disable_p3_3</b> | Bit 3 | "1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage <sup>(1)</sup> |
| <b>disable_p3_4</b> | Bit 4 | "1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage <sup>(1)</sup> |
| <b>disable_p3_5</b> | Bit 5 | "1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage <sup>(1)</sup> |
| <b>disable_p1_5</b> | Bit 6 | "1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage <sup>(1)</sup> |
| <b>disable_p1_6</b> | Bit 7 | "1" disables input driver. Use to enable connection analog voltage input w/o feed through current at PORTx.y input driver stage <sup>(1)</sup> |

(1) force '0' when test\_atpg\_en\_i = '1'

**ANALOG\_TIMERCTL: Analog timer CCx input mux control**

|     |     |                        |      |     |     |                        |      |
|-----|-----|------------------------|------|-----|-----|------------------------|------|
| 15  | 14  | 13                     | 12   | 11  | 10  | 9                      | 8    |
| –   | –   | <b>sel_timer1_cci2</b> | –    | –   | –   | <b>sel_timer1_cci1</b> | –    |
| r-0 | r-0 | rw-0                   | rw-0 | r-0 | r-0 | rw-0                   | rw-0 |
| 7   | 6   | 5                      | 4    | 3   | 2   | 1                      | 0    |
| –   | –   | <b>sel_timer0_cci2</b> | –    | –   | –   | <b>sel_timer0_cci1</b> | –    |
| r-0 | r-0 | rw-0                   | rw-0 | r-0 | r-0 | rw-0                   | rw-0 |

**sel\_port3\_6, sel\_port3\_7: PORT3.6 and PORT3.7 Input multiplexer control**

| <b>sel_timer0_cci1</b> | <b>Bits 1,0</b>           | <b>0,0</b>       | <b>0,1</b>          | <b>1,0</b>   | <b>1,1</b>          |
|------------------------|---------------------------|------------------|---------------------|--------------|---------------------|
|                        | Timer0 CCI1A Input Select | CxOUT from APOOL | Port P1.1           | Port P1.2    | Port P1.3           |
|                        | Timer0 CCI1B Input Select | Port P1.0        | Port P1.4           | Port P1.5    | ACTIVATION_OSC_1KHZ |
| <b>sel_timer0_cci2</b> | <b>Bits 5,4</b>           | <b>0,0</b>       | <b>0,1</b>          | <b>1,0</b>   | <b>1,1</b>          |
|                        | Timer0 CCI2A Input Select | CxOUT from APOOL | Port P1.1DIR        | Port P1.2DIR | Port P1.3DIR        |
|                        | Timer0 CCI2B Input Select | Port P1.0DIR     | Port P1.4DIR        | Port P1.5DIR | SMCLK               |
| <b>sel_timer1_cci1</b> | <b>Bits 9,8</b>           | <b>0,0</b>       | <b>0,1</b>          | <b>1,0</b>   | <b>1,1</b>          |
|                        | Timer1 CCI1A Input Select | CxOUT from APOOL | Port P3.0           | Port P3.1    | Port P3.6           |
|                        | Timer1 CCI1B Input Select | Port P1.6        | ACTIVATION_OSC_1KHZ | ACLK         | SMCLK               |
| <b>sel_timer1_cci2</b> | <b>Bits 13,12</b>         | <b>0,0</b>       | <b>0,1</b>          | <b>1,0</b>   | <b>1,1</b>          |
|                        | Timer1 CCI2A Input Select | CxOUT from APOOL | Port P3.7           | Port P3.4    | Port P3.5           |
|                        | Timer1 CCI2B Input Select | Port P1.6DIR     | ACTIVATION_OSC_1KHZ | ACLK         | SMCLK               |

**ANALOG\_FUSETRIM: Analog e-fuse**

|                 |      |      |                         |      |                    |      |      |
|-----------------|------|------|-------------------------|------|--------------------|------|------|
| 15              | 14   | 13   | 12                      | 11   | 10                 | 9    | 8    |
| –               | –    | –    | <b>cal-fact (cont.)</b> |      |                    |      |      |
| r-0             | r-0  | r-0  | r-f*                    | r-f* | r-f*               | r-f* | r-f* |
| 7               | 6    | 5    | 4                       | 3    | 2                  | 1    | 0    |
| <b>cal-fact</b> |      |      |                         |      | <b>HF-Osc_trim</b> |      |      |
| r-f*            | r-f* | r-f* | r-f*                    | r-f* | r-f*               | r-f* | r-f* |

- HF-Osc\_trim** Bits 2-0 HF-Oscillator trimming. Bits 7-9 of effuse module.
- cal\_fact** Bits 12-3 Discharge calibration factor. Bits 10-19 of e-fuse module.
- Bits 6-0 of e-fuse module can be read via bits 0-6 of APOOL APTRIM register.
  - Some e-fuse bits can also be read via top level register ETTOPCTL0
  - This is a read only register.

**Additional LCD Registers**

LCD registers are described in the LCD\_B chapter of the CC430 Family Users Guide (slau259b). The only exceptions:

1. Bit 15 of register LCDBCPCCTL (LCDPCCLKEXT bit ) has a new functionality as described below.
2. Bit 10 of register ANALOG\_ANACTL (lpm5\_lcd\_ana\_shell bit) has a new functionality as described below.

**1. LCDBCPCCTL, LCD\_B Charge Pump Control Register**

|                    |        |  |  |
|--------------------|--------|--|--|
| <b>LCDCPCLKEXT</b> | Bit 15 | Selects between internal and external clock source for the LCD Charge Pump | '0' – internal clock source<br>'1' – external clock source |
|--------------------|--------|--|--|

Default value of this bit is rw-0

**2. ANALOG\_ANACTL**

|                           |        |   |
|---------------------------|--------|---|
| <b>lpm5_lcd_ana_shell</b> | Bit 10 | "1" powers down (~40nA) the max_detect block inside the LCD Block |
|---------------------------|--------|---|

Default value of this bit is rw-1

**Additional Timer Registers**

Timer registers are described in Timer\_A chapter of the MSP430x09x Family Users Guide ([SLAU321](#)).

**Additional Ports Registers**

Port registers are described in Versatile I/O Port chapter of the MSP430x09x Family Users Guide ([SLAU321](#))

**Additional APOOL Registers**

Analog Functions Pool Module chapter of the MSP430x09x Family Users Guide ([SLAU321](#)).

**Additional CSYS Registers**

Compact System Control Module chapter of the MSP430x09x Family Users Guide ([SLAU321](#)). The only exceptions are:

**MEMSWP BIT 11**

- 1 - Selects the EMU/Loader memory configuration
- 0 - Selects the custom ROM memory configuration

## CCS Registers

Compact Clock System chapter of the MSP430x09x Family Users Guide ([SLAU321](#)). The only exception is different functionality of register CCSCCTL6 as described below:

### CCSCCTL6: CCS control 6

|     |       |     |          |        |      |           |           |
|-----|-------|-----|----------|--------|------|-----------|-----------|
| 15  | 14    | 13  | 12       | 11     | 10   | 9         | 8         |
| –   | –     | –   | Reserved |        |      |           | xt_off    |
| r-0 | r-0   | r-0 | rw-0     | rw-0   | rw-0 | rw-0      | rw-1      |
| 7   | 6     | 5   | 4        | 3      | 2    | 1         | 0         |
| –   | xt_sw |     |          | xt_byp |      | xt_clken2 | xt_clken1 |
| r-0 | rw-1  | r-0 | rw-1     | rw-1   | rw-1 | r-0       | r-0       |

|                  |           |   |
|------------------|-----------|---|
| <b>xt_clken1</b> | Bit 0     | Enable 1 of 32Khz XTAL clock synchronization sequence           |
| <b>xt_clken2</b> | Bit 1     | Enable 2 of 32Khz XTAL clock synchronization sequence           |
| <b>xt_byp</b>    | Bit 2     | 32Khz XTAL Bypass   |
| <b>xt_sw</b>     | Bits 3-6  | 32Khz XTAL switch See table below for recommended switch values |
| <b>xt_off</b>    | Bit 8     | 32Khz XTAL off  |
| Reserved         | Bits 9-12 |   |

Recommended control switch settings:

| XTL Oscillator Performance | SW4 | SW3 | SW2 | SW1 |
|----------------------------|-----|-----|-----|-----|
| Least current              | 1   | 0   | 0   | 0   |
| Fast startup               | 1   | 0   | 1   | 1   |

CCS CTL6 enables the external clock/XTAL clock:

**xt\_clken1**, bit 0 and **xt\_clken2**, bit 1

1. Enable EXT/XTL Clock by setting the xt\_clken2 and xt\_clken1 bits.
2. After sufficient delay for XTAL or external clock source to become stable, the user can switch the CCS clock source to EXT/XTL Clock
3. To stop the clock, clear the two bits in the following sequence:
  - (a) Switch the CCS clock source to other clock source
  - (b) Clear bit xt\_clken2
  - (c) Wait for at least 3 period of XTAL (or external clock)
  - (d) Clear bit xt\_clken1

### CCSCCTL2, Compact Clock System Control 2 Register

|          |       |      |      |      |      |      |      |
|----------|-------|------|------|------|------|------|------|
| 15       | 14    | 13   | 12   | 11   | 10   | 9    | 8    |
| Reserved |       |      |      |      |      |      |      |
| r-0      | r-0   | r-0  | r-0  | r-0  | r-0  | r-0  | r-0  |
| 7        | 6     | 5    | 4    | 3    | 2    | 1    | 0    |
| Reserved | FSELx |      |      |      |      |      |      |
| r-0      | rw-0  | rw-1 | rw-0 | rw-1 | rw-0 | rw-0 | rw-0 |

|                 |             |   |
|-----------------|-------------|---|
| <b>Reserved</b> | Bits 15 – 7 | Reserved. Read back as 0.   |
| <b>FSELx</b>    | Bits 6 – 0  | Frequency trimming of the HF-OSC<br>Value HF-OSC<br>0000000 highest adjustable frequency<br>....<br>0101000 center frequency<br>....<br>1111111 lowest adjustable frequency |

## WDT\_A Registers

WDT\_A registers are described in the Watch Dog Timer (WDT\_A) chapter of the MSP430x09x Family Users Guide ([SLAU321](#)).

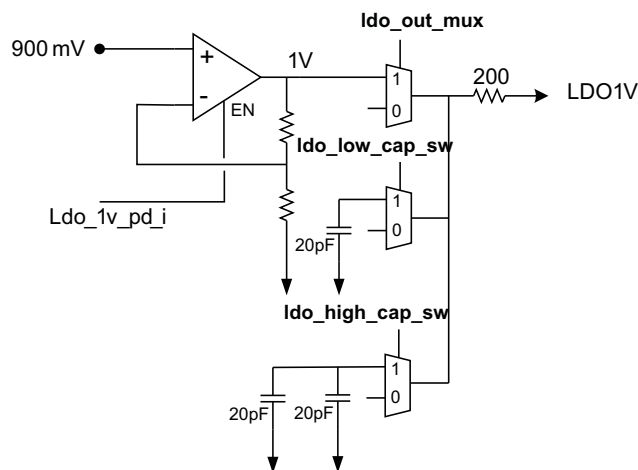
## PMM Registers

Compact System Control chapter of the MSP430x09x Family Users Guide ([SLAU321](#)).

## Peripherals Continued

### LDO1V

The Low Droop Out (LDO) is 1Volt (200 $\mu$ A max) voltage regulator that capable to drive 4 GPIO ports. The regulated 1V output is recommended to use for external RC charge, in order to minimize the effect of battery voltage changes between consecutive RC charges, during Termistor and reference Resistor discharge time measurement.



**Figure 10. LDO1V Block Diagram**

### CP\_1P8

The CP\_1P8 is an internal charge pump module which is used to boost the battery voltage to ~2V. **The voltage boost is mandatory for the LCD operation.**

The CP\_1P8 is sharing the CP\_OSC with the LCD\_CP as the reference clock for the boosting and also using the LF\_clk for voltage feedback sensing.

The CP\_1P8 requires 3 external capacitors for operation which are connected as following:

- 1nF capacitor connected between pads 41 (C1\_out) and 40 (C1\_in)
- 1nF capacitor connected between pads 39 (C2\_out) and 38 (C2\_in)
- 4.7nF capacitor connected between pads 37 and ground – load capacitor.

The CP\_1P8 has a valid signal which indicates when the voltage of the CP\_1P8 has reached a 1.8V (Configurable) to allow operation of the LCD\_CP or of other peripherals.

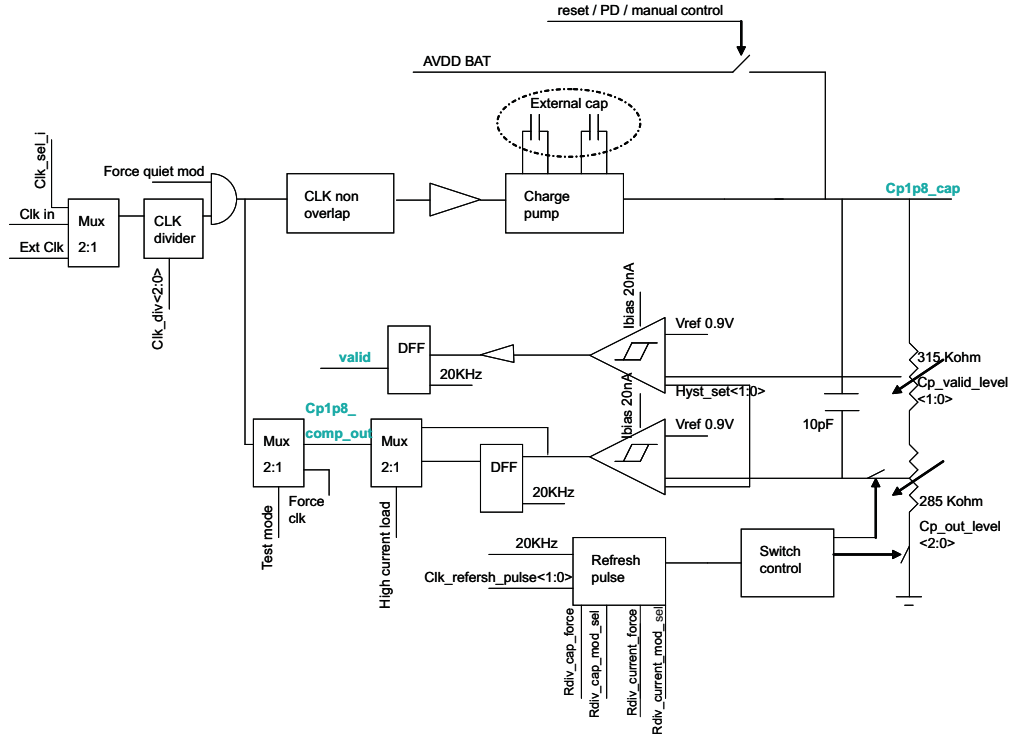
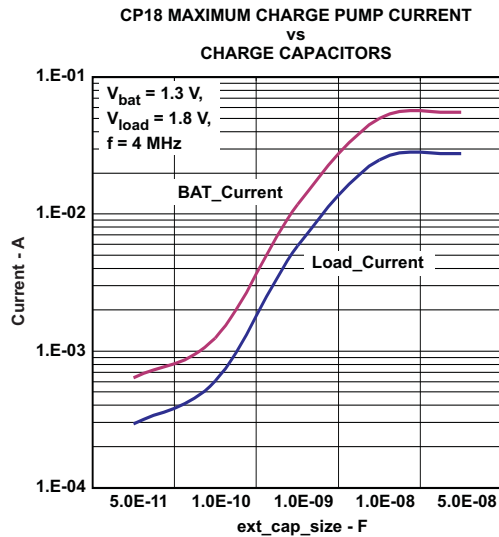
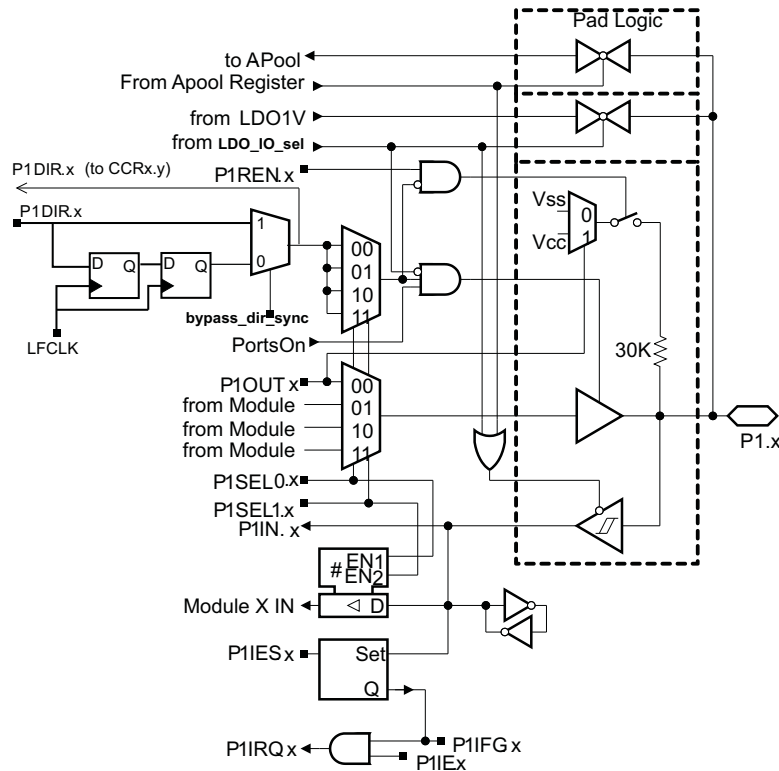


Figure 11. CP\_1P8 Block Diagram



**PARAMETER MEASUREMENT INFORMATION**



**Figure 12. Port P1, P1.0, P1.1, P1.4 Input/Output**

**Table 13. Port P1 (P1.0, P1.1, P1.4) Functions**

| PIN NAME (P1.x)  | x | FUNCTION                               | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |             |                  |
|--|---|--|-------------------------------------|----------|----------|-------------|------------------|
|  |   |  | P1DIR.x                             | P1SEL1.x | P1SEL0.x | NSELx/PSELx | LDO_IO_sel <3-0> |
| P1.0/TA0.2/TA0.1/TA1.2/LDO1/T<br>A0.CC11B0/TA0.CC12B0/A2 | 0 | General-purpose digital I/O            | In:0; Out:1                         | 0        | 0        | 0           | XXX0             |
|  |   | Timer0_A3 Out2 output                  | 1                                   | 0        | 1        | 0           | XXX0             |
|  |   | Timer1_A3 Out2 output                  | 1                                   | 1        | 0        | 0           | XXX0             |
|  |   | Timer0_A3 Out1 output                  | 1                                   | 1        | 1        | 0           | XXX0             |
|  |   | Analog in A2 or<br>Atest1 Out – A Pool | X                                   | X        | X        | 2           | XXXX             |
|  |   | LDO 1V Out                             | 1                                   | X        | X        | X           | XXX1             |
| P1.1/TA0.2/TA0.1/TA1.2/LDO1/T<br>A0.CC11A1/TA0.CC12A1/A1 | 1 | General-purpose digital I/O            | In:0; Out:1                         | 0        | 0        | 0           | XX0X             |
|  |   | Timer0_A3 Out2 output                  | 1                                   | 0        | 1        | 0           | XX0X             |
|  |   | Timer1_A3 Out2 output                  | 1                                   | 1        | 0        | 0           | XX0X             |
|  |   | Timer0_A3 Out1 output                  | 1                                   | 1        | 1        | 0           | XX0X             |
|  |   | Analog in A1 – A-Pool                  | X                                   | X        | X        | 1           | XXXX             |
|  |   | LDO 1V Out                             | 1                                   | X        | X        | X           | XX1X             |
| P1.4/TA0.2/TA0.1/TA1.2/LDO1/T<br>A0.CC11B1/TA0.CC12B1/A0 | 4 | General-purpose digital I/O            | In:0; Out:1                         | 0        | 0        | 0           | X0XX             |
|  |   | Timer0_A3 Out2 output                  | 1                                   | 0        | 1        | 0           | X0XX             |
|  |   | Timer1_A3 Out2 output                  | 1                                   | 1        | 0        | 0           | X0XX             |
|  |   | Timer0_A3 Out1 output                  | 1                                   | 1        | 1        | 0           | X0XX             |
|  |   | Analog in A0 – A-Pool                  | X                                   | X        | X        | 0           | XXXX             |
|  |   | LDO 1V Out                             | 1                                   | X        | X        | X           | X1XX             |

(1) X = Don't care

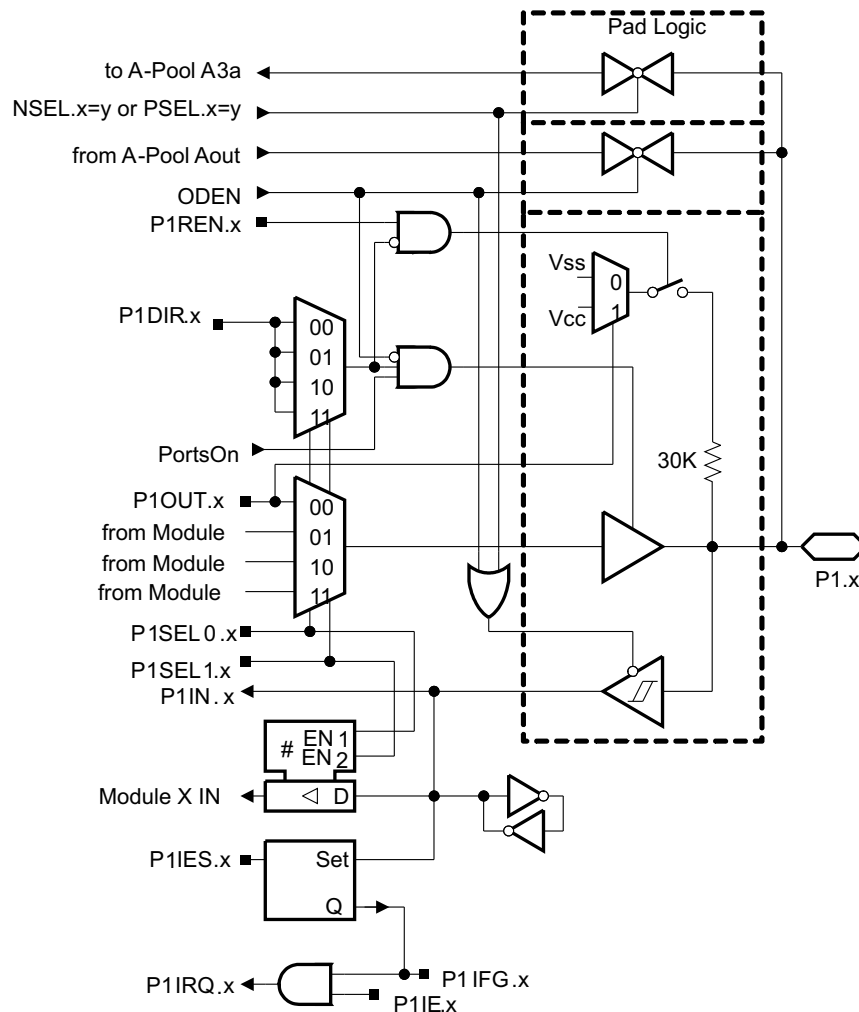
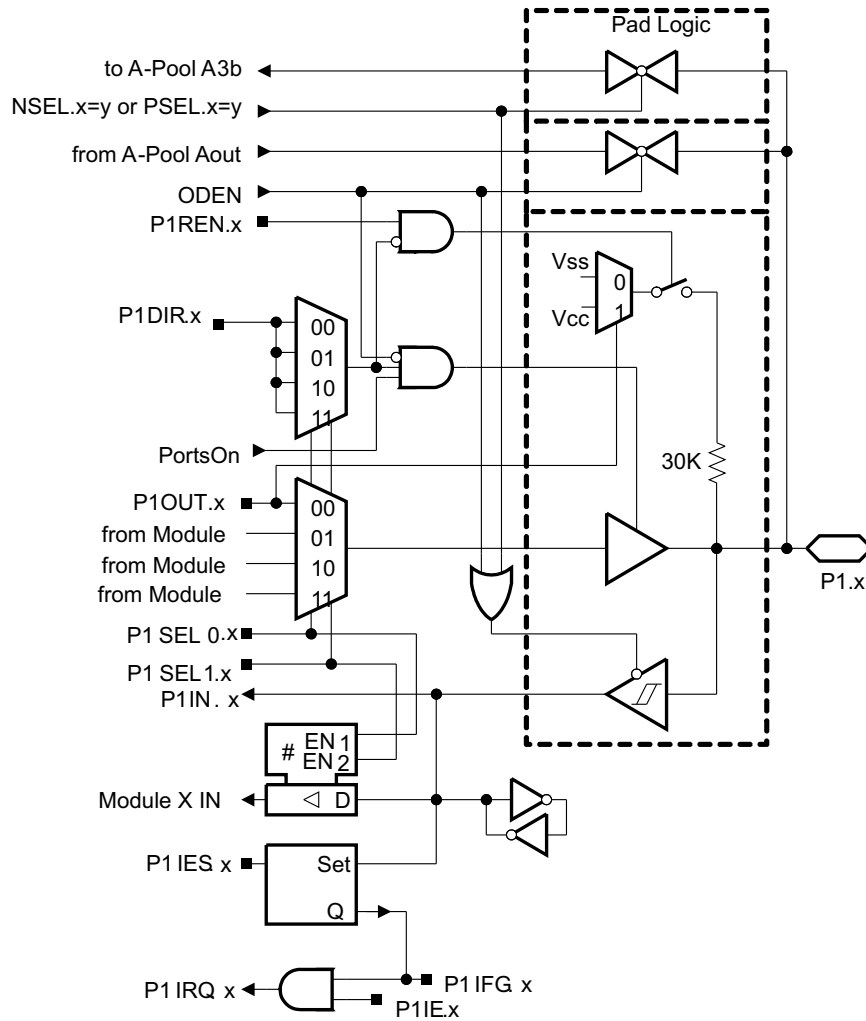


Figure 13. Port P1, P1.2 Input/Output

Table 14. Port P1 (P1.2) Functions

| PIN NAME (P1.x)  | x | FUNCTION                    | CONTROL BITS/SIGNAL <sup>(1)</sup> |          |          |             |      |        |
|--|---|-----------------------------|------------------------------------|----------|----------|-------------|------|--------|
|  |   |                             | P1DIR.x                            | P1SEL1.x | P1SEL0.x | NSELx/PSELx | ODEN | A3PSEL |
| P1.2/TA0.2/TA0.1/TA1.2/<br>AOUT/TA0.CC11A2/TA0.<br>CC12A2/A3 | 2 | General-purpose digital I/O | In:0; Out:1                        | 0        | 0        | #3          | 0    | X      |
|  |   | Timer0_A3 Out2              | 1                                  | 0        | 1        | #3          | 0    | X      |
|  |   | Timer1_A3 Out2              | 1                                  | 1        | 0        | #3          | 0    | X      |
|  |   | Timer0_A3 Out1              | 1                                  | 1        | 1        | #3          | 0    | X      |
|  |   | Analog Input - A3a          | X                                  | X        | X        | 3           | 0    | 0      |
|  |   | A-pool Aout                 | 1                                  | X        | X        | X           | 1    | 0      |

(1) X = Don't care



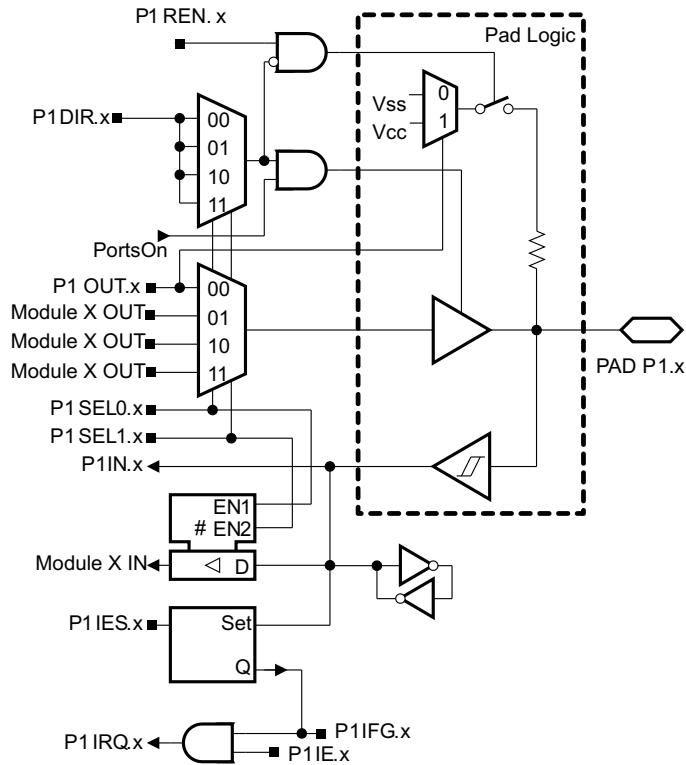
**Figure 14. Port P1, P1.3 Input/Output**

**Table 15. Port P1 (P1.3) Functions**

| PIN NAME (P1.x)   | x | FUNCTION                    | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |             |        |        |
|---|---|-----------------------------|-------------------------------------|----------|----------|-------------|--------|--------|
|   |   |                             | P1DIR.x                             | P1SEL1.x | P1SEL0.x | NSELx/PSELx | VREFEN | A3PSEL |
| P1.3/TA0.2/TA0.1/TA1.2/<br>REFOUT/TA0.CC1A3/T<br>A0.CC12A3/A3 | 3 | General-purpose digital I/O | In:0; Out:1                         | 0        | 0        | #2          | 0      | X      |
|   |   | Timer0_A3 Out2              | 1                                   | 0        | 1        | #2          | 0      | X      |
|   |   | Timer1_A3 Out1              | 1                                   | 1        | 0        | #2          | 0      | X      |
|   |   | Timer0_A3 Out2              | 1                                   | 1        | 1        | #2          | 0      | X      |
|   |   | Timer0_A3 CCR1A3            |                                     |          |          |             |        |        |
|   |   | Timer0_A3 CCR2A3            |                                     |          |          |             |        |        |
|   |   | A-Pool Analog Input - A3b   | X                                   | X        | X        | 2           | 0      | 0      |
|   |   | A-Pool Vref                 | X                                   | X        | X        | X           | 1      | X      |

(1) X = Don't care



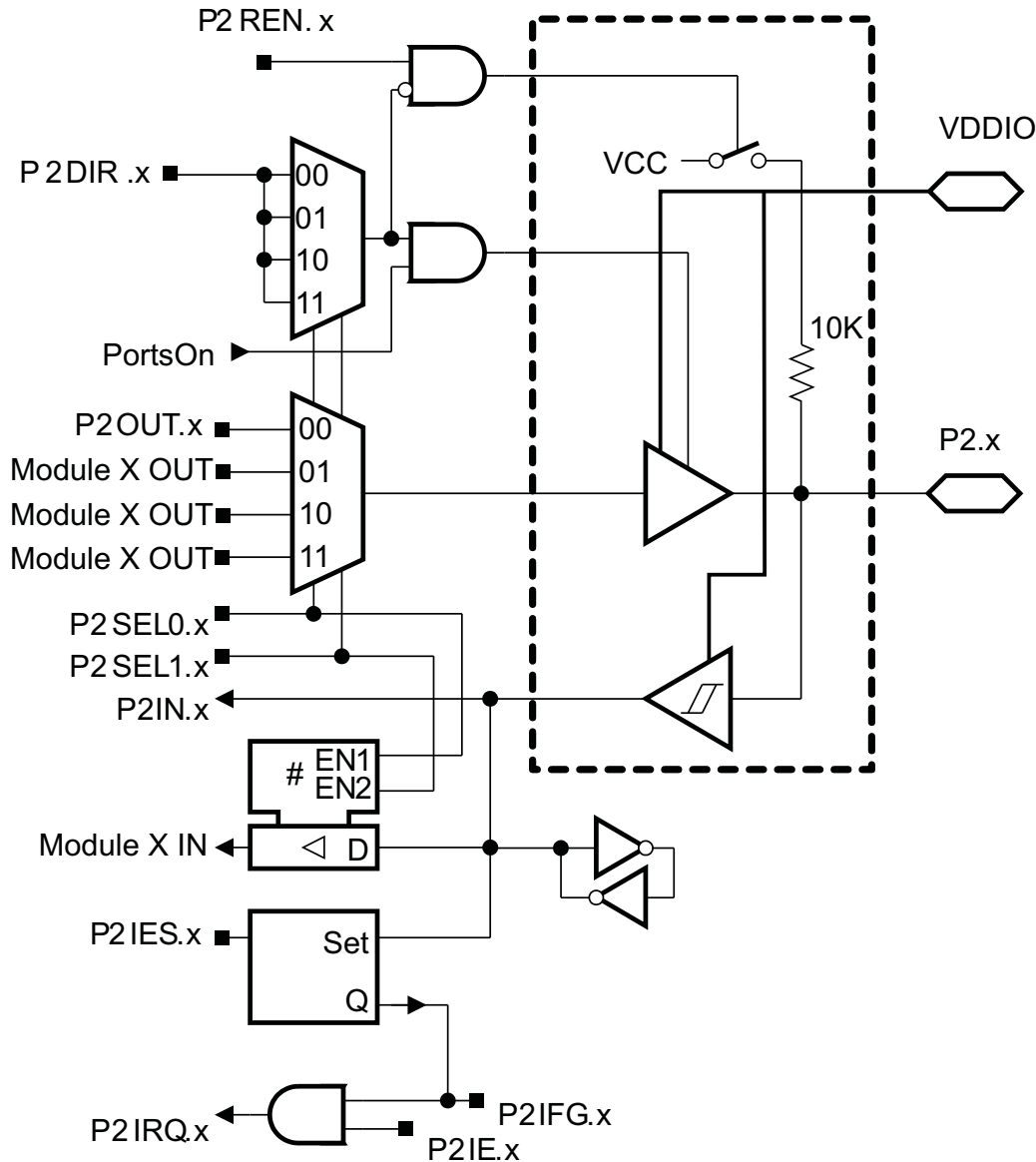


**Figure 15. Port P1, P1.5 to P1.6 Input/Output**

**Table 16. Port P1 (P1.5 to P1.6) Functions**

| PIN NAME (P1.x)        | x | FUNCTION                    | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |
|------------------------|---|-----------------------------|-------------------------------------|----------|----------|
|                        |   |                             | P1DIR.x                             | P1SEL1.x | P1SEL0.x |
| P1.5/TA0.2/TA1.2/TA0.1 | 5 | General-purpose digital I/O | I:0; O:1                            | 0        | 0        |
|                        |   | Timer0_A3 Out2              | 1                                   | 0        | 1        |
|                        |   | Timer1_A3 Out2              | 1                                   | 1        | 0        |
|                        |   | Timer0_A3 Out1              | 1                                   | 1        | 1        |
|                        |   | Timer0_A3 CCR1A3            | 0                                   | ≠0       | ≠0       |
| P1.6/TA0.2/TA1.2/TA0.1 | 6 | General-purpose digital I/O | I:0; O:1                            | 0        | 0        |
|                        |   | Timer0_A3 Out2              | 1                                   | 0        | 1        |
|                        |   | Timer1_A3 Out2              | 1                                   | 1        | 0        |
|                        |   | Timer1_A3 Out1              | 1                                   | 1        | 1        |
|                        |   | Timer1_A2 CCR1B0            | 0                                   | ≠0       | ≠0       |

(1) X = Don't care



**Figure 16. Port P2, P2.0, P2.1, P2.2 and P2.3, Input/Output**

**Table 17. Port P2 (P2.0 to P2.2) Functions**

| PIN NAME (P2.x)            | x | FUNCTION                      | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |           |
|----------------------------|---|-------------------------------|-------------------------------------|----------|----------|-----------|
|                            |   |                               | P2DIR.x                             | P2SEL1.x | P2SEL0.x | JTAG Mode |
| TCK/P2.0/TA1.2/TA1.1/CxOUT | 0 | General-purpose digital I/O   | I:0; O:1                            | 0        | 0        | 0         |
|                            |   | Timer1_A3 Out1                | 1                                   | 0        | 1        | 0         |
|                            |   | Timer1_A3 Out2                | 1                                   | 1        | 0        | 0         |
|                            |   | CxOUT from Apool              | 1                                   | 1        | 1        | 0         |
|                            |   | JTAG-TCK <sup>(2)(3)(4)</sup> | x                                   | x        | x        | 1         |

(1) X = Don't care  
 (2) JTAG signals TMS, TCK and TDI read as "1" when not configured as explicit JTAG terminals.  
 (3) JTAG overrides digital output control when configured as explicit JTAG terminals.  
 (4) JTAG function with enabled pull up resistors is default after power up.

**Table 17. Port P2 (P2.0 to P2.2) Functions (continued)**

| PIN NAME (P2.x)               | x | FUNCTION                      | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |           |
|-------------------------------|---|-------------------------------|-------------------------------------|----------|----------|-----------|
|                               |   |                               | P2DIR.x                             | P2SEL1.x | P2SEL0.x | JTAG Mode |
| TMS/P2.1/ EXT_CLK/TA0.1/TA0.2 | 1 | General-purpose digital I/O   | I:0; O:1                            | 0        | 0        | 0         |
|                               |   | EXT_CLK Out                   | 1                                   | 0        | 1        | 0         |
|                               |   | Timer0_A3 Out1                | 1                                   | 1        | 0        | 0         |
|                               |   | Timer0_A3 Out2                | 1                                   | 1        | 1        | 0         |
|                               |   | JTAG-TMS <sup>(2)(3)(4)</sup> | x                                   | x        | x        | 1         |
| TDI/P2.2/HF_CLK/CxOUT/TA1.0   | 2 | General-purpose digital I/O   | I:0; O:1                            | 0        | 0        | 0         |
|                               |   | HF_CLK Out                    | 1                                   | 0        | 1        | 0         |
|                               |   | Timer1_A3 Out0                | 1                                   | 1        | 0        | 0         |
|                               |   | CxOUT from Apool              | 1                                   | 1        | 1        | 0         |
|                               |   | JTAG-TDI <sup>(2)(3)(4)</sup> | X                                   | X        | X        | 1         |

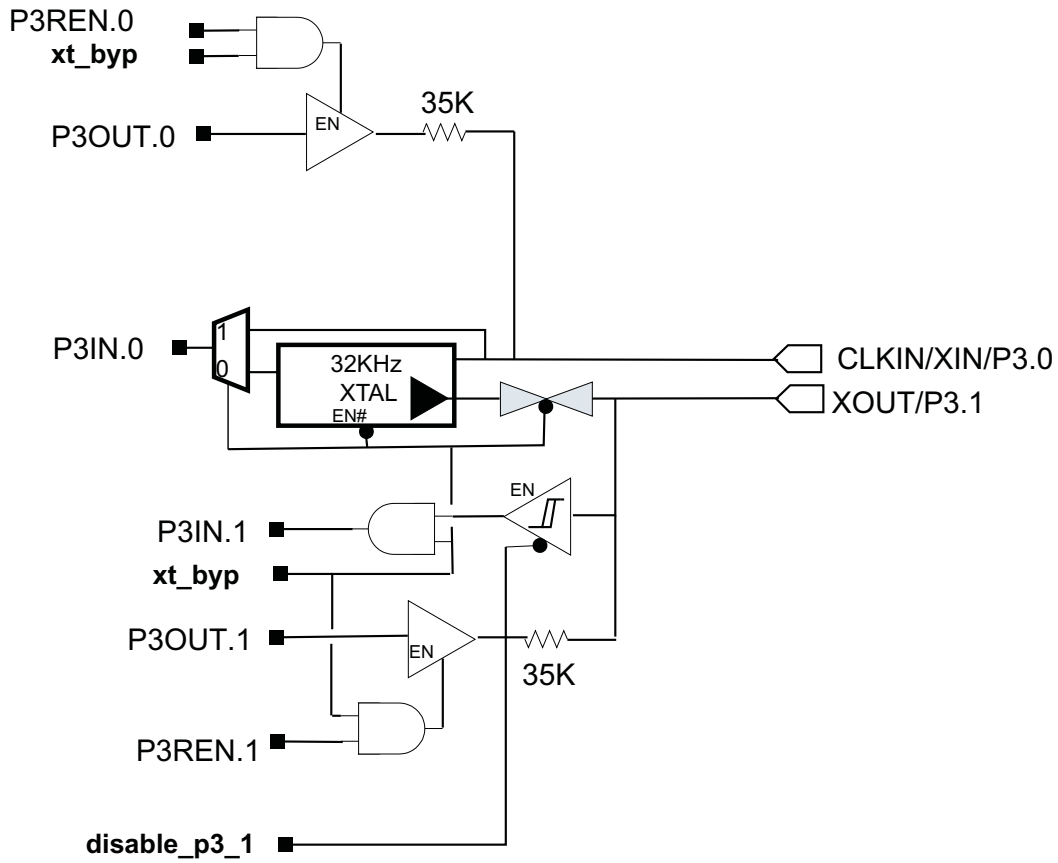
**Port P2, P2.3, Input/Output**
**Table 18. Port P2 (P2.3) Functions**

| PIN NAME (P2.x)      | x | FUNCTION                    | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |
|----------------------|---|-----------------------------|-------------------------------------|----------|----------|
|                      |   |                             | P2DIR.x                             | P2SEL1.x | P2SEL0.x |
| TDO/P2.3/LFCLK/TA0.2 | 3 | General-purpose digital I/O | I:0; O:1                            | 0        | 0        |
|                      |   | LFCLK Out                   | 1                                   | 0        | 1        |
|                      |   | Timer0_A3 Out2              | 1                                   | 1        | 0        |
|                      |   | JTAG-TDO <sup>(2)(3)</sup>  | 1                                   | 1        | 1        |

(1) X = Don't care

(2) Configuring P2.3 to JTAG-TDO turns P2.0 to P2.3 also into JTAG functions

(3) JTAG function with disabled pull up resistors is default after power up.



**Figure 17. Port P3, P3.0, P3.1 Input/Output**

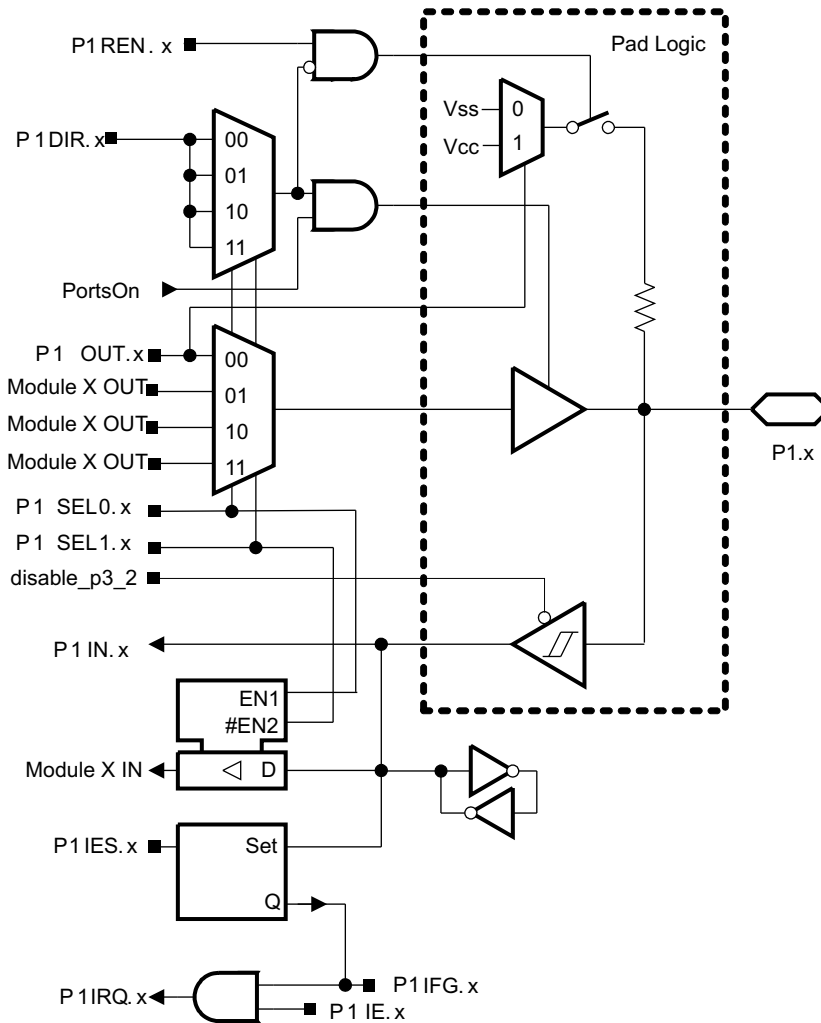


Figure 18. Port P3, P3.2, P3.4 Input/Output

Table 19. Port P3 (P3.2, P3.4, P3.5) Functions

| PIN NAME (P3.x)                       | x | FUNCTION                                       | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |              |
|---------------------------------------|---|--|-------------------------------------|----------|----------|--------------|
|                                       |   |  | P3DIR.x                             | P3SEL1.x | P3SEL0.x | disable_p3_x |
| P3.2/ TA0.1/TA1.1/TA1.0               | 2 | General-purpose digital I/O                    | I:0; O:1                            | 0        | 0        | I:0; O:X     |
|                                       |   | Timer0_A3 Out1 output                          | 1                                   | 0        | 1        | X            |
|                                       |   | Timer1_A3 Out1 output                          | 1                                   | 1        | 0        | X            |
|                                       |   | Timer1_A3 Out0 output                          | 1                                   | 1        | 1        | X            |
| P3.4/TA0.1/TA1.1/TA1.0/<br>TA1.CC12A2 | 4 | General-purpose digital I/O                    | I:0; O:1                            | 0        | 0        | In:0; Out:X  |
|                                       |   | Timer0_A3 Out1 output                          | 1                                   | 0        | 1        | X            |
|                                       |   | Timer1_A3 Out1 output                          | 1                                   | 1        | 0        | X            |
|                                       |   | Timer1_A3 Out0 output                          | 1                                   | 1        | 1        | X            |
|                                       |   | Timer1_A3 CCR2A2 capture: CC12A2 input compare | X                                   | X        | X        | 0            |

(1) Don't Care

**Table 19. Port P3 (P3.2, P3.4, P3.5) Functions (continued)**

| PIN NAME (P3.x)                       | x | FUNCTION  | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |              |
|---------------------------------------|---|---|-------------------------------------|----------|----------|--------------|
|                                       |   |   | P3DIR.x                             | P3SEL1.x | P3SEL0.x | disable_p3_x |
| P3.5/TA0.1/TA1.1/TA1.0/<br>TA1.CCI2A3 | 5 | General-purpose digital I/O                     | In:0; Out:1                         | 0        | 0        | In:0; Out:X  |
|                                       |   | Timer0_A3 Out1 output                           | 1                                   | 0        | 1        | X            |
|                                       |   | Timer1_A3 Out1 output                           | 1                                   | 1        | 0        | X            |
|                                       |   | Timer1_A3 Out0 output                           | 1                                   | 1        | 1        | X            |
|                                       |   | Timer1_A3 CCR2A3 capture: CCI2A3 input, compare | X                                   | X        | X        | 0            |

**Table 20. Port P3 (P3.6) Functions**

| PIN NAME (P3.x)  | x | FUNCTION  | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |                  |
|--|---|---|-------------------------------------|----------|----------|------------------|
|  |   |   | P3DIR.x                             | P3SEL1.x | P3SEL0.x | Sel_port3_6<1:0> |
| P3.6/TA0.0/TA0.1/TA0.2/TA0.0<br>N/<br>TA0.1N/TA0.2N/TA1.CCI1A3/<br>TA1.1/BOR/ACTSEN/LFOSC/C<br>P18OK | 6 | 10mA General-purpose digital I/O                | In:0; Out:1                         | 0        | 0        | XX               |
|  |   | Timer0_A3 Out0 output                           | 1                                   | 0        | 1        | 00               |
|  |   | Timer0_A3 Out1 output                           | 1                                   | 0        | 1        | 01               |
|  |   | Timer0_A3 Out2 output                           | 1                                   | 0        | 1        | 10               |
|  |   | Timer1_A3 Out1 output                           | 1                                   | 0        | 1        | 11               |
|  |   | Timer0_A3 Out0# output                          | 1                                   | 1        | 0        | 00               |
|  |   | Timer0_A3 Out1# output                          | 1                                   | 1        | 0        | 01               |
|  |   | Timer0_A3 Out2# output                          | 1                                   | 1        | 0        | 10               |
|  |   | Timer1_A3 Out1# output                          | 1                                   | 1        | 0        | 11               |
|  |   | BOR Out   | 1                                   | 1        | 1        | 00               |
|  |   | Activation Sense Output                         | 1                                   | 1        | 1        | 01               |
|  |   | LFCLK Out                                       | 1                                   | 1        | 1        | 10               |
|  |   | CP 1.8V OK Out                                  | 1                                   | 1        | 1        | 11               |
|  |   | Timer1_A3 CCR1A3 capture: CCI1A3 input, compare | X                                   | X        | X        | XX               |

(1) Don't Care

**Table 21. Port P3 (P3.7) Functions**

| PIN NAME (P3.x)   | x | FUNCTION  | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |                  |
|---|---|---|-------------------------------------|----------|----------|------------------|
|   |   |   | P3DIR.x                             | P3SEL1.x | P3SEL0.x | Sel_port3_7<1:0> |
| P3.7/TA0.0/TA0.1/TA0.2/TA0.0<br>N/TA0.1N/<br>TA0.2N/TA1.CCI2A1/HFOSC/L<br>CDCPCLK/<br>LCDCLK/1KCLK/LCDCMP | 7 | 10mA General-purpose digital I/O                | In:0; Out:1                         | 0        | 0        | XX               |
|   |   | Timer0_A3 Out0 output                           | 1                                   | 0        | 1        | 00               |
|   |   | Timer0_A3 Out1 output                           | 1                                   | 0        | 1        | 01               |
|   |   | Timer0_A3 Out2 output                           | 1                                   | 0        | 1        | 10               |
|   |   | LCD Voltage Comparator Out                      | 1                                   | 0        | 1        | 11               |
|   |   | Timer0_A3 Out0# output                          | 1                                   | 1        | 0        | 00               |
|   |   | Timer0_A3 Out1# output                          | 1                                   | 1        | 0        | 01               |
|   |   | Timer0_A3 Out2# output                          | 1                                   | 1        | 0        | 10               |
|   |   | LCD Voltage Comparator Out#                     | 1                                   | 1        | 0        | 11               |
|   |   | LCD Charge Pump Clock Out                       | 1                                   | 1        | 1        | 00               |
|   |   | LCD Frame Clock Out                             | 1                                   | 1        | 1        | 01               |
|   |   | HFCLK Out                                       | 1                                   | 1        | 1        | 10               |
|   |   | 1Khz Activation Clock Out                       | 1                                   | 1        | 1        | 11               |
|   |   | Timer1_A3 CCR2A1 capture: CCI2A1 input, compare |                                     |          |          |                  |

(1) Don't Care

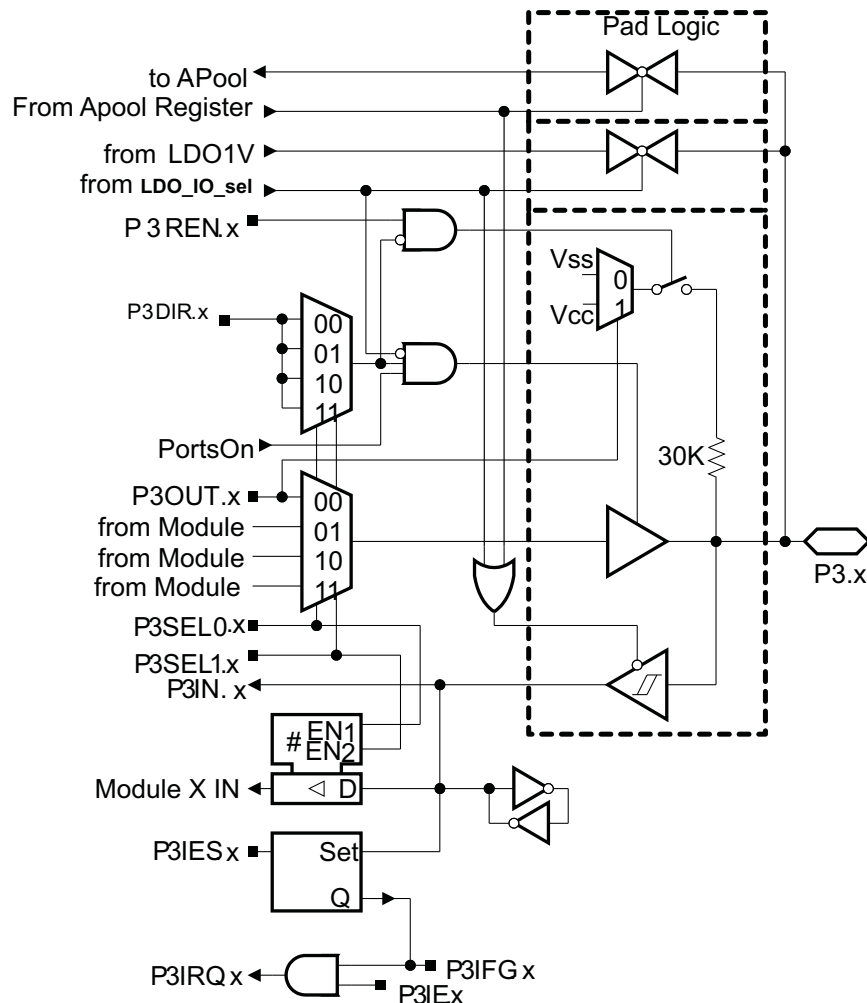


Figure 19. Port P3, P3.3, Input/Output

Table 22. Port P3 (P3.3) Functions

| PIN NAME (P3.x)                 | x | FUNCTION                    | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |             |                  |
|---------------------------------|---|-----------------------------|-------------------------------------|----------|----------|-------------|------------------|
|                                 |   |                             | P1DIR.x                             | P1SEL1.x | P1SEL0.x | NSELx/PSELx | LDO_IO_sel <3-0> |
| P3.3/ TA0.1/TA1.1/TA1.0/A0/LDO1 | 3 | General-purpose digital I/O | In:0; Out:1                         | 0        | 0        | 0           | 0XXX             |
|                                 |   | Timer0_A3 Out1 output       | 1                                   | 0        | 1        | 0           | 0XXX             |
|                                 |   | Timer1_A3 Out1 output       | 1                                   | 1        | 0        | 0           | 0XXX             |
|                                 |   | Timer1_A3 Out0 output       | 1                                   | 1        | 1        | 0           | 0XXX             |
|                                 |   | Analog input A0 – A-Pool    | X                                   | X        | X        | 0           | XXXX             |
|                                 |   | LDO 1V Out                  | 1                                   | X        | X        | X           | 1XXX             |

(1) X = Don't care

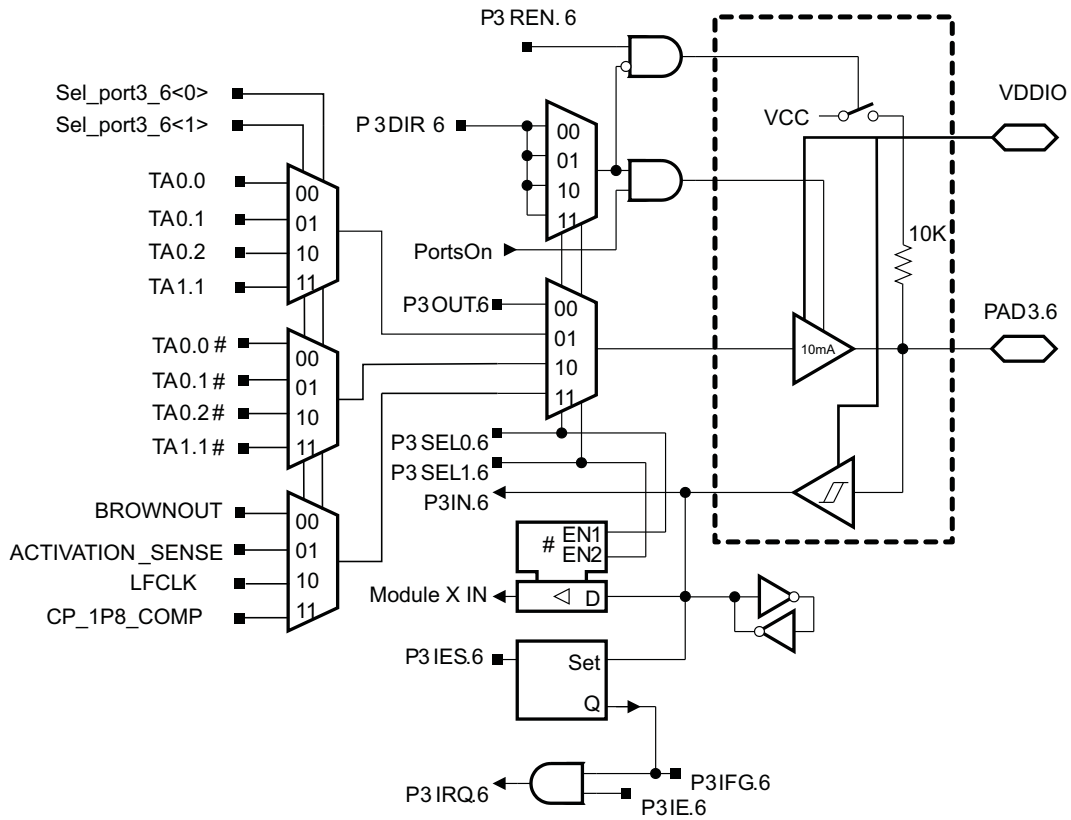


Figure 20. Port P3, P3.6, Input/Output

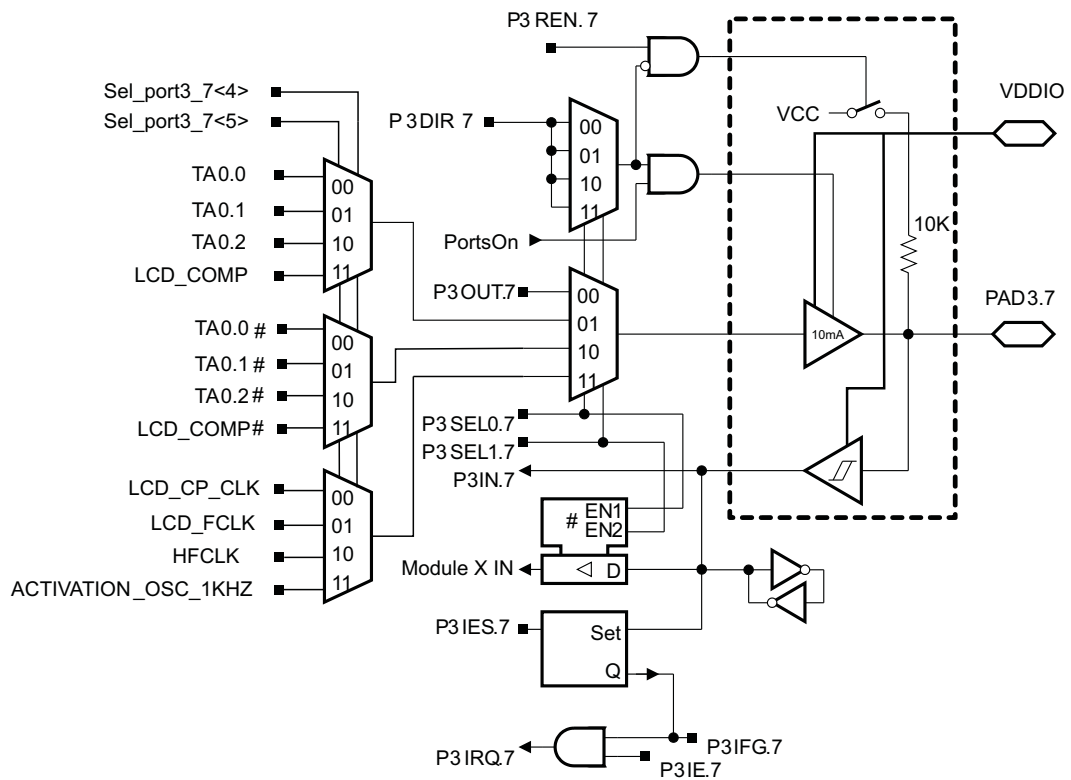


Figure 21. Port P3, P3.7, Input/Output



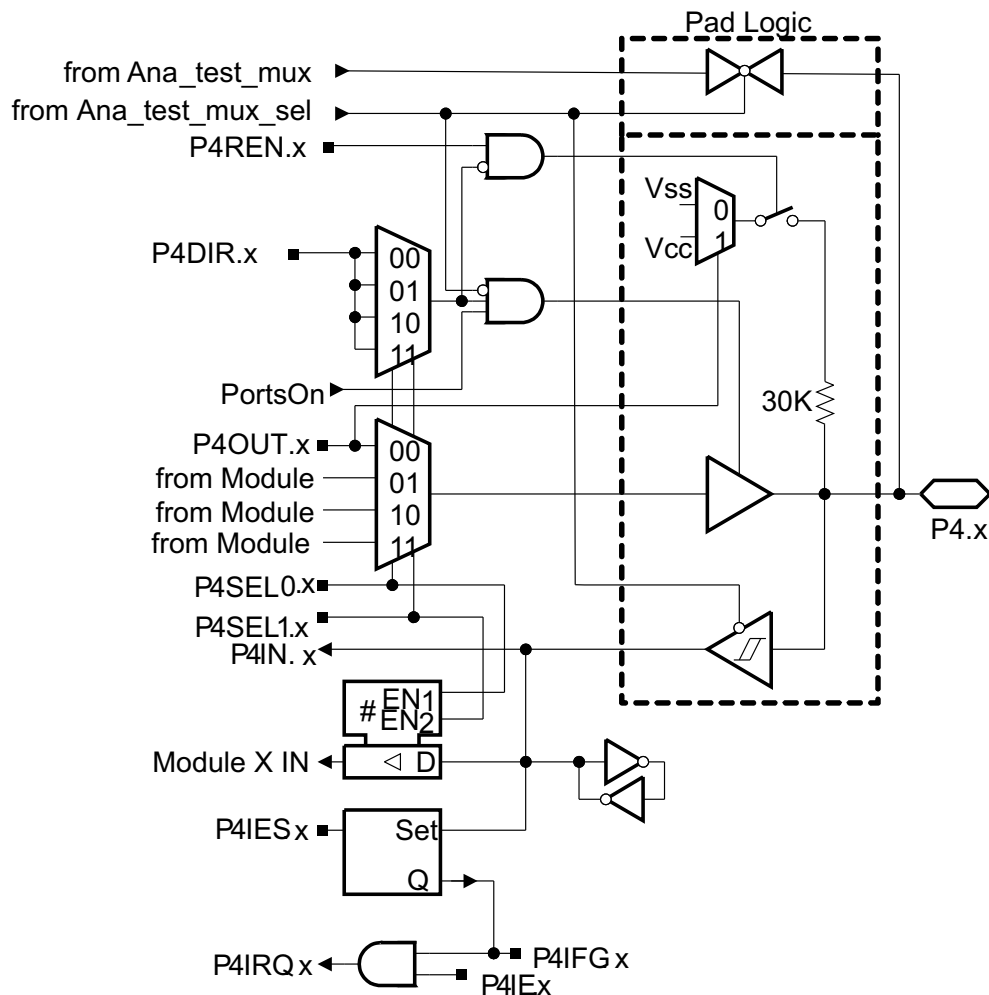
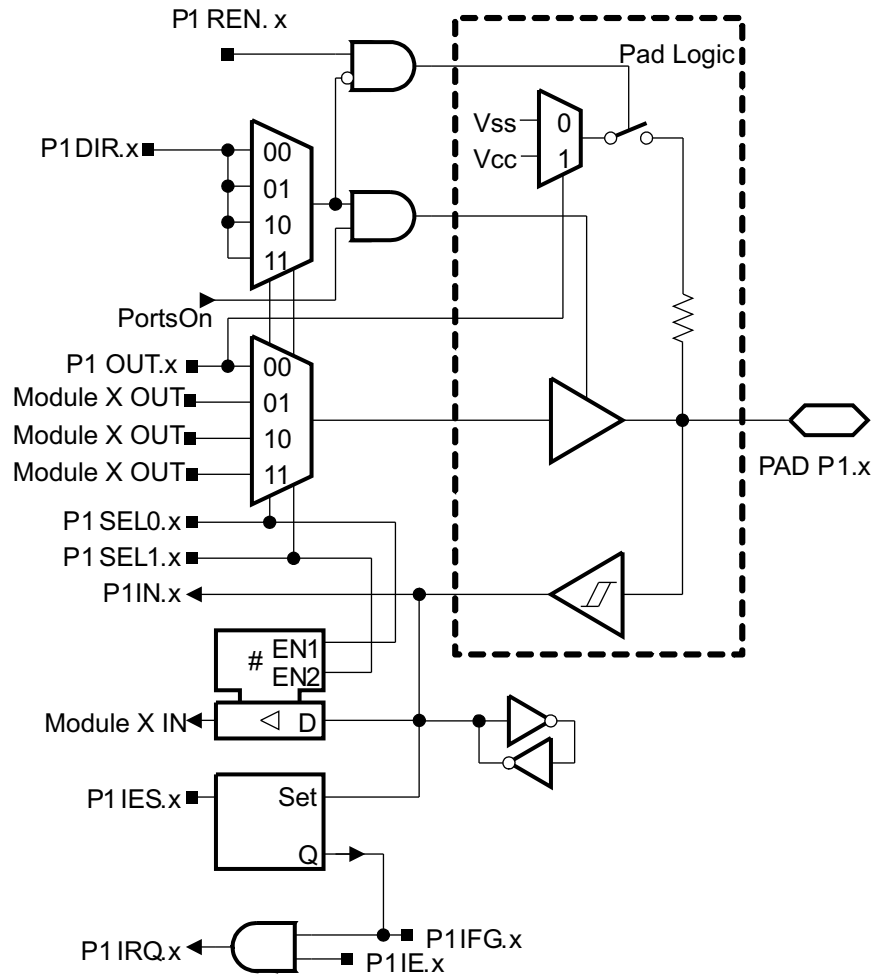


Figure 22. Port P4 (P4.0) Pin Input/Output

Table 23. Port P4 (P4.0) Pin Functions

| PIN NAME (P4.x)                    | x | FUNCTION                    | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |                   |
|------------------------------------|---|-----------------------------|-------------------------------------|----------|----------|-------------------|
|                                    |   |                             | P4DIR.x                             | P4SEL1.x | P4SEL0.x | Ana_test_mux<3:0> |
| P4.0/TA0.2/TA1.2/ACLK/ATEST/SPI_CS | 0 | General-purpose digital I/O | I:0; O:1                            | 0        | 0        | 0                 |
|                                    |   | Timer0_A3 Out2 output       | 1                                   | 0        | 1        | 0                 |
|                                    |   | Timer1_A3 Out2 output       | 1                                   | 1        | 0        | 0                 |
|                                    |   | ACLK Out                    | 1                                   | 1        | 1        | 0                 |
|                                    |   | Analog Test Multiplexer Out |                                     |          |          | /=0               |
|                                    |   | SPI Chip Select             | 1                                   | 0        | 0        | 0                 |

(1) Don't Care



**Figure 23. Port P4 (P4.1, P4.2, P4.3) Pin Input/Output**

**Table 24. Port P4 (P4.1, P4.2, P4.3) Pin Functions**

| PIN NAME (P4.x)                     | x | FUNCTION                       | CONTROL BITS/SIGNALS <sup>(1)</sup> |          |          |
|-------------------------------------|---|--------------------------------|-------------------------------------|----------|----------|
|                                     |   |                                | P4DIR.x                             | P4SEL1.x | P4SEL0.x |
| P4.1/TA0.2/TA1.2/SMCLK/<br>SPI_MOSI | 1 | General-purpose digital I/O    | I:0; O:1                            | 0        | 0        |
|                                     |   | Timer0_A3 Out2 output          | 1                                   | 0        | 1        |
|                                     |   | Timer1_A3 Out2 output          | 1                                   | 1        | 0        |
|                                     |   | SMCLK Out                      | 0                                   | 1        | 1        |
|                                     |   | SPI Serial In                  | 0                                   | 0        | 0        |
| P4.2/TA0.2/TA1.2/MCLK/<br>SPI_CLK   | 2 | General-purpose digital I/O    | I:0; O:1                            | 0        | 0        |
|                                     |   | Timer0_A3 Out2 output          | 1                                   | 0        | 1        |
|                                     |   | Timer1_A3 Out2 output          | 1                                   | 1        | 0        |
|                                     |   | MCLK Out                       | 0                                   | 1        | 1        |
|                                     |   | SPI Clock Out                  | 1                                   | 0        | 0        |
| P4.3/TA0.2/TA1.2/1KOSC/<br>SPI_MISO | 3 | General-purpose digital I/O    | I:0; O:1                            | 0        | 0        |
|                                     |   | Timer0_A3 Out2 output          | 1                                   | 0        | 1        |
|                                     |   | Timer1_A3 Out2 output          | 1                                   | 1        | 0        |
|                                     |   | 1KHz Activation Oscillator Out | 0                                   | 1        | 1        |
|                                     |   | SPI Serial Out                 | 1                                   | 0        | 0        |

(1) Don't Care

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/ Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|-------------------|------------------------------|-----------------------------|
| AFE4110B000YS    | ACTIVE                | WAFERSALE    | YS              | 0    | 1           | TBD                     | Call TI           | Call TI                      |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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