Features

- Utilizes the ARM7TDMI® ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - EmbeddedICE™ (In-Circuit Emulation)
- 8K Bytes Internal SRAM
- Fully-programmable External Bus Interface (EBI)
  - Maximum External Address Space of 128M Bytes
  - 8 Chip Selects
  - Software Programmable 8/16-bit External Databus
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 7 External Interrupts, Including a High-priority, Low-latency Interrupt Request
- 58 Programmable I/O Lines
- 6-channel 16-bit Timer/Counter
  - 6 External Clock Inputs and 2 Multi-purpose I/O Pins per Channel
- 3 USARTs
- Master/Slave SPI Interface
  - 8-bit to 16-bit Programmable Data Length
  - 4 External Slave Chip Selects
- Programmable Watchdog Timer
- 8-channel 10-bit ADC
- 2-channel 10-bit DAC
- Clock Generator with On-chip Main Oscillator and PLL for Multiplication
  - 3 to 20 MHz Frequency Range Main Oscillator
- Real-time Clock with On-chip 32 kHz Oscillator
  - Battery Backup Operation and External Alarm
- 8-channel Peripheral Data Controller for USARTs and SPIs
- Advanced Power Management Controller (APMC)
  - Normal, Wait, Slow, Standby and Power-down modes
- IEEE® 1149.1 JTAG Boundary-scan on all Digital Pins
- Fully Static Operation: 0 Hz to 33 MHz Internal Frequency Range at VDDCORE = 3.0V, 85° C
- 2.7V to 3.6V Core Operating Range, 2.7V to 5.5V I/O Operating Range
- 2.7V to 3.6V Analog Operating Range
- 1.8V to 3.6V Backup Battery Operating Range
- 2.7V to 3.6V Oscillator and PLL Operating Range
- -40° C to +85° C Temperature Range
- Available in a 176-lead LQFP (Green) or 176-ball BGA Package (RoHS-compliant)

AT91 ARM Thumb-based Microcontrollers

AT91M55800A Summary

1. Description

The AT91M55800A is a member of the Atmel AT91 16/32-bit microcontroller family, which is based on the ARM7TDMI processor core. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications.

The fully programmable External Bus Interface provides a direct connection to off-chip memory in as fast as one clock cycle for a read or write operation. An eight-level prior-

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ity vectored interrupt controller in conjunction with the peripheral data controller significantly improve the real-time performance of the device.

The device is manufactured using Atmel's high-density CMOS technology. By combining the ARM7TDMI processor core with an on-chip SRAM, a wide range of peripheral functions, analog interfaces and low-power oscillators on a monolithic chip, the Atmel AT91M55800A is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many ultra low-power applications.

2. Pin Configurations

Table 2-1. Pin Configuration for 176-lead LQFP Package

Pin	AT91M55800A	Pin	AT91M55800A	Pin	AT91M55800A	Pin	AT91M55800A
1	GND	45	GND	89	GND	133	GND
2	GND	46	GND	90	GND	134	GND
3	NCS0	47	D8	91	PA19/RXD1	135	NCS4
4	NCS1	48	D9	92	PA20/SCK2	136	NCS5
5	NCS2	49	D10	93	PA21/TXD2	137	NCS6
6	NCS3	50	D11	94	PA22/RXD2	138	NCS7
7	NLB/A0	51	D12	95	PA23/SPCK	139	PB0
8	A1	52	D13	96	PA24/MISO	140	PB1
9	A2	53	D14	97	PA25/MOSI	141	PB2
10	A3	54	D15	98	PA26/NPCS0/NSS	142	PB3/IRQ4
11	A4	55	PB19/TCLK0	99	PA27/NPCS1	143	PB4/IRQ5
12	A5	56	PB20/TIOA0	100	PA28/NPCS2	144	PB5
13	A6	57	PB21/TIOB0	101	PA29/NPCS3	145	PB6/AD0TRIG
14	A7	58	PB22/TCLK1	102	VDDIO	146	PB7/AD1TRIG
15	VDDIO	59	VDDIO	103	GND	147	VDDIO
16	GND	60	GND	104	VDDPLL	148	GND
17	A8	61	PB23/TIOA1	105	XIN	149	PB8
18	A9	62	PB24/TIOB1	106	XOUT	150	PB9
19	A10	63	PB25/TCLK2	107	GNDPLL	151	PB10
20	A11	64	PB26/TIOA2	108	PLLRC	152	PB11
21	A12	65	PB27/TIOB2	109	VDDBU[2]	153	PB12
22	A13	66	PA0/TCLK3	110	XIN32[2]	154	PB13
23	A14	67	PA1/TIOA3	111	XOUT32[2]	155	PB14
24	A15	68	PA2/TIOB3	112	NRSTBU[2]	156	PB15
25	A16	69	PA3/TCLK4	113	GNDBU[2]	157	PB16
26	A17	70	PA4/TIOA4	114	WAKEUP[2]	158	PB17
27	A18	71	PA5/TIOB4	115	SHDN[2]	159	NWDOVF
28	A19	72	PA6/TCLK5	116	GNDBU[1]	160	MCKO
29	VDDIO	73	VDDIO	117	VDDA[1]	161	VDDIO
30	GND	74	GND	118	AD0[1]	162	GND
31	A20	75	PA7/TIOA5	119	AD1[1]	163	PB18/BMS
32	A21	76	PA8/TIOB5	120	AD2[1]	164	JTAGSEL
33	A22	77	PA9/IRQ0	121	AD3[1]	165	TMS
34	A23	78	PA10/IRQ1	122	AD4[1]	166	TDI
35	D0	79	PA11/IRQ2	123	AD5[1]	167	TDO
36	D1	80	PA12/IRQ3	124	AD6[1]	168	TCK
37	D2	81	PA13/FIQ	125	AD7[1]	169	NTRST
38	D3	82	PA14/SCK0	126	ADVREF[1]	170	NRST
39	D4	83	PA15/TXD0	127	DAVREF[1]	171	NWAIT
40	D5	84	PA16/RXD0	128	DA0[1]	172	NOE/NRD
41	D6	85	PA17/SCK1	129	DA1[1]	173	NWE/NWR0
42	D7	86	PA18/TXD1/NTRI	130	GNDA[1]	174	NUB/NWR1
43	VDDCORE	87	VDDCORE	131	VDDCORE	175	VDDCORE
44	VDDIO	88	VDDIO	132	VDDIO	176	VDDIO

Notes: 1. Analog pins
2. Battery backup pins

Table 2-2. Pin Configuration for 176-ball BGA Package

Pin	AT91M55800A
A1	NCS1
A2	NWAIT
A3	NRST
A4	NTRST
A5	PB18/BMS
A6	NWDOVF
A7	PB16
A8	PB12
A9	PB10
A10	PB9
A11	PB8
A12	NCS7
A13	NCS6
A14	GND
A15	DAVREF
B1	NCS2
B2	NUB/NWR1
B3	NWE/NWR0
B4	NOE/NRD
B5	TD0
B6	TDI
B7	PB17
B8	PB11
B9	PB7/AD1TRIG
B10	PB3/IRQ4
B11	PB2
B12	NCS5
B13	NCS4
B14	DA1
B15	GNDA
J1	A17
J2	A18
J3	VDDIO
J4	A16
J5	–
J6	–
J7	–
J8	–
J9	–
J10	–
J11	–
J12	PA29/NPCS3
J13	SHDN
J14	VDDPLL
J15	PLLRC

Pin	AT91M55800A
C1	A0/NLB
C2	NCS0
C3	VDDIO
C4	VDDCORE
C5	TMS
C6	VDDIO
C7	MCK0
C8	PB13
C9	PB6/AD0TRIG
C10	VDDIO
C11	PB4/IRQ5
C12	PB0
C13	VDDIO
C14	DA0
C15	ADVREF
D1	A2
D2	A1
D3	NCS3
D4	GND
D5	TCK
D6	JTAGSEL
D7	GND
D8	PB15
D9	PB14
D10	PB5
D11	PB1
D12	GND
D13	VDDCORE
D14	AD7
D15	VDDA
L1	A20
L2	A23
L3	D0
L4	D1
L5	–
L6	–
L7	–
L8	–
L9	–
L10	–
L11	–
L12	PA25/MOSI
L13	PA22RXD2
L14	PA26/NPCS0/NSS
L15	XOUT

Pin	AT91M55800A
E1	A4
E2	A3
E3	A5
E4	GND
E5	–
E6	–
E7	–
E8	–
E9	–
E10	–
E11	–
E12	AD6
E13	AD5
E14	NRSTBU
E15	GNDBU
F1	A10
F2	A7
F3	VDDIO
F4	A6
F5	–
F6	–
F7	–
F8	–
F9	–
F10	–
F11	–
F12	GND
F13	AD4
F14	VDDBU
F15	XOUT32
N1	D4
N2	D6
N3	VDDIO
N4	D14
N5	PB19/TCLK0
N6	VDDIO
N7	PB25/TCLK2
N8	PA1/TIOA3
N9	VDDIO
N10	PA8/TIOB5
N11	PA9/IRQ0
N12	VDDCORE
N13	VDDIO
N14	PA19/RXD1
N15	GND

Pin	AT91M55800A
G1	A12
G2	A9
G3	A8
G4	GND
G5	–
G6	–
G7	–
G8	–
G9	–
G10	–
G11	–
G12	AD3
G13	AD2
G14	GND
G15	XIN32
H1	A15
H2	A14
H3	A13
H4	A11
H5	–
H6	–
H7	–
H8	–
H9	–
H10	–
H11	–
H12	AD1
H13	AD0
H14	WAKEUP
H15	GND
R1	D10
R2	D11
R3	D12
R4	D13
R5	PB20/TIOA0
R6	PB23/TIOA1
R7	PB24/TIOB1
R8	PA3/TCLK4
R9	PA4/TIOA4
R10	PA5/TIOB4
R11	PA6/TCLK5
R12	PA12/IRQ3
R13	PA14/SCK0
R14	PA15/TXD0
R15	PA16/RXD0

Table 2-2. Pin Configuration for 176-ball BGA Package (Continued)

Pin	AT91M55800A	Pin	AT91M55800A	Pin	AT91M55800A	Pin	AT91M55800A
K1	A19	M1	D2	P1	D5		
K2	A22	M2	D3	P2	D7		
K3	A21	M3	VDDCORE	P3	D8		
K4	GND	M4	GND	P4	D9		
K5	–	M5	GND	P5	D15		
K6	–	M6	PB21/TIOB0	P6	PB22/TCLK1		
K7	–	M7	GND	P7	PB26/TIOA2		
K8	–	M8	PB27/TIOB2	P8	PA2/TIOB3		
K9	–	M9	PA0/TCLK3	P9	PA7/TIOA5		
K10	–	M10	GND	P10	PA10/IRQ1		
K11	–	M11	PA23/SPCK	P11	PA11/IRQ2		
K12	PA28/NPCS2	M12	GND	P12	PA13/FIQ		
K13	VDDIO	M13	PA21/TXD2	P13	PA17SCK1		
K14	PA27/NPCS1	M14	PA24/MISO	P14	PA18/TXD1/NTRI		
K15	GNDPLL	M15	XIN	P15	PA20/SCK2		

Figure 2-1. 176-lead LQFP Pinout

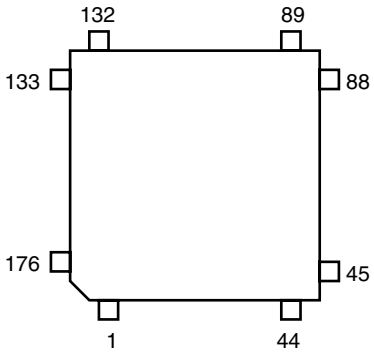
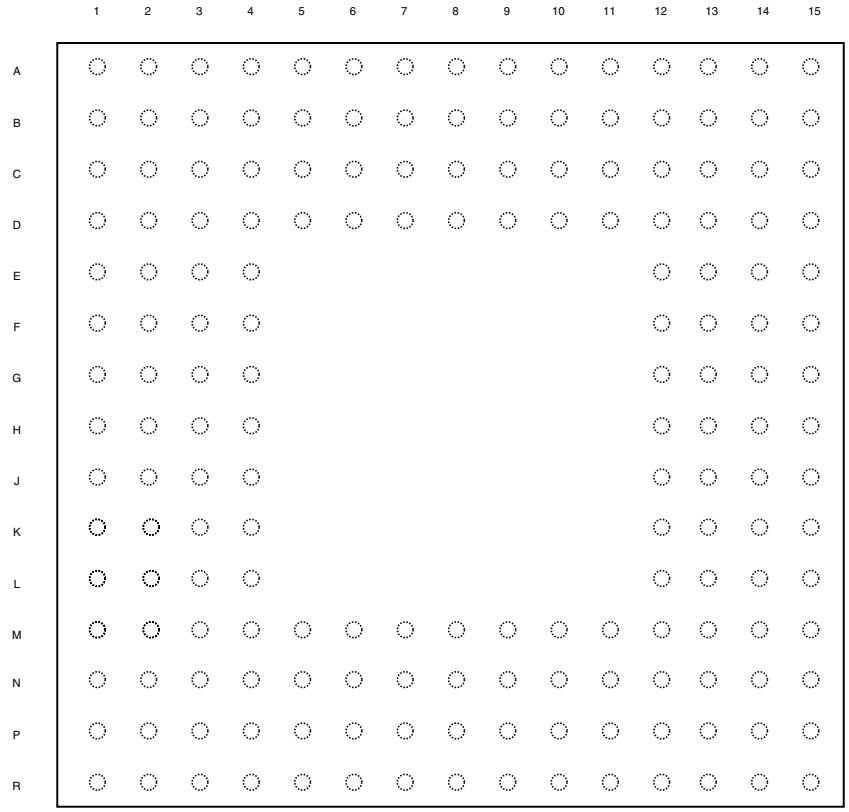


Figure 2-2. 176-ball BGA Pinout



3. Pin Description

Table 3-1. Pin Description

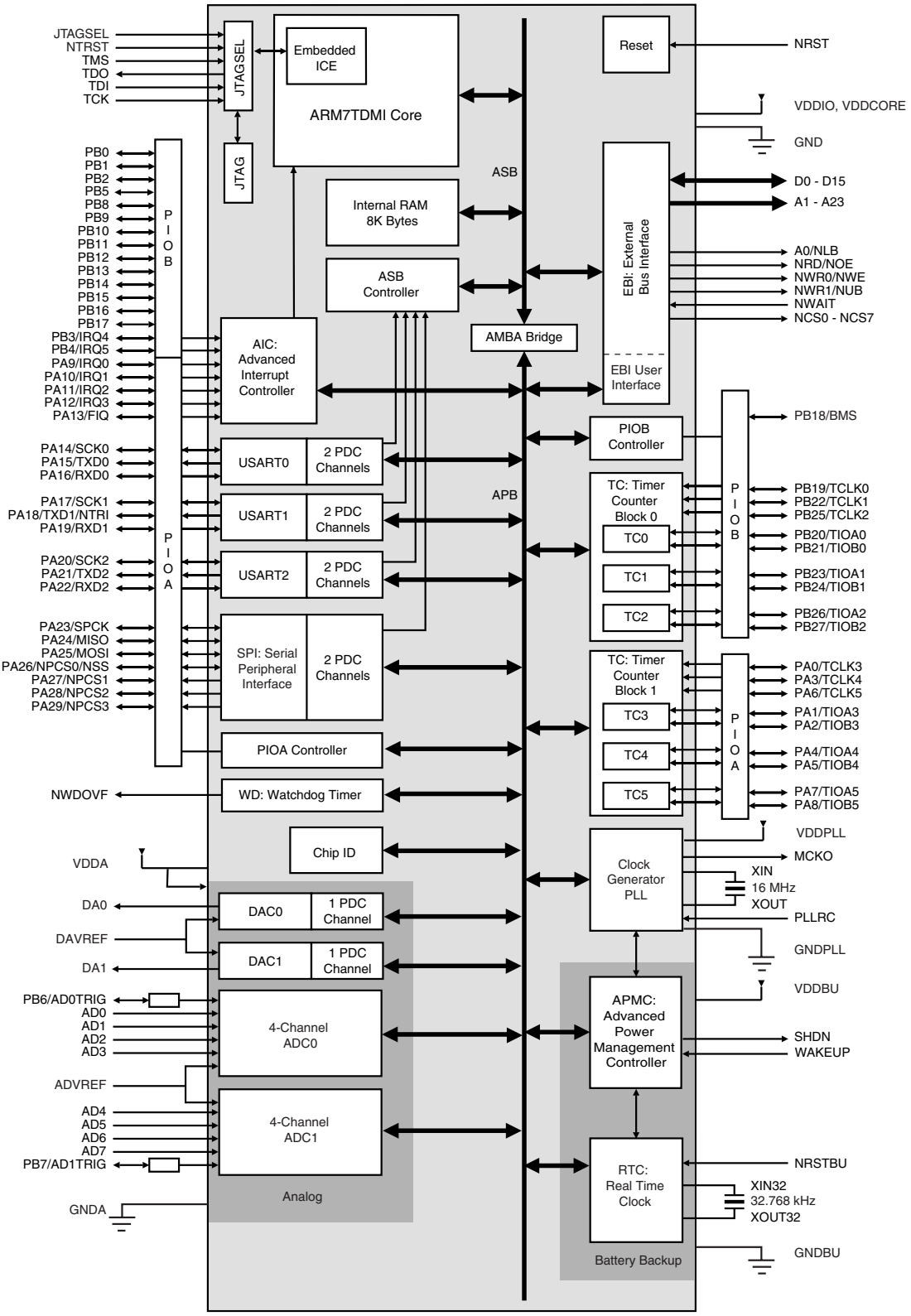
Module	Name	Function	Type	Active Level	Comments
EBI	A0 - A23	Address bus	Output	–	
	D0 - D15	Data bus	I/O	–	
	NCS0 - NCS7	Chip select	Output	Low	
	NWR0	Lower byte 0 write signal	Output	Low	Used in Byte-write option
	NWR1	Lower byte 1 write signal	Output	Low	Used in Byte-write option
	NRD	Read signal	Output	Low	Used in Byte-write option
	NWE	Write enable	Output	Low	Used in Byte-select option
	NOE	Output enable	Output	Low	Used in Byte-select option
	NUB	Upper byte-select	Output	Low	Used in Byte-select option
	NLB	Lower byte-select	Output	Low	Used in Byte-select option
	NWAIT	Wait input	Input	Low	
	BMS	Boot mode select	Input	–	Sampled during reset
AIC	IRQ0 - IRQ5	External interrupt request	Input	–	PIO-controlled after reset
	FIQ	Fast external interrupt request	Input	–	PIO-controlled after reset
Timer	TCLK0 - TCLK5	Timer external clock	Input	–	PIO-controlled after reset
	TIOA0 - TIOA5	Multipurpose timer I/O pin A	I/O	–	PIO-controlled after reset
	TIOB0 - TIOB5	Multipurpose timer I/O pin B	I/O	–	PIO-controlled after reset
USART	SCK0 - SCK2	External serial clock	I/O	–	PIO-controlled after reset
	TXD0 - TXD2	Transmit data output	Output	–	PIO-controlled after reset
	RXD0 - RXD2	Receive data input	Input	–	PIO-controlled after reset
SPI	SPCK	SPI clock	I/O	–	PIO-controlled after reset
	MISO	Master in slave out	I/O	–	PIO-controlled after reset
	MOSI	Master out slave in	I/O	–	PIO-controlled after reset
	NSS	Slave select	Input	Low	PIO-controlled after reset
	NPCS0 - NPCS3	Peripheral chip select	Output	Low	PIO-controlled after reset
PIO	PA0 - PA29	Parallel I/O port A	I/O	–	Input after reset
	PB0 - PB27	Parallel I/O port B	I/O	–	Input after reset
WD	NWDOVF	Watchdog timer overflow	Output	Low	Open drain
ADC	AD0 - AD7	Analog input channels 0 - 7	Analog in	–	
	AD0TRIG	ADC0 external trigger	Input	–	PIO-controlled after reset
	AD1TRIG	ADC1 external trigger	Input	–	PIO-controlled after reset
	ADVREF	Analog reference	Analog ref	–	

Table 3-1. Pin Description (Continued)

Module	Name	Function	Type	Active Level	Comments
DAC	DA0 - DA1	Analog output channels 0 - 1	Analog out	–	
	DAVREF	Analog reference	Analog ref	–	
Clock	XIN	Main oscillator input	Input	–	
	XOUT	Main oscillator output	Output	–	
	PLLRC	RC filter for PLL	Input	–	
	XIN32	32 kHz oscillator input	Input	–	
	XOUT32	32 kHz oscillator output	Output	–	
	MCKO	System clock	Output	–	
APMC	WAKEUP	Wakeup request	Input	–	
	SHDN	Shutdown request	Output	–	Tri-state after backup reset
Reset	NRST	Hardware reset input	Input	Low	Schmidt trigger
	NRSTBU	Hardware reset input for battery part	Input	Low	Schmidt trigger
	NTRI	Tri-state mode select	Input	Low	Sampled during reset
JTAG/ICE	JTAGSEL	Selects between ICE and JTAG mode	Input	–	
	TMS	Test mode select	Input	–	Schmidt trigger, internal pull-up
	TDI	Test data input	Input	–	Schmidt trigger, internal pull-up
	TDO	Test data output	Output	–	
	TCK	Test clock	Input	–	Schmidt trigger, internal pull-up
	NTRST	Test reset input	Input	Low	Schmidt trigger, internal pull-up
Power	VDDA	Analog power	Analog pwr	–	
	GNDA	Analog ground	Analog gnd	–	
	VDDBU	Power backup	Power	–	
	GNDBU	Ground backup	Ground	–	
	VDDCORE	Digital core power	Power	–	
	VDDIO	Digital I/O power	Power	–	
	VDDPLL	Main oscillator and PLL power	Power	–	
	GND	Digital ground	Ground	–	
	GNDPLL	PLL ground	Ground	–	

4. Block Diagram

Figure 4-1. AT91M55800A



5. Architectural Overview

The AT91M55800A microcontroller integrates an ARM7TDMI with its EmbeddedICE interface, memories and peripherals. Its architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). Designed for maximum performance and controlled by the memory controller, the ASB interfaces the ARM7TDMI processor with the on-chip 32-bit memories, the External Bus Interface (EBI) and the AMBA™ Bridge. The AMBA Bridge drives the APB, which is designed for accesses to on-chip peripherals and optimized for low power consumption.

The AT91M55800A microcontroller implements the ICE port of the ARM7TDMI processor on dedicated pins, offering a complete, low cost and easy-to-use debug solution for target debugging.

5.1 Memory

The AT91M55800A microcontroller embeds 8K bytes of internal SRAM. The internal memory is directly connected to the 32-bit data bus and is single-cycle accessible.

The AT91M55800A microcontroller features an External Bus Interface (EBI), which enables connection of external memories and application-specific peripherals. The EBI supports 8- or 16-bit devices and can use two 8-bit devices to emulate a single 16-bit device. The EBI implements the early read protocol, enabling faster memory accesses than standard memory interfaces.

5.2 Peripherals

The AT91M55800A microcontroller integrates several peripherals, which are classified as system or user peripherals. All on-chip peripherals are 32-bit accessible by the AMBA Bridge, and can be programmed with a minimum number of instructions. The peripheral register set is composed of control, mode, data, status and enable/disable/status registers.

An on-chip, 8-channel Peripheral Data Controller (PDC) transfers data between the on-chip USARTs/SPI and the on and off-chip memories without processor intervention. One PDC channel is connected to the receiving channel and one to the transmitting channel of each USART and of the SPI.

Most importantly, the PDC removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64K contiguous bytes. As a result, the performance of the microcontroller is increased and the power consumption reduced.

5.2.1 System Peripherals

The External Bus Interface (EBI) controls the external memory and peripheral devices via an 8- or 16-bit data bus and is programmed through the APB. Each chip select line has its own programming register.

The Advanced Power Management Controller (APMC) optimizes power consumption of the product by controlling the clocking elements such as the oscillators and the PLL, system and user peripheral clocks, and the power supplies.

The Advanced Interrupt Controller (AIC) controls the internal interrupt sources from the internal peripherals and the eight external interrupt lines (including the FIQ), to provide an interrupt and/or fast interrupt request to the ARM7TDMI. It integrates an 8-level priority controller and, using the auto-vectoring feature, reduces the interrupt latency time.

The Real-time Clock (RTC) peripheral is designed for very low power consumption, and combines a complete time-of-day clock with alarm and a two-hundred year Gregorian calendar, complemented by a programmable periodic interrupt.

The Parallel Input/Output Controllers (PIOA and PIOB) control the 58 I/O lines. They enable the user to select specific pins for on-chip peripheral input/output functions, and general-purpose input/output signal pins. The PIO controllers can be programmed to detect an interrupt on a signal change from each line.

The Watchdog (WD) can be used to prevent system lock-up if the software becomes trapped in a deadlock.

The Special Function (SF) module integrates the Chip ID and Reset Status registers.

5.2.2 User Peripherals

Three USARTs, independently configurable, enable communication at a high baud rate in synchronous or asynchronous mode. The format includes start, stop and parity bits and up to 8 data bits. Each USART also features a Timeout and a Time Guard Register, facilitating the use of the two dedicated Peripheral Data Controller (PDC) channels.

The six 16-bit Timer/Counters (TC) are highly programmable and support capture or waveform modes. Each TC channel can be programmed to measure or generate different kinds of waves, and can detect and control two input/output signals. Each TC also has three external clock signals.

The SPI provides communication with external devices in master or slave mode. It has four external chip selects which can be connected to up to 15 devices. The data length is programmable, from 8- to 16-bit.

The two identical 4-channel 10-bit analog-to-digital converters (ADC) are based on a Successive Approximation Register (SAR) approach.

The two identical single-channel 10-bit digital-to-analog converters (DAC).

6. Associated Documentation

Table 6-1. Associated Documentation

Product	Information	Document Title	Literature Number
AT91M55800A	Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM7TDMI (Thumb) Datasheet	0673
	External memory interface mapping Peripheral operations Peripheral user interfaces Ordering information Packaging information Soldering profile Errata	AT91M55800A Datasheet	1745
	DC Characteristics Power consumption Thermal and reliability considerations AC characteristics	AT91M55800A Electrical Characteristics	1727
	Product overview Ordering information Packaging information Soldering profile	AT91M55800A Summary Datasheet (this document)	1745S

7. Product Overview

7.1 Power Supplies

The AT91M55800A has 5 kinds of power supply pins:

- VDDCORE pins, which power the chip core
- VDDIO pins, which power the I/O Lines
- VDDPLL pins, which power the oscillator and PLL cells
- VDDA pins, which power the analog peripherals ADC and DAC
- VDDBU pins, which power the RTC, the 32768 Hz oscillator and the Shut-down Logic of the APMC

VDDIO and VDDCORE are separated to permit the I/O lines to be powered with 5V, thus resulting in full TTL compliance.

The following ground pins are provided:

- GND for both VDDCORE and VDDIO
- GNDPLL for VDDPLL
- GNDA for VDDA
- GNDBU for VDDBU

All of these ground pins must be connected to the same voltage (generally the board electric ground) with wires as short as possible. GNDPLL, GNDA and GNDBU are provided separately in order to allow the user to add a decoupling capacitor directly between the power and ground pads. In the same way, the PLL filter resistor and capacitors must be connected to the device and to GNDBU with wires as short as possible. Also, the external load capacitances of the main oscillator crystal and the 32768 Hz crystal must be connected respectively to GNDPLL and to GNDBU with wires as short as possible.

The main constraints applying to the different voltages of the device are:

- VDDBU must be lower than or equal to VDDCORE
- VDDA must be higher than or equal to VDDCORE
- VDDCORE must be lower than or equal to VDDIO

The nominal power combinations supported by the AT91M55800A are described in the following table:

Table 7-1. Nominal Power Combinations

VDDIO	VDDCORE	VDDA	VDDPLL	VDDBU	Maximum Operating Frequency
3V	3V	3V	3V	3V	33 MHz
3.3V	3.3V	3.3V	3.3V	3.3V	33 MHz
5V	3.3V	3.3V	3.3V	3.3V	33 MHz

7.2 Input/Output Considerations

After the reset, the peripheral I/Os are initialized as inputs to provide the user with maximum flexibility. It is recommended that in any application phase, the inputs to the AT91M55800A microcontroller be held at valid logic levels to minimize the power consumption.

7.3 Master Clock

Master Clock is generated in one of the following ways, depending on programming in the APMC registers:

- From the 32768 Hz low-power oscillator that clocks the RTC
- The on-chip main oscillator, together with a PLL, generate a software-programmable main clock in the 500 Hz to 33 MHz range. The main oscillator can be bypassed to allow the user to enter an external clock signal.

The Master Clock (MCK) is also provided as an output of the device on the MCKO pin, whose state is controlled by the APMC module.

7.4 Reset

Reset restores the default states of the user interface registers (defined in the user interface of each peripheral), and forces the ARM7TDMI to perform the next instruction fetch from address zero. Aside from the program counter, the ARM7TDMI registers do not have defined reset states.

7.4.1 NRST Pin

NRST is active low-level input. It is asserted asynchronously, but exit from reset is synchronized internally to the MCK. At reset, the source of MCK is the Slow Clock (32768 Hz crystal), and the signal presented on MCK must be active within the specification for a minimum of 10 clock cycles up to the rising edge of NRST, to ensure correct operation.

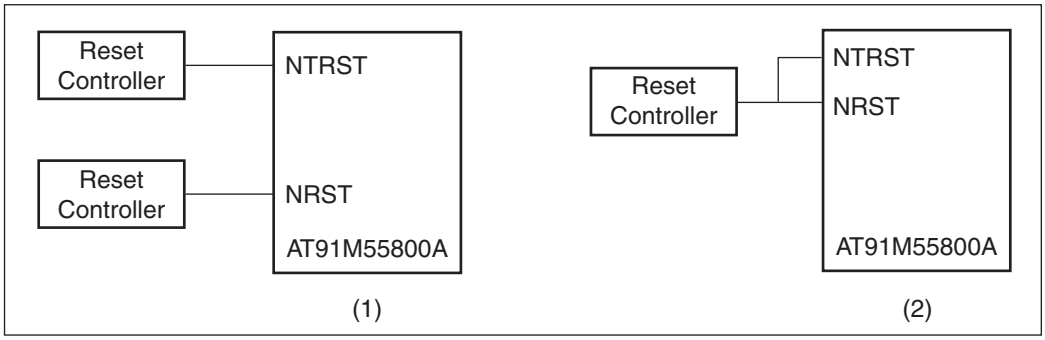
7.4.2 NTRST Pin

Test Access Port (TAP) reset functionality is provided through the NTRST signal.

The NTRST control pin initializes the selected TAP controller. The TAP controller involved in this reset is determined according to the initial logical state applied on the JTAGSEL pin after the last valid NRST.

In either Boundary Scan or ICE Mode a reset can be performed from the same or different circuitry, as shown in Figure 7-1 below. But in all cases, the NTRST like the NRST signal, must be asserted after each power-up. (See the AT91M55800A electrical datasheet, Atmel lit° 1727, for the necessary minimum pulse assertion time.)

Figure 7-1. Separate or Common Reset Management



Notes: 1. NRST and NTRST handling in Debug Mode during development.
2. NRST and NTRST handling during production.

In order to benefit the most regarding the separation of NRST and NTRST during the Debug phase of development, the user must independently manage both signals as shown in example (1) of Figure 7-1 above. However, once Debug is completed, both signals are easily managed together during production as shown in example (2) of Figure 7-1 above.

7.4.3 Watchdog Reset

The watchdog can be programmed to generate an internal reset. In this case, the reset has the same effect as the NRST pin assertion, but the BMS and NTRI pins are not sampled. Boot Mode and Tri-state Mode are not updated. If the NRST pin is asserted and the watchdog triggers the internal reset, the NRST pin has priority.

7.5 Emulation Functions

7.5.1 Tri-state Mode

The AT91M55800A provides a Tri-state Mode, which is used for debug purposes. This enables the connection of an emulator probe to an application board without having to desolder the device from the target board. In Tri-state Mode, all the output pin drivers of the AT91M55800A microcontroller are disabled.

To enter Tri-state Mode, the NTRI pin must be held low during the last 10 clock cycles before the rising edge of NRST. For normal operation the NTRI pin must be held high during reset, by a resistor of up to 400K Ohm.

NTRI is multiplexed with I/O line PA18 and USART 1 serial data transmit line TXD1.

Standard RS232 drivers generally contain internal 400K Ohm pull-up resistors. If TXD1 is connected to a device not including this pull-up, the user must make sure that a high level is tied on NTRI while NRST is asserted.

7.5.2 JTAG/ICE Debug Mode

ARM Standard Embedded In-Circuit Emulation is supported via the JTAG/ICE port. It is connected to a host computer via an external ICE Interface. The JTAG/ICE debug mode is enabled when JTAGSEL is low.

In ICE Debug Mode the ARM Core responds with a non-JTAG chip ID which identifies the core to the ICE system. This is not JTAG compliant.

7.5.3 IEEE 1149.1 JTAG Boundary-scan

JTAG Boundary-scan is enabled when JTAGSEL is high. The functions SAMPLE, EXTEST and BYPASS are implemented. There is no JTAG chip ID. The Special Function module provides a chip ID which is independent of JTAG.

It is not possible to switch directly between JTAG and ICE operations. A chip reset must be performed (NRST and NTRST) after JTAGSEL is changed.

7.6 Memory Controller

The ARM7TDMI processor address space is 4G bytes. The memory controller decodes the internal 32-bit address bus and defines three address spaces:

- Internal memories in the four lowest megabytes
- Middle space reserved for the external devices (memory or peripherals) controlled by the EBI

- Internal peripherals in the four highest megabytes

In any of these address spaces, the ARM7TDMI operates in Little-Endian mode only.

7.6.1 Internal Memories

The AT91M55800A microcontroller integrates an 8-Kbyte primary SRAM bank. This memory bank is mapped at address 0x0 (after the remap command), allowing ARM7TDMI exception vectors between 0x0 and 0x20 to be modified by the software. The rest of the bank can be used for stack allocation (to speed up context saving and restoring), or as data and program storage for critical algorithms. All internal memory is 32 bits wide and single-clock cycle accessible. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one cycle. Fetching Thumb or ARM instructions is supported and internal memory can store twice as many Thumb instructions as ARM ones.

7.6.2 Boot Mode Select

The ARM reset vector is at address 0x0. After the NRST line is released, the ARM7TDMI executes the instruction stored at this address. This means that this address must be mapped in nonvolatile memory after the reset.

The input level on the BMS pin during the last 10 clock cycles before the rising edge of the NRST selects the type of boot memory (see Table 5).

The BMS pin is multiplexed with the I/O line PB18 that can be programmed after reset like any standard PIO line.

Table 7-2. Boot Mode Select

BMS	Boot Mode
1	External 8-bit memory on NCS0
0	External 16-bit memory on NCS0

7.6.3 Remap Command

The ARM vectors (Reset, Abort, Data Abort, Prefetch Abort, Undefined Instruction, Interrupt, Fast Interrupt) are mapped from address 0x0 to address 0x20. In order to allow these vectors to be redefined dynamically by the software, the AT91M55800A microcontroller uses a remap command that enables switching between the boot memory and the internal RAM bank addresses. The remap command is accessible through the EBI User Interface, by writing one in RCB of EBI_RCR (Remap Control Register). Performing a remap command is mandatory if access to the other external devices (connected to chip selects 1 to 7) is required. The remap operation can only be changed back by an internal reset or an NRST assertion.

7.6.4 Abort Control

The abort signal providing a Data Abort or a Prefetch Abort exception to the ARM7TDMI is asserted when accessing an undefined address in the EBI address space.

No abort is generated when reading the internal memory or by accessing the internal peripherals, whether the address is defined or not.

7.6.5 External Bus Interface

The External Bus Interface handles the accesses between addresses 0x0040 0000 and 0xFFC0 0000. It generates the signals that control access to the external devices, and can

configure up to eight 16-Mbyte banks. In all cases it supports byte, half-word and word aligned accesses.

For each of these banks, the user can program:

- Number of wait states
- Number of data float times (wait time after the access is finished to prevent any bus contention in case the device is too long in releasing the bus)
- Data bus width (8-bit or 16-bit)
- With a 16-bit wide data bus, the user can program the EBI to control one 16-bit device (Byte Access Select Mode) or two 8-bit devices in parallel that emulate a 16-bit memory (Byte-write Access mode).

The External Bus Interface features also the Early Read Protocol, configurable for all the devices, that significantly reduces access time requirements on an external device.

8. Peripherals

The AT91M55800A peripherals are connected to the 32-bit wide Advanced Peripheral Bus. Peripheral registers are only word accessible. Byte and half-word accesses are not supported. If a byte or a half-word access is attempted, the memory controller automatically masks the lowest address bits and generates a word access.

Each peripheral has a 16-Kbyte address space allocated (the AIC only has a 4-Kbyte address space).

8.0.1 Peripheral Registers

The following registers are common to all peripherals:

- Control Register – write only register that triggers a command when a one is written to the corresponding position at the appropriate address. Writing a zero has no effect.
- Mode Register – read/write register that defines the configuration of the peripheral. Usually has a value of 0x0 after a reset.
- Data Registers – read and/or write register that enables the exchange of data between the processor and the peripheral.
- Status Register – read only register that returns the status of the peripheral.
- Enable/Disable/Status Registers – shadow command registers. Writing a one in the Enable Register sets the corresponding bit in the Status Register. Writing a one in the Disable Register resets the corresponding bit and the result can be read in the Status Register. Writing a bit to zero has no effect. This register access method maximizes the efficiency of bit manipulation, and enables modification of a register with a single non-interruptible instruction, replacing the costly read-modify-write operation.

Unused bits in the peripheral registers are shown as "–" and must be written at 0 for upward compatibility. These bits read 0.

8.0.2 Peripheral Interrupt Control

The Interrupt Control of each peripheral is controlled from the status register using the interrupt mask. The status register bits are ANDed to their corresponding interrupt mask bits and the result is then ORed to generate the Interrupt Source signal to the Advanced Interrupt Controller.

The interrupt mask is read in the Interrupt Mask Register and is modified with the Interrupt Enable Register and the Interrupt Disable Register. The enable/disable/status (or mask) makes it possible to enable or disable peripheral interrupt sources with a non-interruptible single instruction. This eliminates the need for interrupt masking at the AIC or Core level in real-time and multi-tasking systems.

8.0.3 Peripheral Data Controller

An on-chip, 8-channel Peripheral Data Controller (PDC) transfers data between the on-chip USARTs/SPI/DACs and the on and off-chip memories without processor intervention. One PDC channel is connected to the receiving channel and one to the transmitting channel of each USART and SPI.

The user interface of a PDC channel is integrated in the memory space of each peripheral. It contains a 32-bit address pointer register and a 16-bit count register. When the programmed data is transferred, an end of transfer interrupt is generated by the corresponding peripheral.

Most importantly, the PDC removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64K contiguous bytes. As a result, the performance of the microcontroller is increased and the power consumption reduced.

8.1 System Peripherals

8.1.1 APMC: Advanced Power Management Controller

The AT91M55800A Advanced Power Management Controller allows optimization of power consumption. The APMC enables/disables the clock inputs of most of the peripherals and the ARM core. Moreover, the main oscillator, the PLL and the analog peripherals can be put in standby mode allowing minimum power consumption to be obtained. The APMC provides the following operating modes:

- Normal mode: clock generator provides clock to the entire chip except the RTC.
- Wait mode: ARM core clock deactivated
- Slow Clock mode: clock generator deactivated, master clock 32 kHz
- Standby mode: RTC active, all other clocks disabled
- Power-down mode: RTC active, supply on the rest of the circuit deactivated

8.1.2 RTC: Real Time Clock

The AT91M55800A features a Real-time Clock (RTC) peripheral that is designed for very low power consumption. It combines a complete time-of-day clock with alarm and a two-hundred year Gregorian calendar, complemented by a programmable periodic interrupt.

The time and calendar values are coded in Binary-Coded Decimal (BCD) format. The time format can be 24-hour mode or 12-hour mode with an AM/PM indicator.

Updating time and calendar fields and configuring the alarm fields is performed by a parallel capture on the 32-bit data bus. An entry control is performed to avoid loading registers with incompatible BCD format data or with an incompatible date according to the current month/year/century.

8.1.3 AIC: Advanced Interrupt Controller

The AIC has an 8-level priority, individually maskable, vectored interrupt controller, and drives the NIRQ and NFIQ pins of the ARM7TDMI from:

- The external fast interrupt line (FIQ)
- The six external interrupt request lines (IRQ0 - IRQ5)
- The interrupt signals from the on-chip peripherals

The AIC is largely programmable offering maximum flexibility, and its vectoring features reduce the real-time overhead in handling interrupts.

The AIC also features a spurious vector, which reduces spurious interrupt handling to a minimum, and a protect mode that facilitates the debug capabilities.

8.1.4 PIO: Parallel I/O Controller

The AT91M55800A has 58 programmable I/O lines. 13 pins are dedicated as general-purpose I/O pins. The other I/O lines are multiplexed with an external signal of a peripheral to optimize the use of available package pins. The PIO lines are controlled by two separate and identical

PIO Controllers called PIOA and PIOB. The PIO controller enables the generation of an interrupt on input change and insertion of a simple input glitch filter on any of the PIO pins.

8.1.5 WD: Watchdog

The Watchdog is built around a 16-bit counter, and is used to prevent system lock-up if the software becomes trapped in a deadlock. It can generate an internal reset or interrupt, or assert an active level on the dedicated pin NWDOVF. All programming registers are password-protected to prevent unintentional programming.

8.1.6 SF: Special Function

The AT91M55800A provides registers which implement the following special functions.

- Chip identification
- RESET status

8.2 User Peripherals

8.2.1 USART: Universal Synchronous/ Asynchronous Receiver Transmitter

The AT91M55800A provides three identical, full-duplex, universal synchronous/asynchronous receiver/transmitters.

Each USART has its own baud rate generator, and two dedicated Peripheral Data Controller channels. The data format includes a start bit, up to 8 data bits, an optional programmable parity bit and up to 2 stop bits.

The USART also features a Receiver Timeout register, facilitating variable-length frame support when it is working with the PDC, and a Time-guard register, used when interfacing with slow remote equipment.

8.2.2 TC: Timer/Counter

The AT91M55800A features two Timer/Counter blocks that include three identical 16-bit timer/counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse-width modulation.

The Timer/Counters can be used in Capture or Waveform mode, and all three counter channels can be started simultaneously and chained together.

8.2.3 SPI: Serial Peripheral Interface

The SPI provides communication with external devices in master or slave mode. It has four external chip selects that can be connected to up to 15 devices. The data length is programmable, from 8- to 16-bit.

8.2.4 ADC: Analog-to-digital Converter

The two identical 4-channel 10-bit analog-to-digital converters (ADC) are based on a Successive Approximation Register (SAR) approach.

Each ADC has 4 analog input pins, AD0 to AD3 and AD4 to AD7, digital trigger input AD0TRIG and AD1TRIG pins, and provides an interrupt signal to the AIC. Both ADCs share the analog power supply VDDA and GNDA pins, and the input reference voltage ADVREF pin.

Each channel can be enabled or disabled independently, and has its own data register. The ADC can be configured to automatically enter Sleep Mode after a conversion sequence, and can be triggered by the software, the Timer/Counter, or an external signal.

8.2.5 DAC: Digital-to-analog Converter

Two identical 1-channel 10-bit digital-to-analog converters (DAC).

Each DAC has an analog output pin, DA0 and DA1, and provides an interrupt signal to the AIC DA0IRQ and DA1IRQ. Both DACs share the analog power supply VDDA and GNDA pins, and the input reference DAVREF.

9. Packaging Information

Figure 9-1. 176-lead Thin Quad Flat Pack Package Drawing

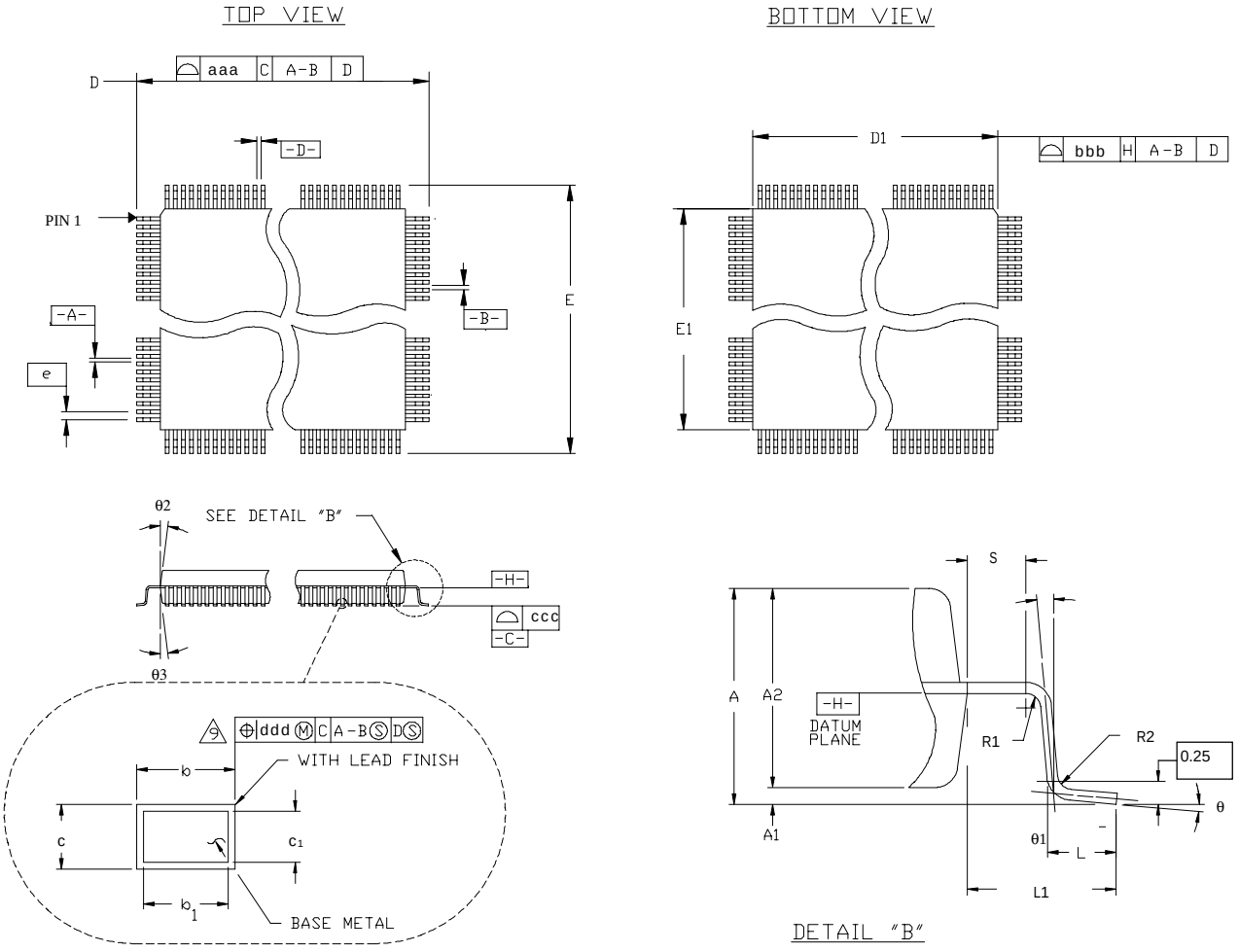


Table 9-1. Common Dimensions (mm)

Symbol	Min	Nom	Max
c	0.09		0.20
c1	0.09		0.16
L	0.45	0.6	0.75
L1		1.00 REF	
R2	0.08		0.2
R1	0.08		
S	0.2		
q	0°	3.5°	7°
θ1	0°		
θ2	11°	12°	13°
θ3	11°	12°	13°
A			1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
Tolerances of form and position			
aaa		0.2	
bbb		0.2	

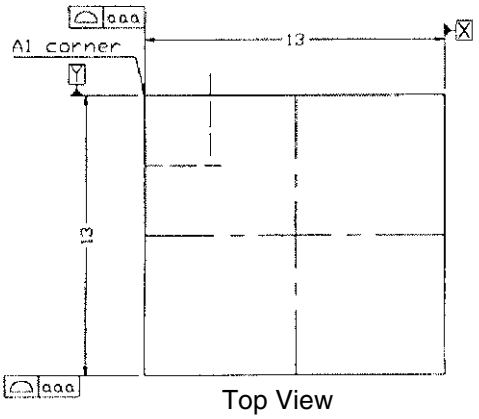
Table 9-2. Lead Count Dimensions (mm)

Pin Count	D/E BSC	D1/E1 BSC	b			b1			e BSC	ccc	ddd
			Min	Nom	Max	Min	Nom	Max			
176	26.0	24.0	0.17	0.20	0.27	0.17	0.20	0.23	0.50	0.10	0.08

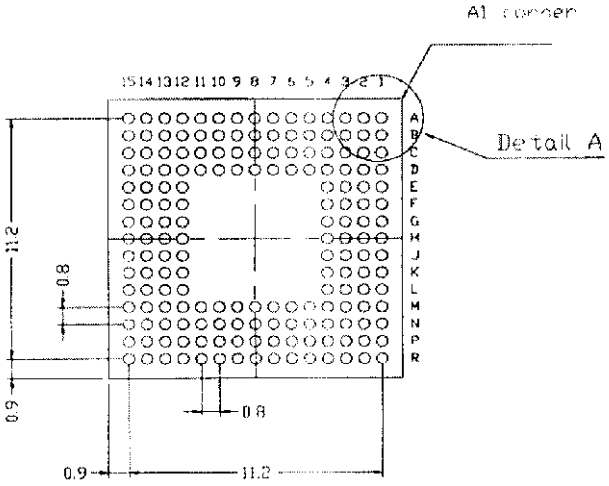
Table 9-3. Device and 176-lead LQFP Package Maximum Weight

2023	mg

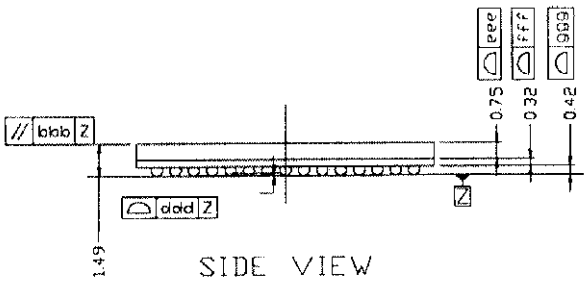
Figure 9-2. 176-ball Ball Grid Array Package Drawing



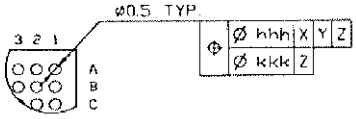
Top View



Bottom View



SIDE VIEW



Detail A

Symbol	Maximum
aaa	0.1
bbb	0.1
ddd	0.1
eee	0.03
fff	0.04
ggg	0.03
hhh	0.1
kkk	0.1

Notes:
1. Package dimensions conform to JEDEC MO-205
2. Dimensioning and tolerancing per ASME Y14.5M-1994
3. All dimensions in mm
4. Solder Ball position designation per JESD 95-1, SPP-010
5. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls

Table 9-4. Device and 176-ball BGA Package Maximum Weight

606	mg

10. Soldering Profile

10.1 LQFP Soldering Profile (Green)

Table 10-1 gives the recommended soldering profile from J-STD-020C.

Table 10-1. Soldering Profile Green Compliant Package

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3° C/sec. max.
Preheat Temperature 175°C ±25°C	180 sec. max.
Temperature Maintained Above 217°C	60 sec. to 150 sec.
Time within 5° C of Actual Peak Temperature	20 sec. to 40 sec.
Peak Temperature Range	260 +0 ° C
Ramp-down Rate	6° C/sec. max.
Time 25° C to Peak Temperature	8 min. max.

Note: The package is certified to be backward compatible with Pb/Sn soldering profile.

A maximum of three reflow passes is allowed per component.

10.2 BGA Soldering Profile (RoHS-compliant)

Table 10-2 gives the recommended soldering profile from J-STD-20C.

Table 10-2. Soldering Profile RoHS Compliant Package

Profile Feature	Convection or IR/Convection
Average Ramp-up Rate (183° C to Peak)	3° C/sec. max.
Preheat Temperature 125° C ±25° C	180 sec. max
Temperature Maintained Above 183° C	60 sec. to 150 sec.
Time within 5° C of Actual Peak Temperature	20 sec. to 40 sec.
Peak Temperature Range	260 + 0° C
Ramp-down Rate	6° C/sec.
Time 25° C to Peak Temperature	8 min. max

Note: It is recommended to apply a soldering temperature higher than 250°C.

A maximum of three reflow passes is allowed per component.

11. Ordering Information

Table 11-1. Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT91M55800A-33AU	LQFP 176	Green	Industrial (-40° C to 85° C)
AT91M55800A-33CJ	BGA 176	RoHS-compliant	

Revision History

Doc. Rev	Date	Comments		Change Request Ref.
1745AS	**Jul-01**	First issue		
1745BS	**29-Jan-02**			
		pg. 14	Added information to section Internal Memories	
		pg. 19	Changed Table 7	
		pg. 21	Added Table 10	
		pg. 22	Added Table 11	
		pg. 23	Added section Soldering Profile	
1745CS	**18-Apr-02**			
		pg. 3	Changed Table 2	
		pg. 8	Changed FIgure 3, Block Diagram.	
		pg. 9	Changed “Peripherals” paragraph.	
		pg. 10	Changed “User Peripherals” paragraph.	
		pg. 16	Changed “Peripheral Data Controller” paragraph.	
		pg. 17	Changed “AIC” paragraph.	
		pg. 18	Changed “DAC” paragraph	
		pg. 19	Changed Table 7	
1745DS	**14-Jun-05**			
		Global	New corporate format numbering package reference TQFP changed to LQFP	
		pg. 25	added 10.1 ”Green Package Soldering Profile”	05-330
		pg. 25	added 10.2 ”BGA Soldering Profile (RoHS-compliant)”	
		pg. 26	new package info inserted in 11. ”Ordering Information”	
1745ES	**03-Oct-05**			
		Global	Change in format introduced Chapter numbering with change to table and figure numbering.	1745D
		page 14	Section 7.4.2 ”NTRST Pin” info added Figure 7-1, “Separate or Common Reset Management,” added to chapter	05-452
1745FS	**18-Apr-06**			
		page 25 page 26	10. ”Soldering Profile” Standard Soldering Profile section errased 11. ”Ordering Information” AT91M55800A-33AI LQFP176 Sn/Pb package removed AT91M55800A-33CI BGA 176 Sn/Pb package removed	#2602

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