

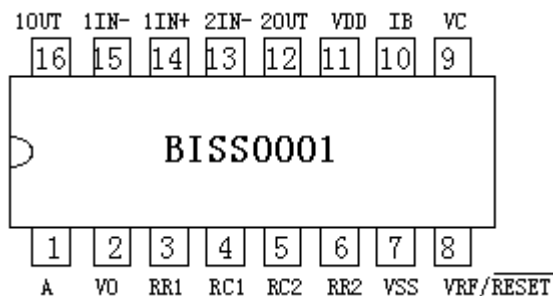
# BISS0001

## Micro Power PIR Motion Detector IC

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### Features

- Low power CMOS technology (ideal for battery operated PIR devices)
- CMOS high input impedance operational amplifiers
- Bi-directional level detector / Excellent noise immunity
- Built-in Power up disable & output pulse control logic
- Dual mode : retriggerable & non-retriggerable



### Pin description

| Pin Number | Symbol      | Description  |
|------------|-------------|--|
| 1          | <b>A</b>    | Retriggerable & non-retriggerable mode select (A=1 : re-triggerable) |
| 2          | <b>VO</b>   | Detector output pin (active high)                                    |
| 3          | <b>RR1</b>  | Output pulse width control (Tx) * See definition below               |
| 4          | <b>RC1</b>  | Output pulse width control (Tx) *                                    |
| 5          | <b>RC2</b>  | Trigger inhibit control (Ti) *                                       |
| 6          | <b>RR2</b>  | Trigger inhibit control (Ti) *                                       |
| 7          | <b>Vss</b>  | Ground   |
| 8          | <b>VRF</b>  | RESET & voltage reference input (Normally high. Low=reset)           |
| 9          | <b>VC</b>   | Trigger disable input (VC >0.2Vdd=enable; Vc<0.2Vdd =disabled)       |
| 10         | <b>IB</b>   | Op-amp input bias current setting                                    |
| 11         | <b>Vdd</b>  | Supply voltage   |
| 12         | <b>2OUT</b> | 2 <sup>nd</sup> stage Op-amp output                                  |
| 13         | <b>2IN-</b> | 2 <sup>nd</sup> stage Op-amp inverting input                         |
| 14         | <b>1IN+</b> | 1 st stage Op-amp non-inverting input                                |
| 15         | <b>1IN-</b> | 1 st stage Op-amp inverting input                                    |
| 16         | <b>1OUT</b> | 1 st stage Op-amp output   |

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Tx = The time duration during which the output pin (Vo) remains high after triggering.

Ti = During this time period, triggering is inhibited. See timing charts for details.

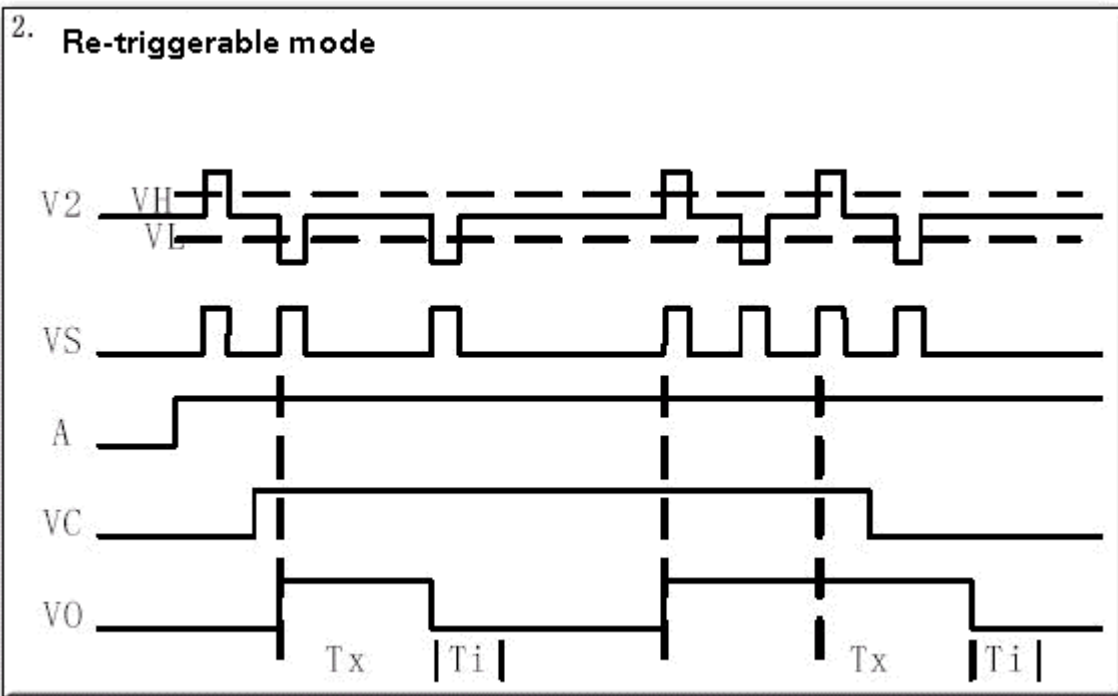
**Tx** ≈ 24576 x R10 x C6;     **Ti** ≈ 24 x R9 x C7。 (ref to schematic)

## Absolute max. ratings

| Description           | Condition   | Range                        | Unit |
|-----------------------|-------------|------------------------------|------|
| Supply voltage        | --          | 3 ~ 5                        | V    |
| Input voltage         | --          | $V_{SS}-0.3 \sim V_{DD}+0.3$ | V    |
| Output current        | $V_{DD}=5V$ | 10                           | mA   |
| Operating temperature | --          | -20 ~ +70                    | °C   |
| Storage temperature   | --          | -40 ~ +125                   | °C   |

## Retrigerrable waveform

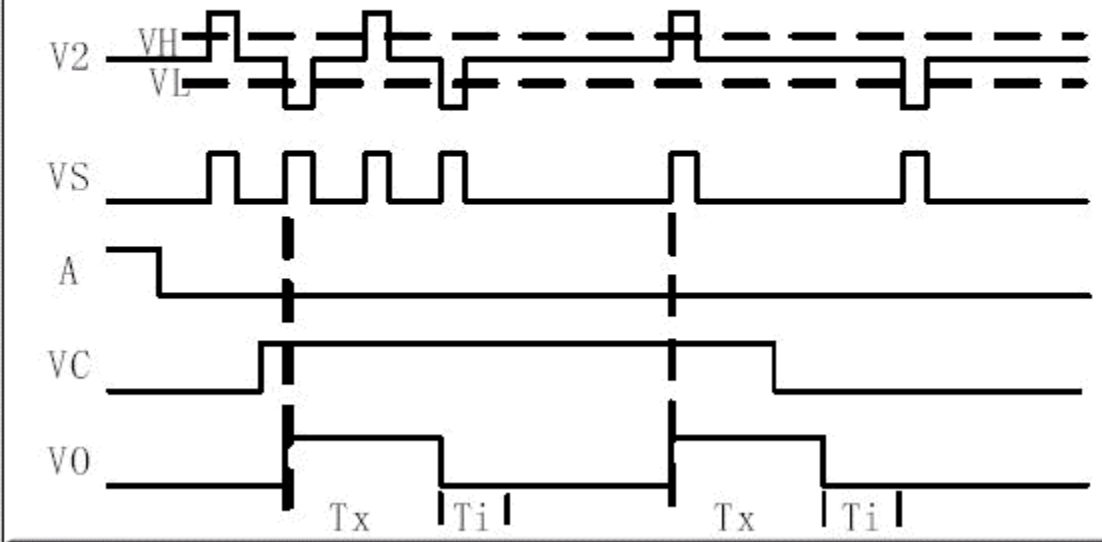
(NOTE :  $V_H=0.7V_{DD}$ ,  $V_L=0.3V_{DD}$ )



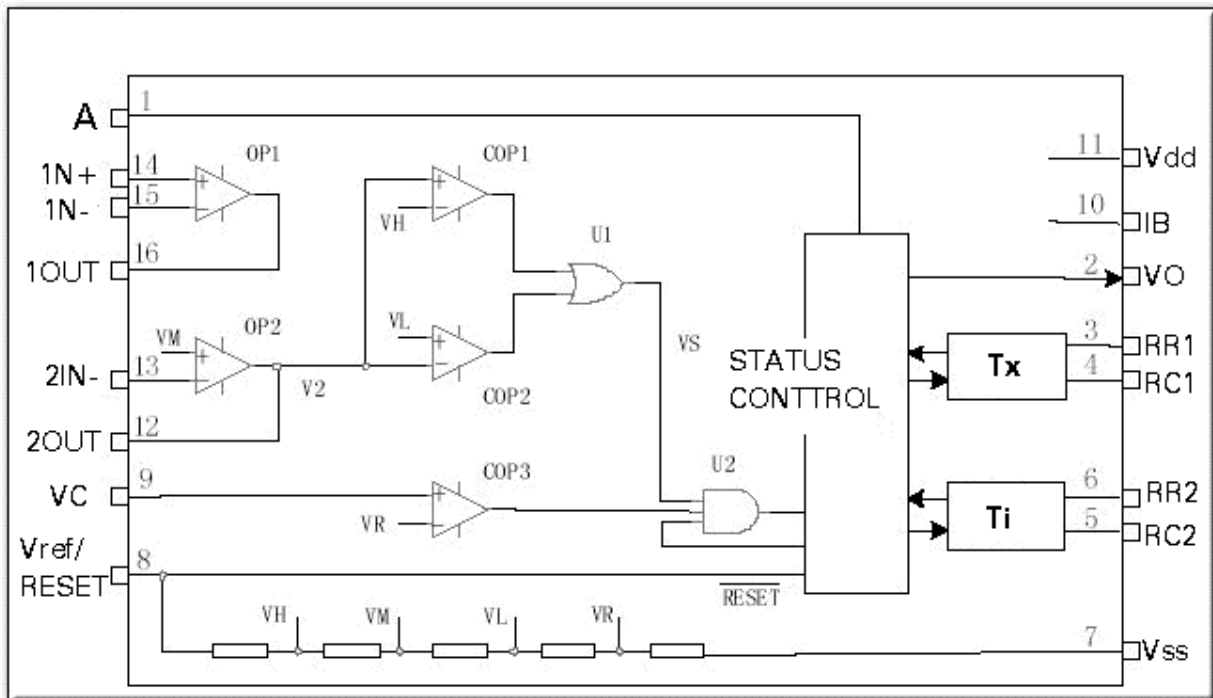
# Non-retriggerable waveform

(NOTE :  $V_H=0.7V_{dd}$ ,  $V_L=0.3V_{dd}$ )

## 1. NON-retriggerable mode



## Internal Block Diagram

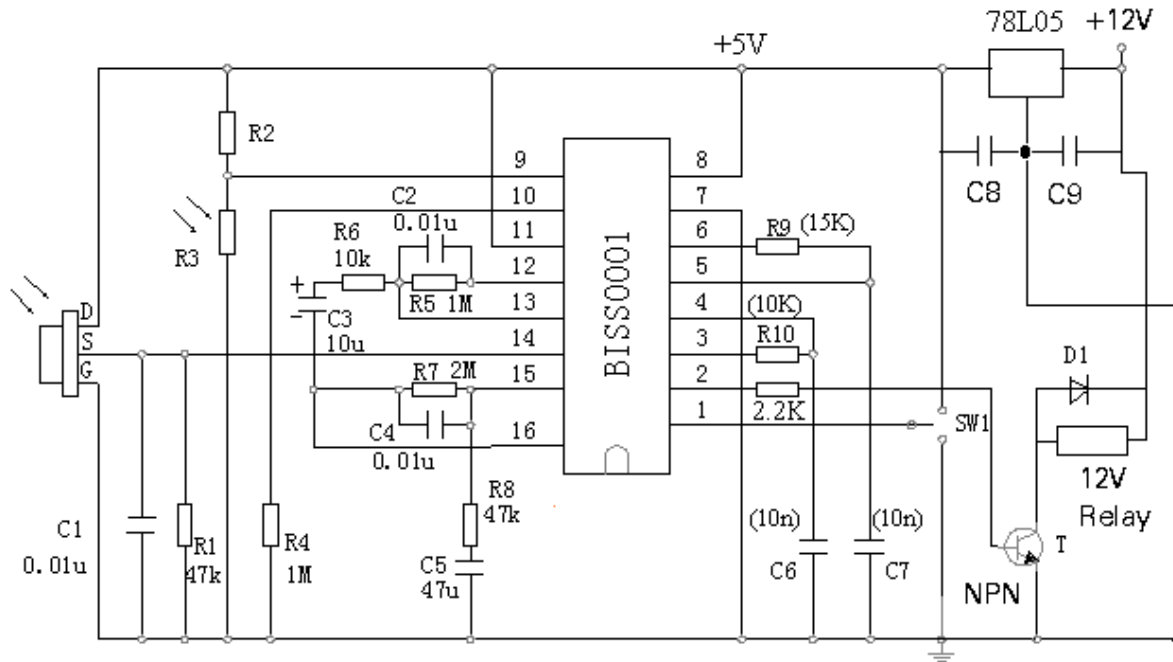


**Tx** - Output pulse width control

**Ti** - Trigger inhibit timing control

## Application Example

### -- Passive Infrared Detector for alarm system



$T_x \approx 24576 \times R_{10} \times C_6$  ;  $T_i \approx 24 \times R_9 \times C_7$  . (ref to schematic)

**R3** is a light dependent resistor which has low resistance under strong ambient light. This causes the detector to be operational only when the detection area is sufficiently dark.