TechNexion

September 2nd 2011

TDM-3730

BASEBOARD DESIGN AND LAYOUT GUIDELINES

TechNexion

Baseboard Design and Layout Guidelines

TDM-3730 Baseboard

Design and Layout Guidelines

Rev 090

1 Contents

2 Revision

Revision	Date	Description	Created by
-	-	Preliminary version	TechNexion
090	2011/09/02	First public version	TechNexion

3 Care and Maintenance

3.1 General

Your device is a product of superior design and craftsmanship and should be treated with care. The following suggestions will help you.

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

These suggestions apply equally to your device, battery, charger, or any enhancement. If any device is not working properly, take it to the nearest authorized service facility for service.

3.2 Regulatory Information

Disposal of Waste Equipment by Users in Private Household in the European Union

This symbol on the product or on its packaging indicates that this product must not be disposed of with your other household waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service or the shop where you purchased the product.

We hereby declare that the product is in compliance with the essential requirements and other relevant provisions of European Directive 1999/5/EC (radio equipment and telecommunications terminal equipment Directive).

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The Compliance of RoHS New Requirement

According to the new requirements in directive 2002/95/EC, DecaBDE is added with specification starting by July 1, 2008 as follows:

Cadmium (Cd)	: Under 100ppm
Lead (Pb)	: Under 1000ppm
Mercury (Hg)	: Under 1000ppm
Hexavalent Chromium (Cr6)	: Under 1000ppm
PBB	: Under 1000ppm
PBDE (include DecaBDE)	: Under 1000ppm

Please confirm and send back, thanks.

RoHS Compliance Statement

We aware the change in this directive and our product can meet this new specification as above.

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Company Stamp

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Federal Communications Commission (FCC) Unintentional emitter per FCC Part 15

This device has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio or television reception. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio and television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

■ Reorient or relocate the receiving antenna
■ Increase the separation between the equipment and receiver
■ Connect the equipment to an outlet on a different circuit from that to which the receiver is connected
■ Consult the dealer or an experienced radio/TV technician for help.

WARNING! To reduce the possibility of heat-related injuries or of overheating the computer, do not place the computer directly on your lap or obstruct the computer air vents. Use the computer only on a hard, flat surface. Do not allow another hard surface, such as an adjoining optional printer, or a soft surface, such as pillows or rugs or clothing, to block airflow. Also, do not allow the AC adapter to contact the skin or a soft surface, such as pillows or rugs or clothing, during operation. The computer and the AC adapter comply with the user-accessible surface temperature limits defined by the International Standard for Safety of Information Technology Equipment (IEC 60950).

4 Description

4.1 About this Guideline

This document is intended as a guide for designing a custom baseboard for the TechNexion modular computers or for starting a Custom Design Project with TechNexion.

To get familiar with the module and baseboard system, one can first buy a development kit and test drive the system and test your application software.

This manual provides the basic baseboard design information with the TechNexion modules. The manual is intended for technically qualified personnel and not for general audiences. No warranty of suitability, purpose, or fitness is implied. The information contained within is supplied “as-is” and is subject to change without notice.

One can always check our website (www.technexion.com) for additional product information, mechanical design files, software programming guides, source code software and hardware manuals.

5 Baseboard PCB

5.1 PCB Stackup recommendations

It is recommended to use a 4 layer PCB for the baseboard with a thickness of 1.6 mm and 60 Ohm (Ω) impedance.

5.2 Power and ground planes

The sections below describe typical 2, 4 and 6 layer board stackups. The goal of the 4 layer designs is to keep the signal routing on outer layers, isolated by the power and ground planes. These power and ground planes also serve the purpose of reference planes for the signal traces. The signal traces should run over continuous reference planes when possible. When 2 layer board designs are required, it remains necessary that the signal traces run over continuous reference planes when possible.

5.2.1 2 Layer Stackup

- Top (Layer 1) Signal with ground plane except where noted.
- Bottom (Layer 2) Ground plane and power islands. A limited number of slow speed signals may be routed on the bottom layer.
- Signal traces should be surrounded by ground or ground trace along at least one edge. If ground trace is used, it should be connected to ground plane on this layer and decoupled to ground plane on top layer.
- Decouple ground planes as practical, as shown below in Figure 5-1. This will allow short (direct) return current paths when signal traces are re-referenced to different power island planes.

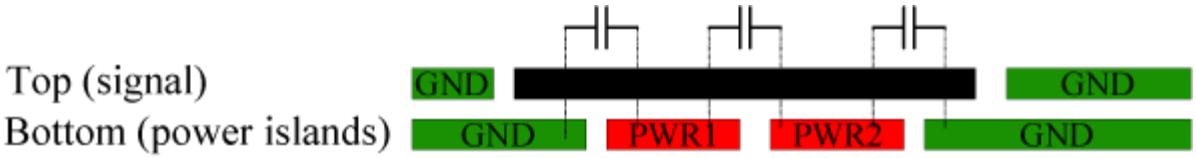


Figure 5-1: Layer Stackup Power and Ground decoupling

5.2.2 4 Layer Stackup

- Top (Layer 1) – Signal with ground plane except where noted.
- Layer 2 – Continuous ground plane. No signals should be routed on this layer.
- Layer 3 – Power planes with ground planes except where noted. Signals may be routed on this layer if needed, especially for buried MII/RMII bus and MII/RMII CLK signals.
- Bottom (Layer 4) – Signal with ground plane except where noted.
- Decouple ground floods and ground layer as practical. When signal traces are re-referenced to power island planes, decoupling capacitors (0.01uF ceramic) are required between the ground plane and power plane.
- Signal traces routed on bottom layer over power islands that are on Layer 3 layer should have decoupling capacitors (0.01uF ceramic) near the trace to enable short (direct) return current paths.

- When signal traces are re-referenced to power island planes, decoupling capacitors (0.01uF ceramic) are required between the ground plane and power plane as shown below in Figure 5-2

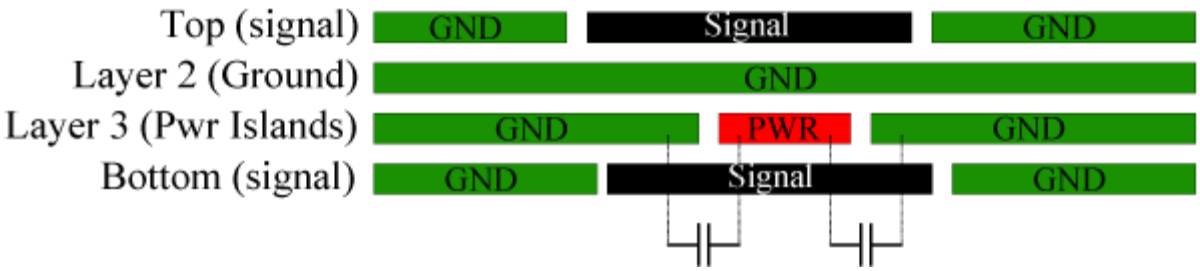


Figure 5-2: Layer stackup Power and Ground Decoupling

5.2.3 6 Layer Stackup

In a few cases 6 layer PCBs are used for complex layouts or to reduce the size of the PCB.

- Top (Layer 1) – Signal with ground plane except where noted.
- Layer 2 – Continuous ground plane. No signals should be routed on this layer.
- Layer 3 –Signals
- Layer 4 - Signals
- Layer 5 – Power planes with ground planes except where noted. Signals may be routed on this layer if needed, especially for buried MII/RMII bus and MII/RMII CLK signals.
- Bottom (Layer 6) – Signal with ground plane except where noted.
- Decouple ground floods and ground layer as practical. When signal traces are re-referenced to power island planes, decoupling capacitors (0.01uF ceramic) are required between the ground plane and power plane.
- Signal traces routed on bottom layer over power islands should have decoupling capacitors (0.01uF ceramic) near the trace to enable short (direct) return current paths.
- When signal traces are re-referenced to power island planes, decoupling capacitors (0.01uF ceramic) are required between the ground plane and power plane as shown below in Figure 5-3

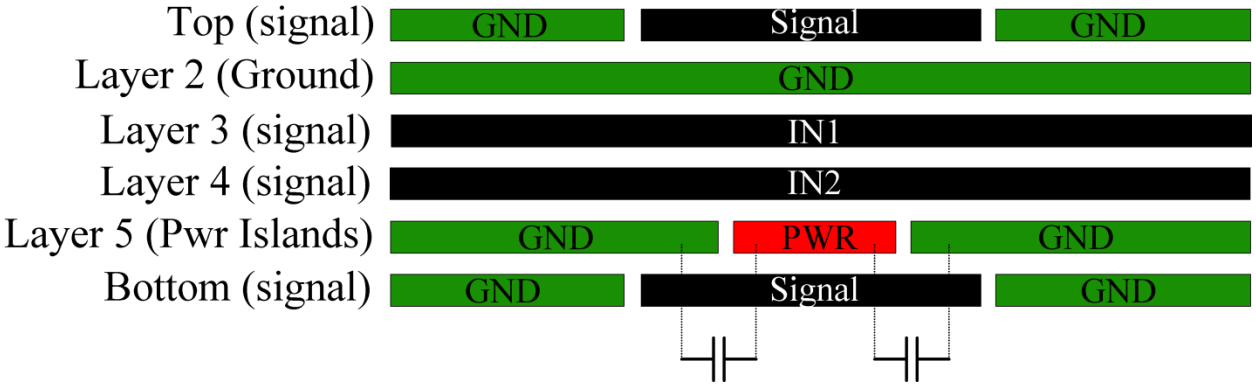


Figure 5-3: Layer stackup Power and Ground Decoupling

6 Baseboard functions

6.1 LAN

6.1.1 Component Placement

Component placement can affect signal quality, emissions, and component operating temperature. Careful component placement can decrease potential EMI problems and simplify the task of routing traces.

- If the magnetic is a discrete component, then the distance between the magnetic and the RJ-45 needs to have the highest consideration and be kept to less than 25mm (approx. 1 inch) of separation Refer to Figure 6-1.

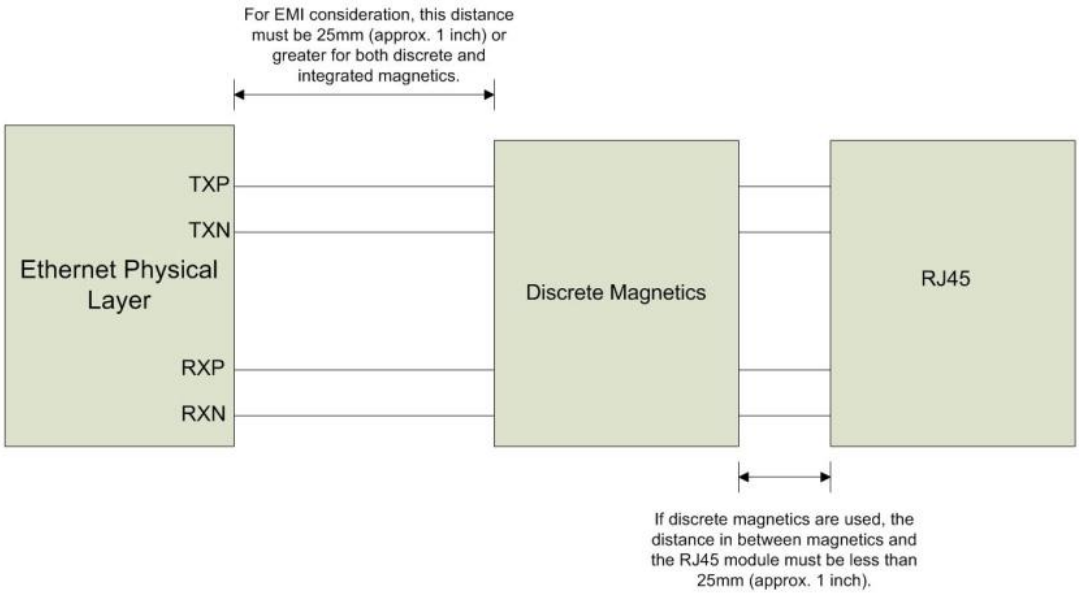


Figure 6-1: Discrete magnetic and RJ-45 Placement

- The distance between the PHY and the magnetics needs to be 25mm (approx. 1 inch) or greater. Among PHY vendors, the 25mm (approx. 1 inch) rule is considered good design practice for EMI considerations. The intention is to isolate the PHY from the magnetics.
- The crystal oscillator and its resistors and capacitors must be placed within 12mm (approx. 500mils) of the PHY.
- The power supply decoupling capacitors need to be placed within 7mm (approx. 280mils) of the power supply.
- Keep the PHY device and the differential transmit pairs at least 25mm (approx. 1 inch) from the edge of the PCB, up to the magnetics. If the magnetics are integrated into the RJ45, the differential pairs should be routed to the back of the integrated magnetics RJ45 connector, away from the board edge.
- The 49.9 ohm pull-up resistors on the differential lines, TXP/TXN and RXP/RXN, must be placed within 10mm (approx. 400mils) of the PHY device. This ensures the transmit path is identical between the TX and RX.

- The signals associated with each port (TX or RX) should be independently matched in length to within 6mm (approx. 240 mils).
- The strapping resistors need to be located within 20mm (approx. 800mils) of the Ethernet PHY to ensure the voltage into the pin at boot-up is at the correct Vih or Vil level.

6.1.2 Design Techniques for EMI Suppression

The following techniques may improve EMI margin.

- Common mode capacitors may be added to the TX+/- and RX+/- signals of the Ethernet PHY device for high frequency attenuation, as shown below in Figure 6-2. One end of each capacitor should be connected to the system ground plane, and placed within 10mm (approx. 400mils) of the magnetics. Typical capacitance values should be between 10pF and 22pF. Values higher than 22pF may negatively impact the TX and RX signaling.

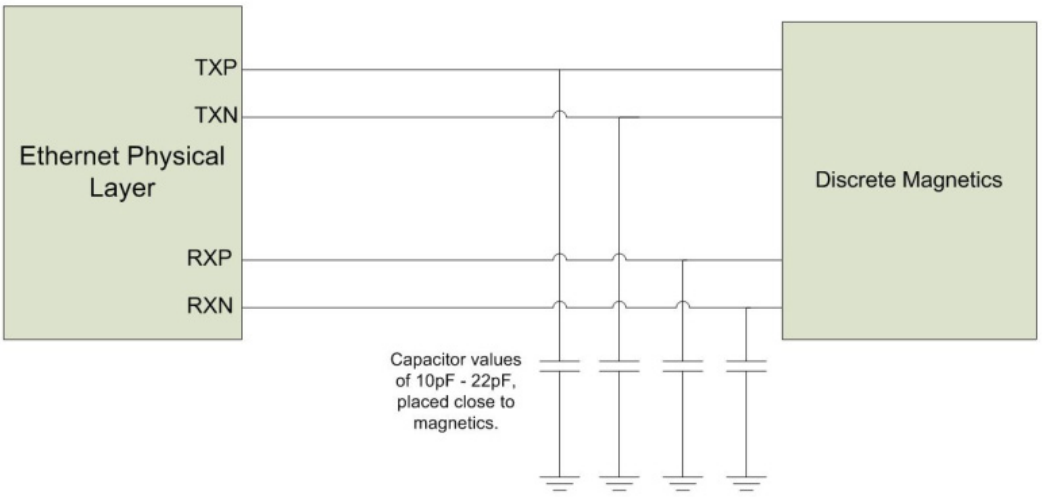


Figure 6-2: Common Mode Capacitors

- Common mode chokes may be added to the design at the point where DC power enters the PCB as shown below in Figure 6-3. This attenuates emissions that would otherwise be radiated from the system power cord. Common mode chokes will have some impedance at a given frequency. Choose the number of chokes and/or type of ferrite material to provide adequate attenuation at the frequencies in the system that may generate unwanted emissions.

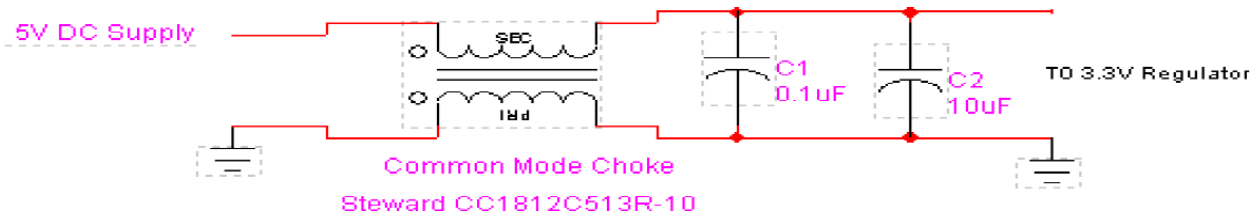


Figure 6-3: Common Mode Choke on PCB DC Input

- Common mode chokes may be added to the TX and RX differential pairs as shown below in Figure 6-4. The common mode chokes should be placed within 10mm (approx 400mils) of the integrated RJ45 module, and on the magnetics side of the common mode EMI suppression capacitors. Typical common mode impedance of the common mode choke selected should be 2Kohm @ 100 MHz or higher.

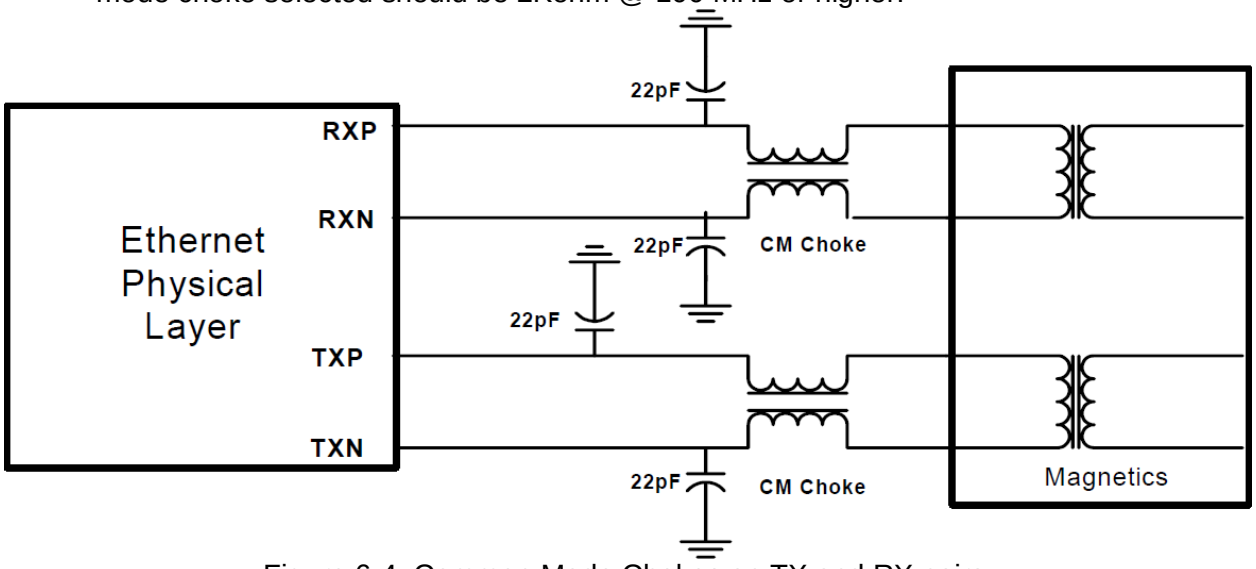


Figure 6-4: Common Mode Chokes on TX and RX pairs

- In general, no ground plane should extend under the TX and RX differential pairs, under the magnetics, or under the RJ45 jack. In case where common mode capacitors are used for EMI suppression, a ground plane may be located under the TX and RX signals, however the plane must not extend beyond the capacitors. When designing 4 layer boards, the ground plane should exist on layer 4, assuming the differential pair is routed on layer 1. On 2 layer boards, the ground plane can be located on layer 2. The adjacent layer to the TX and RX signal pairs. Under no circumstances should a ground plane exist under the magnetics, the RJ 45 connector, or in between the magnetics and the RJ45 connector.

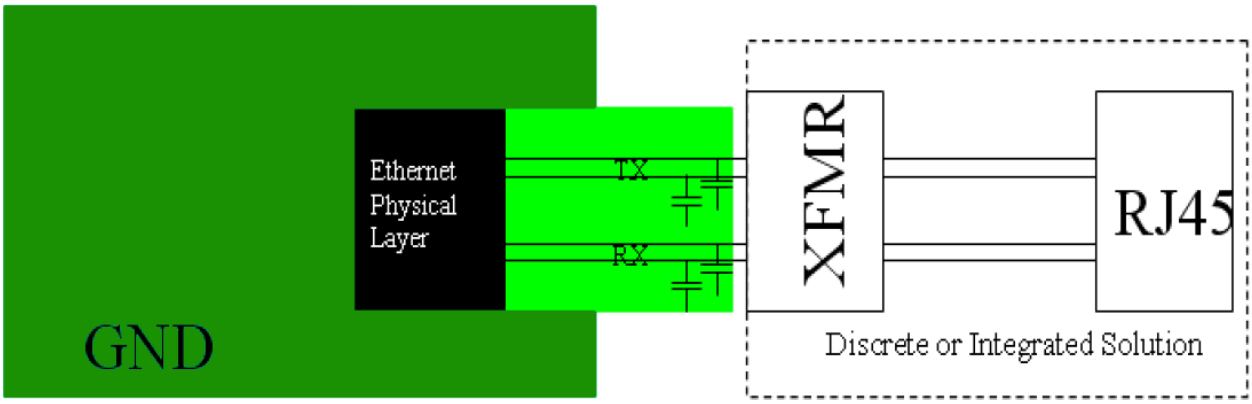


Figure 6-5

Generally, MII/ RMII interface signals can be directly routed to the MAC; however series termination resistors may be included on RXCLK, TXCLK, and all other RX MII or RMII

interface signals for additional EMI suppression. Figure 6-6 below shows these termination resistors. MII/ RMII series terminations should be located within 10 mm (approx. 400 mils) of the Ethernet physical layer device, and routed adjacent to an uninterrupted reference plane. 100 ohm series termination resistors have been found to be good values for improving EMI.

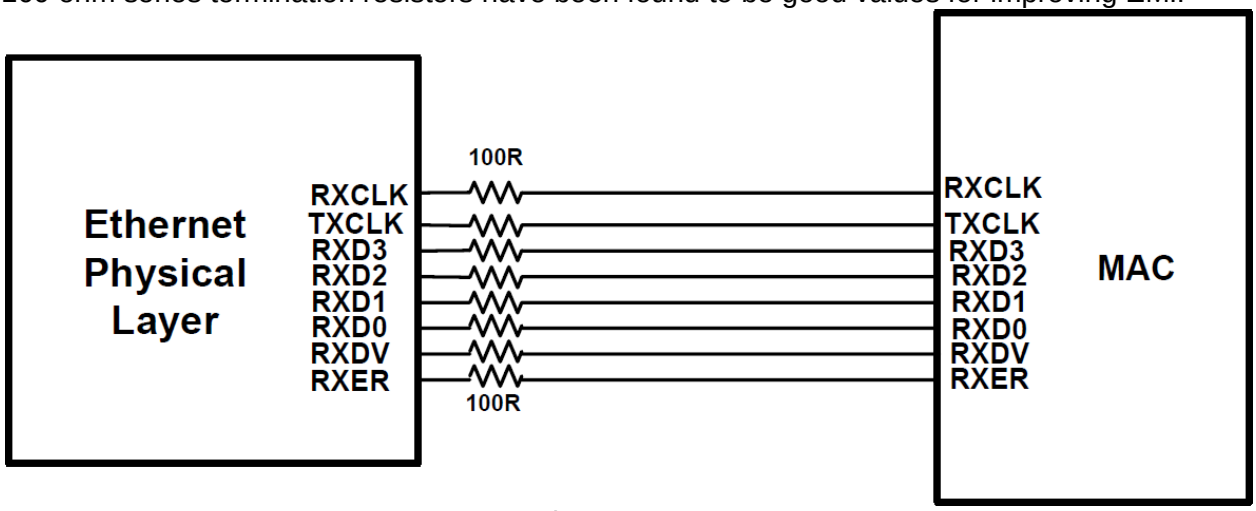


Figure 6-6

6.1.3 Controlled Impedance for Differential Signals

The 802.3-2005 specifications require the TX and RX lines to run in differential mode. The TXP and TXN are a differential pair and need to be designed to a 100 ohm differential impedance. The RXP and RXN traces are also a differential pair and need to be designed to a 100 ohm differential impedance target.

The board designer must maintain 100 ohm differential impedance in the layout for all the differential pairs. For different dielectric thickness, copper weight or board stack-up, trace widths and spacings will need to be recalculated.

Differential pair nets must maintain symmetry. TXP and TXN must be equal length and symmetric with regrds to shape, length, and via count. RXP and RXN must also be equal length and symmetric. For example, if TXP goes through a via at 8 mm, then TXN should also go through a via at 8 mm.

Figure 6-7 shows TX/ RX traces with approximately equal trace length and symmetry. It is important to maintain width and spacing that provides differential and common mode impedances compliant with the 802.3 specification. Avoid using 90 degree turns to minimize impedance discontinuities.

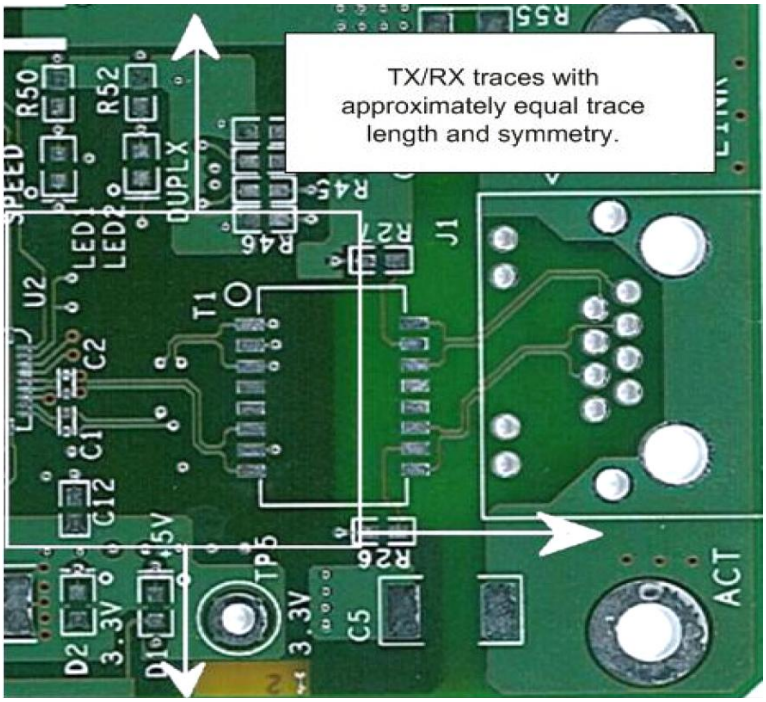


Figure 6-7: Example of Routing TX/RX to RJ-45

- Isolation of TX/RX Traces
  The TX/RX traces must be isolated from nearby circuitry and signals. Maintain a distance of parts to lines that are greater than or equal to 5 times the distance of the spacing between the traces. Do not route differential pairs under parts. Do not cross TX/ RX lines with other PCB traces unless the traces are on the opposite side of the ground plane from the TX/ RX.
- Crystal Oscillator
  The crystal oscillator is sensitive to stray capacitances and noise from other signals. It can also disturb other signals and cause EMI noise. The load capacitors, crystal and parallel resistors should be placed within 7mm (approx. 20mils) of each other. The ground connection for the load capacitors should be short and out of the way from return currents of power lines.

6.1.4 Magnetic module

The magnetics module has a critical effect on overall IEEE and emissions conformance. The device should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Occasionally, components that meet basic specification may cause the system to fail IEEE testing because of interactions with other components or the Printed Circuit Board (PCB) itself. Carefully qualifying new magnetics modules can go a long way toward preventing this type of problem.

There are two levels of magnetics qualification, Suggested magnetics and qualified magnetics.

Suggested magnetics have not been tested in order to verify proper operation with specific device. This category of magnetic has been evaluated by the contents of the vendor supplied datasheet and legacy performance only. However, the designer can assume with some degree

of confidence, that with proper PCB design techniques, the combination of devices and magnetics presented as suggested magnetic will perform to high standards.

Qualified magnetics have been tested in order to verify proper operation with the specific device listed with it. The designer can assume with high degree of confidence, that with proper PCB design techniques, the combination of devices and qualified magnetics will perform to the highest standards.

Vendor	Part Number	Package	Temp
Qualified Magnetics			
UDE	RT7-115A1K1A	Integrated RJ45	0° - +70° C
Pulse	H1102	16-pin SOIC	0° - +70° C
Halo	TG110-RP55N5	16-pin SOIC	0° - +70° C
Halo	HFJ11-RP26E- L12RL	Integrated RJ45	0° - +70° C
Delta	RJSE1R5310A	Integrated RJ45	0° - +70° C
Pulse	HX1188	16-pin SOIC	-40° - +85° C
Halo	TG110-RPE5N5	16-pin SOIC	-40° - +85° C
Halo	HFJ11-RPE26E-L12RL	Integrated RJ45	-40° - +85° C
TDK	TLA-6T717W	Integrated RJ45	-40° - +85° C
Delta	LFE8505T	16-pin SOIC	-40° - +85° C
Suggested Magnetics			
Pulse	J0011D01B	Integrated RJ45	0° - +70° C
Midcom	000-7219-35	Cardbus	0° - +70° C
Bothhand	TS6121C	16-pin SOIC	0° - +70° C
Bothhand	LU1S041X-43	Integrated RJ45	0° - +70° C
Midcom	000-7090-37R	16-pin SOIC	-40° - +85° C
Midcom	MIC66211-5171T- LF3	Integrated RJ45	-40° - +85° C
Elec & Eltek	820-M0323R	16-pin SOIC	-40° - +85° C

6.2 USB PHY layout Guidelines

The Universal serial Bus (USB) is capable of operating at 480 Mbps. Excellent signal integrity is required to operate reliably at high-speed data rates. The PCB layout is a critical component in maintaining signal integrity. This chapter provides recommendations regarding the PCB layout.

6.2.1 Controlled impedance for USB traces

The USB 2.0 specification requires the USB DP/ DM traces maintain nominally 90 Ohms differential impedance (see USB specification Rev 2.0, paragraph 7.1.1.3 for more details). In this design the traces are 14 mil wide with minimum line spacing of 7 mils. These numbers are derived for 13 mil distance from ground reference plane. A continuous ground plane is required directly beneath the DP/ DM traces and extending at least 5 times the spacing width to either side of the DP/ DM lines.

Maintain close to 90 Ohms differential impedance. For different dielectric thickness, copper weight or board stackup, trace width and spacing will need to be recalculated.

Maintain symmetry between DP/ DM lines in regards to shape and length.

Single ended impedance is not as critical as the differential impedance, a range of 42 to 78 Ohms is acceptable (equivalently, common mode impedance must be between 21 Ohms and 39 Ohms).

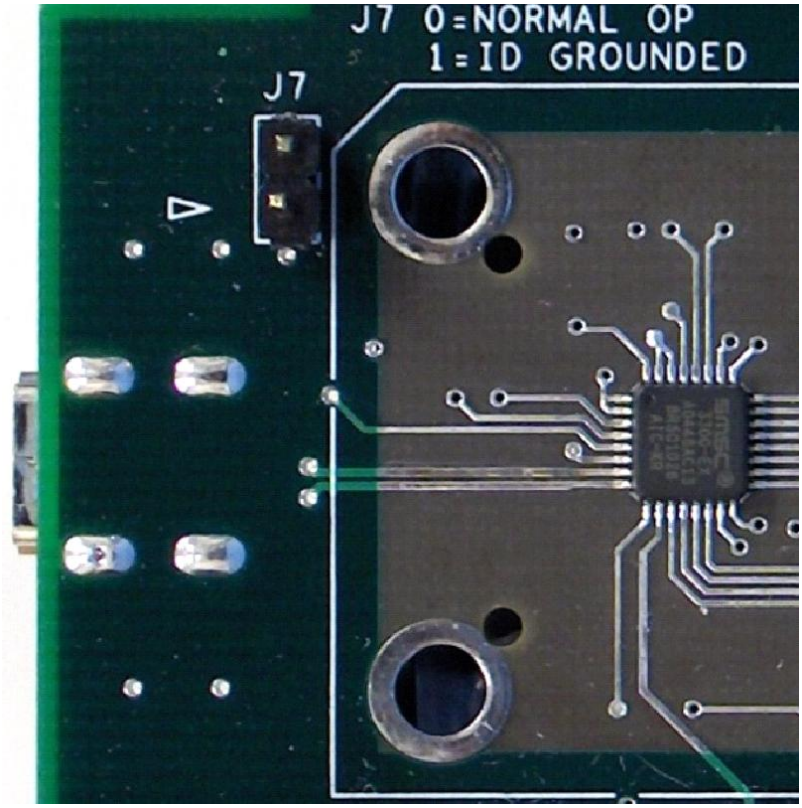


Figure 7-8: Example of routing DP/ DM to Type B connector

Above figure shows DP/ DM traces with approximately equal trace length and symmetry. It is important to maintain a conductor width and spacing that provides differential and common mode impedances compliant with the USB specification. Use 45 degree turns to minimize impedance discontinuities.

6.2.2 Isolation of DP/ DM Traces

The DP/ DM traces must be isolated from nearby circuitry and signals. Maintain a distance of parts to lines that is greater than or equal to 5 times the distance of the 7 mil spacing between the traces. Do not route differential pairs under parts. Do not cross DP/ Dm lines with other PCB traces unless the traces are on the opposite side of the ground plane from GP/ DM. Route DP/ DM traces over solid plane not over power planes.

Note1: USB 1.1 devices can be connected to the USB 2.0 host port only through a USB 2.0 hub.
Note2: USB 1.1 devices can be connected directly to the USB OTG port

6.2.3 Isolated Shielding on the USB Connector.

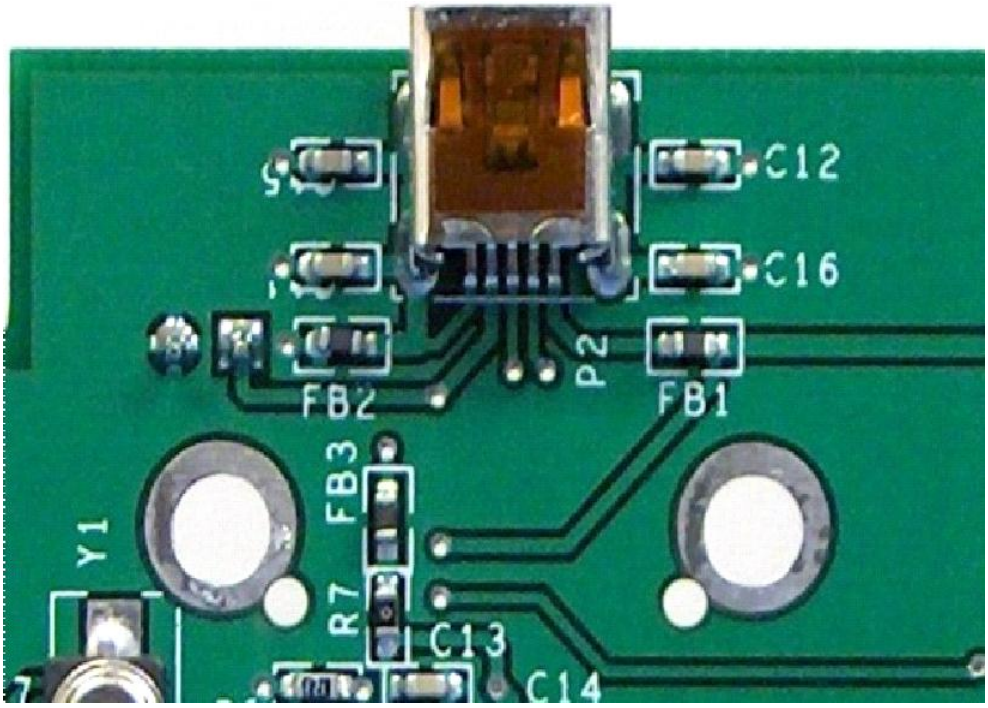


Figure 7-9: Connections to Shield of Type B USB Connector

The USB fully supports USB On-the-Go (OTG) PHY. Above figure shows the Mini AB connector housing is AC coupled to the device ground. The housing is also DC coupled to ground through the ferrite bead, FB2. Industry convention is to ground only the host side of the cable shield. This is done to provide cable shielding while preventing possible ground currents from flowing in the USB cable if there happens to be a potential difference between host and device grounds. If device only operation were desired, it would be advised to cut the trace between FB2 and the connector housing so that only AC grounding of the housing was present.

6.3 Interfaces

6.3.1 I²C

I²C uses only two bidirectional open-drain lines, Serial Data Line (SDA) and Serial Clock (SCL), pulled up with resistors.

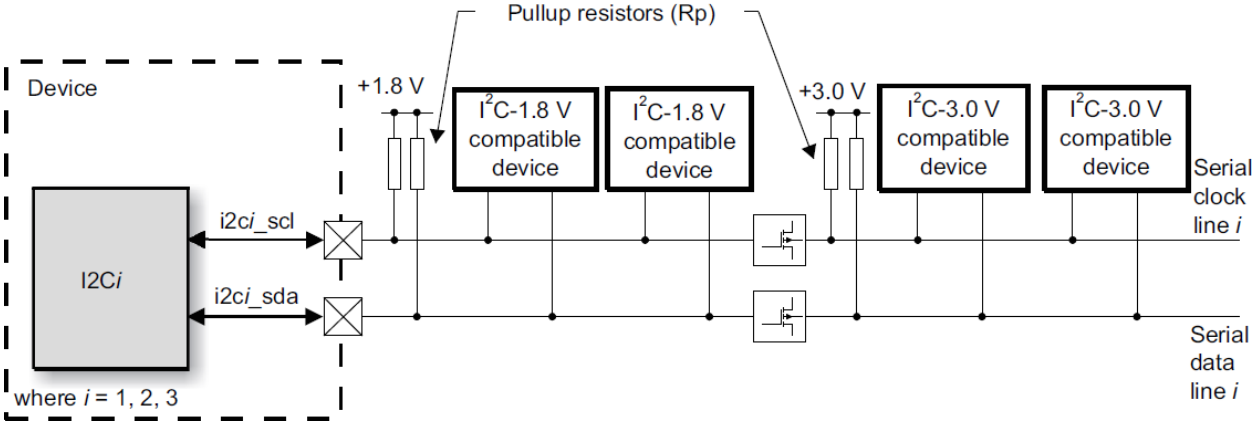


Figure 7-10: HS I²C Controllers and Typical Connections to I²C Devices

6.3.2 I²C Schematic checklist

It is recommended to use 4.7K resistors as pull ups on SDA and SCL. When implementing high speed I²C, lower values (for example 470 ohm) should be used.
As with the standard I²C system pull-up resistors ate required to provide the logic high levels on the translator's bus. (TXS0102 for example) The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with the standard mode and fast mode I²C devices, in addition to SMBus devices. Standard-mode I2C devices only specify 3 mA in a generic I2C system where standard mode devices and multiple masters are possible. Under certain conditions, high termination current can be used.

6.3.3 SPI

The Serial Peripheral Interface Bus or SPI bus is a synchronous serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines.

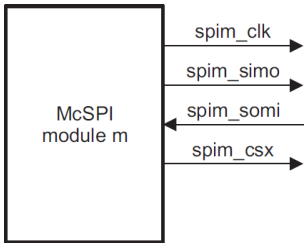


Figure 6-12: McSPI Interface Signals in master Mode

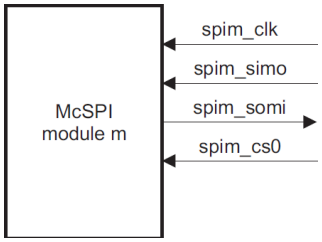


Figure 7-13: McSPI Interface Signals in Slave Mode

6.3.4 Voltage level shifts

The TI TXS0102 **two-bit** non-inverting translator is a bidirectional voltage-level translator and can be used to establish digital switching compatibility between mixed-voltage systems.

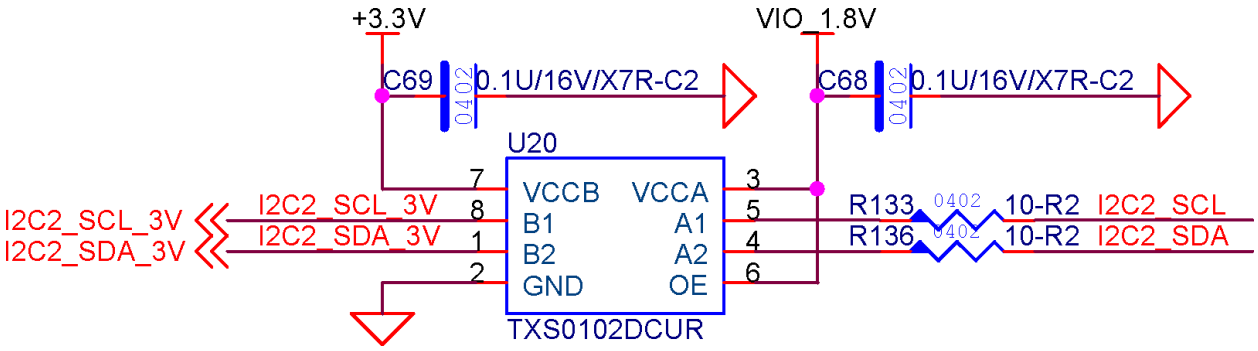
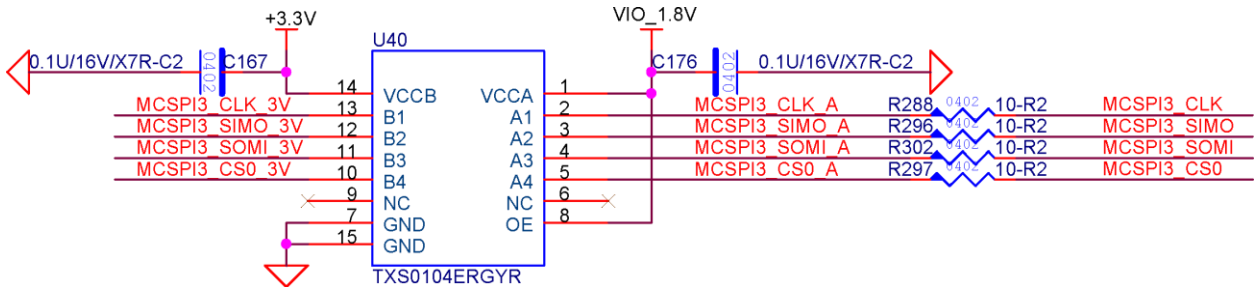


Figure 7-11: typical operating circuit of a voltage level translator

The TI TXS0104 **4-bit** non-inverting translator uses two separate configurable power-supply rails. The A port is designed to track VCCA. VCCA accepts any supply voltage from 1.65 V to 3.6 V. VCCA must be less than or equal to VCCB. The B port is designed to track VCCB. VCCB accepts any supply voltage from 2.3 V to 5.5 V. This allows for low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.



For more details of the level translators, please check the related datasheet.

6.3.5 An example of RTC for I²C

The DS1337 serial real-time clock is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I2C bus.

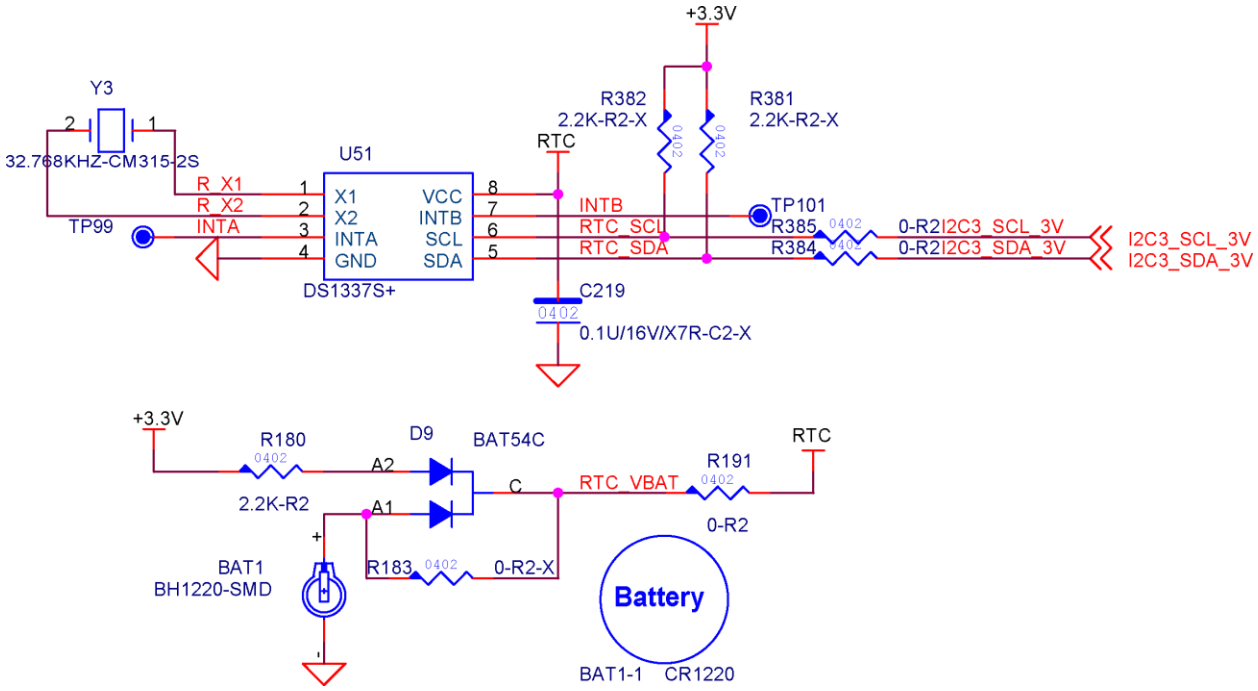


Figure 7-29: Real Time Clock with backup battery

For more details of the RTC, please check the related datasheet.

6.3.6 An example of a Touch screen controller for SPI

The TI TSC2046 is a 4-wire touch screen controller which supports a low-voltage I/O interface from 1.5V to 5.25V.

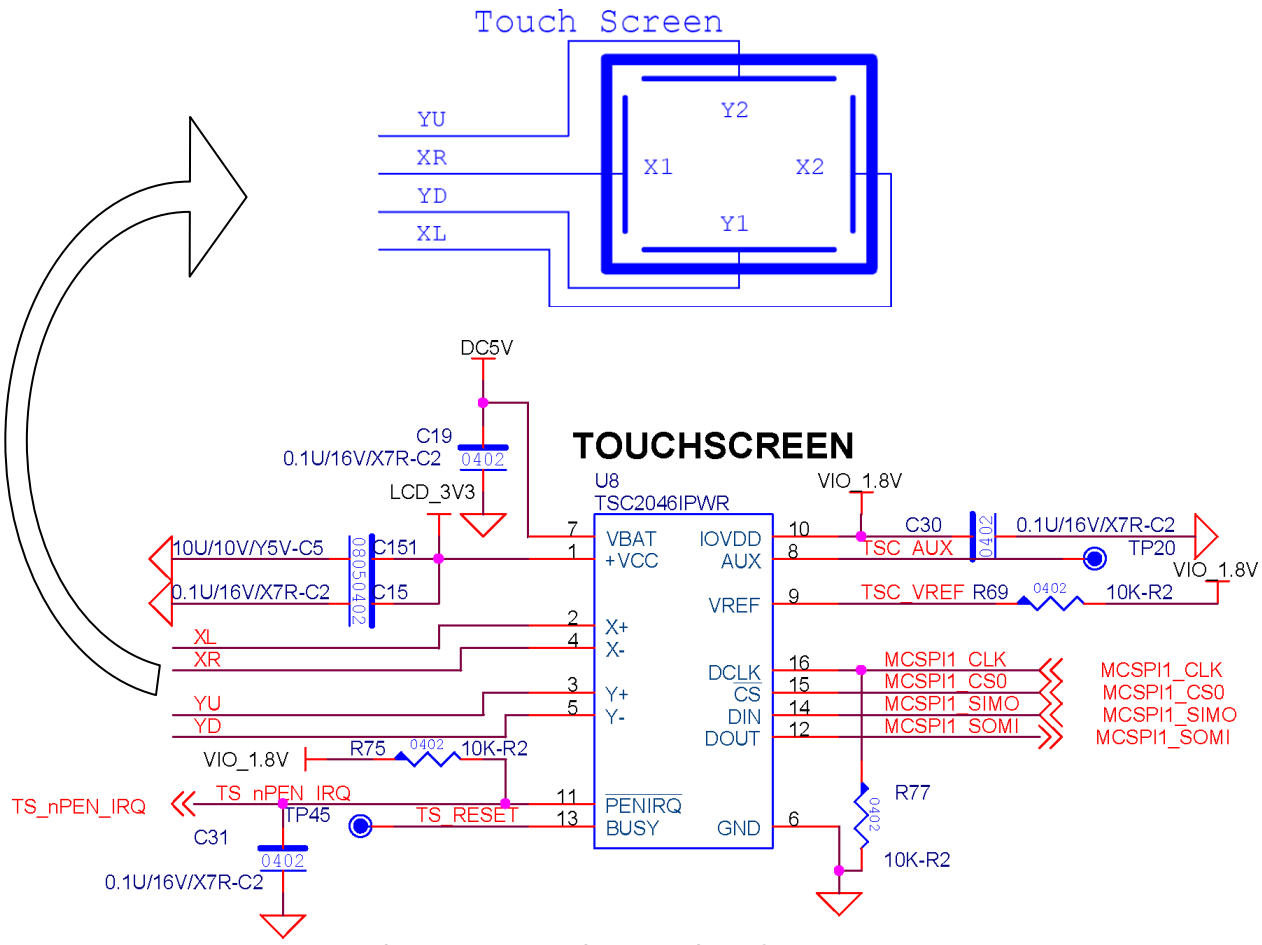


Figure 7-14: Basic operation of TSC2046

For more details of the Touch Screen Controller, please check the related datasheet.

6.4 UART

A universal asynchronous receiver/transmitter (UART) is a type of "asynchronous receiver/transmitter", a piece of computer hardware that translates data between parallel and serial forms. UARTs are commonly used in conjunction with communication standards such as EIA RS-232, RS-422 or RS-485.

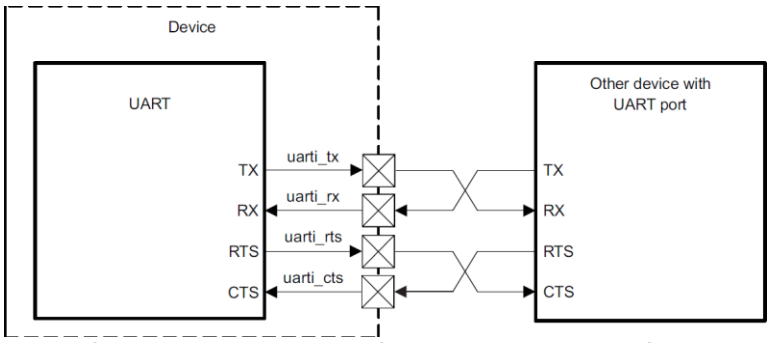


Figure 7-15: UART Mode Bus System overview

6.4.1 An example of a RS-232 Line Driver/ receiver for UART

The ADM3202 transceiver is a high speed, 2-channel RS-232/V.28 interface device that operate from a single 3.3 V power supply.

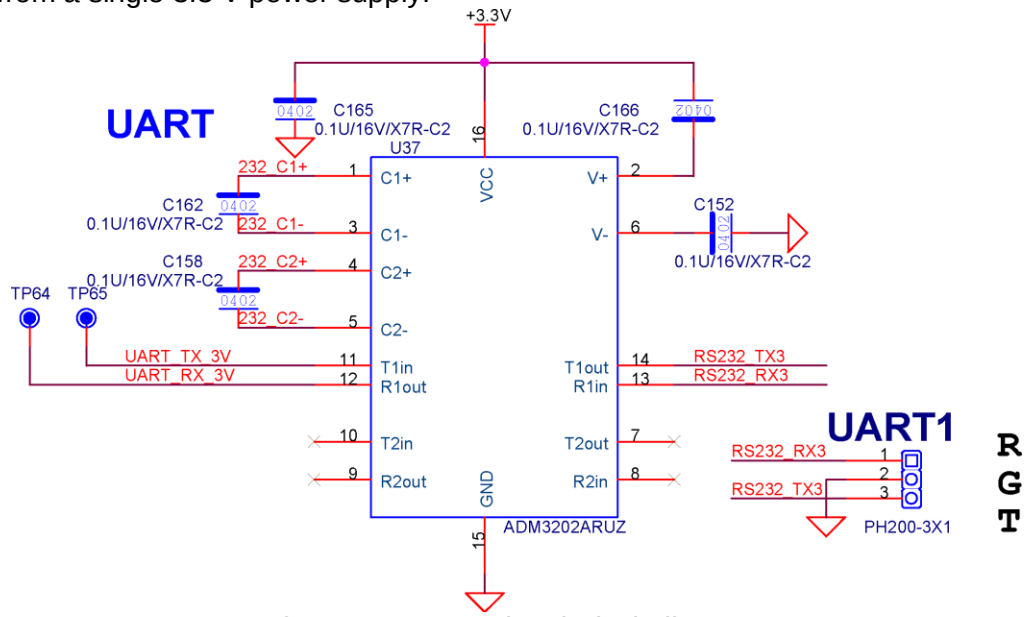


Figure 7-16: Functional Block diagram

For more details of the RS-232 line driver/ receiver, please check the related datasheet.

In the Blizzard baseboard the UART1 is used as the debug port, please check the TDM-3730-userguide for more details

In the event that more UARTs are needed please check the tdm-3730-hardware-manual or contact sales@technexion.com for information and suggestions concerning additional chips and other options.

6.5 DSS

- Add 10ohm series resistors to all data lines, HSYNC, VSYNC, ACBIAS, and PCLK

The TDM-3730 can easily be connected to a 18 or 24 bit TTL panel by following this table:.

DSS_D	24 bit	18 bit
Dss_data0	B0	
Dss_data1	B1	
Dss_data2	B2	B0
Dss_data3	B3	B1
Dss_data4	B4	B2
Dss_data5	B5	B3
Dss_data6	B6	B4
Dss_data7	B7	B5
Dss_data8	B0	
Dss_data9	G1	
Dss_data10	G2	G0
Dss_data11	G3	G1
Dss_data12	G4	G2
Dss_data13	G5	G3
Dss_data14	G6	G4
Dss_data15	G7	G5
Dss_data16	R0	
Dss_data17	R1	
Dss_data18	R2	R0
Dss_data19	R3	R1
Dss_data20	R4	R2
Dss_data21	R5	R3
Dss_data22	R6	R4
Dss_data23	R7	R5

For configuration examples such as VGA, DVI and HDMI check the schematics in the back of this guideline.

For LVDS examples please check the LVDS connection guide

6.6 MMC

The TDM-3730 baseboard includes a micro-SD card slot.

6.6.1 An example of the connection of the MMC Card reader

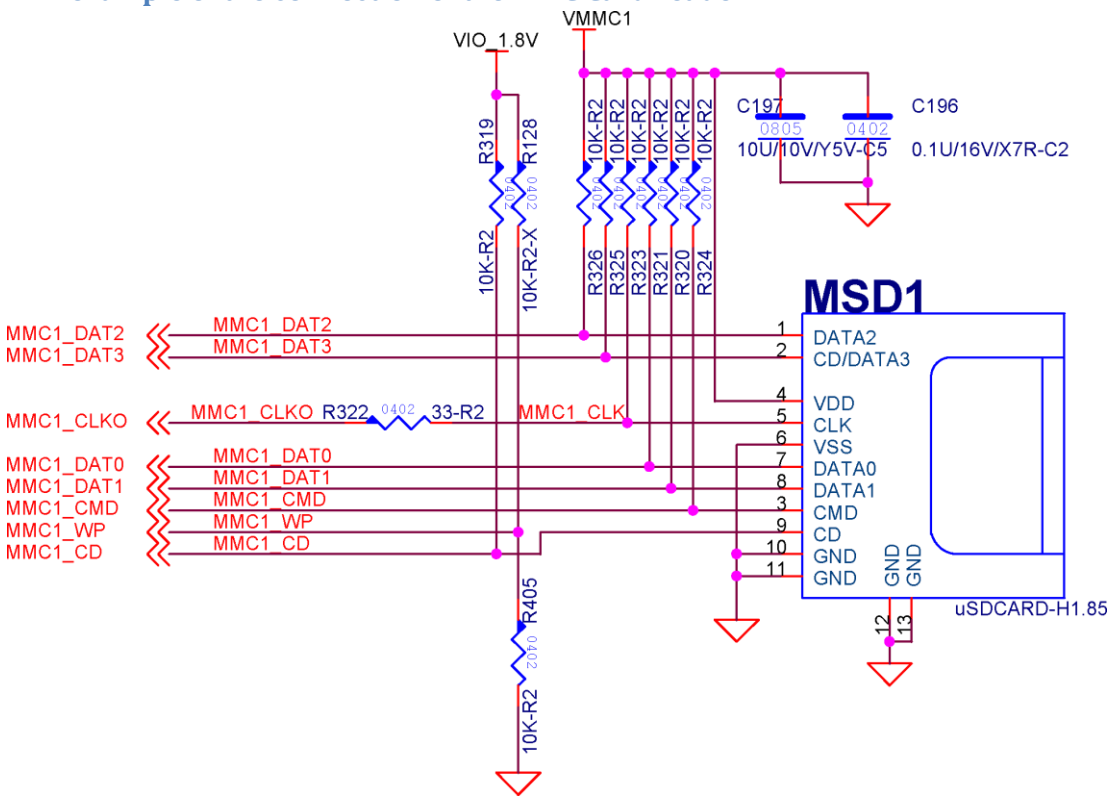


Figure 7-30: MMC card reader

6.6.2 Schematic checklist

- MMC_CLK : no pull ups needed
- MMC_CMD, MMC_DATx: 10K pull ups needed on each signal, unless using it in SDIO mode (eg., connected to a WLAN device) . Be sure to pull up to MMC voltage (on MMC1, that can be 1.8V or 3.0V)
- MMC1_CLK series resistor is needed, placed as close to the processor as possible. Recommended value is 33ohm, but will need to be adjusted based on trace length to the MMC peripheral.
- When using MMC1, VDDS_MMC1 supplies power for MMC1_DAT (0-3).
- If using MMC1_WP (write protect) and MMC1_CD (card detect) signals, they would typically be pulled up to 1.8V before connecting to the processor GPIO or TPS659xx GPIO. MMC1_CD can be used as a power saving feature to detect insertion of the card even when you have shut off the power via VDDS_MMC1. Connecting it to TPS659xx device will allow it to turn on/off voltage upon insertion/removal of the card. Similarly, connecting MMC1_CD to the processor will allow for an interrupt to enable an external power source to turn on/off upon insertion/removal of the card.

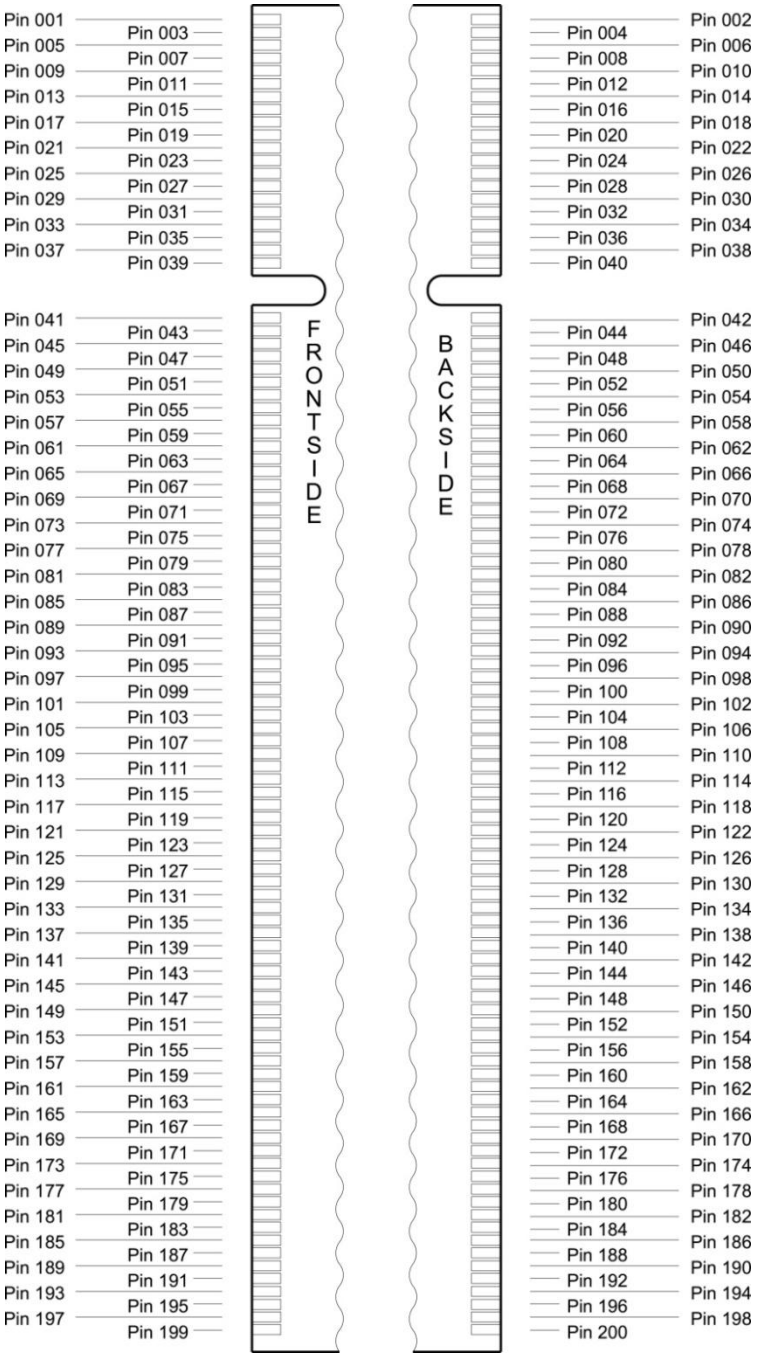
6.7 Video recording

Video recording can be done with for example the TVP5146 Digital Video Decoder or a camera sensor. The Blizzard baseboard has a camera interface. The TechNexion TCM500A camera module can be mounted on this standard dual row connector (17 x 2 female header, 1.27 mm pitch, and 4.4 mm height).

Download the TCM-500A Camera Module user guide for more information about this interface.

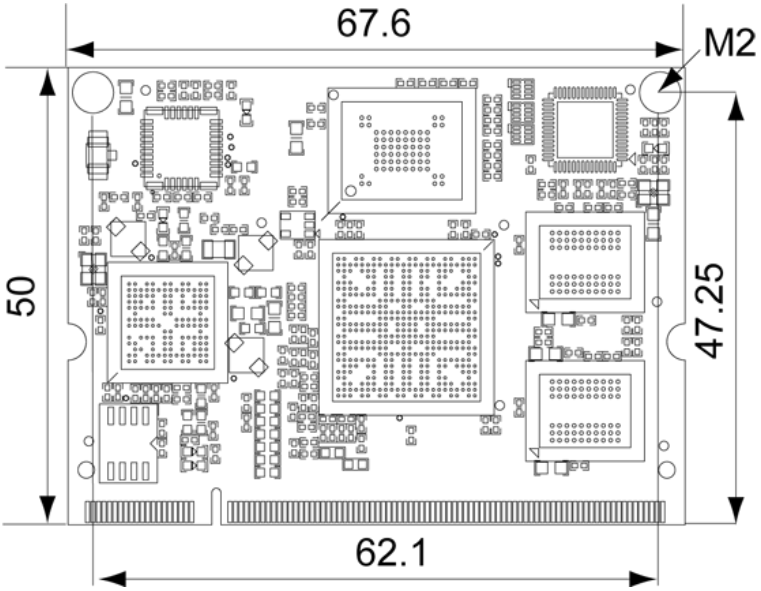
7 Module Connection

7.1 Module connector Standard Pin Out



For the Pin out and for changing the signals on the pins, it is recommended to read the TDM-3730-hardware-manual, which describes how signals can be multiplexed.

7.2 TDM-3730 System on Module Dimensions



Dimensions in mm, tolerance +/- 0.2 mm

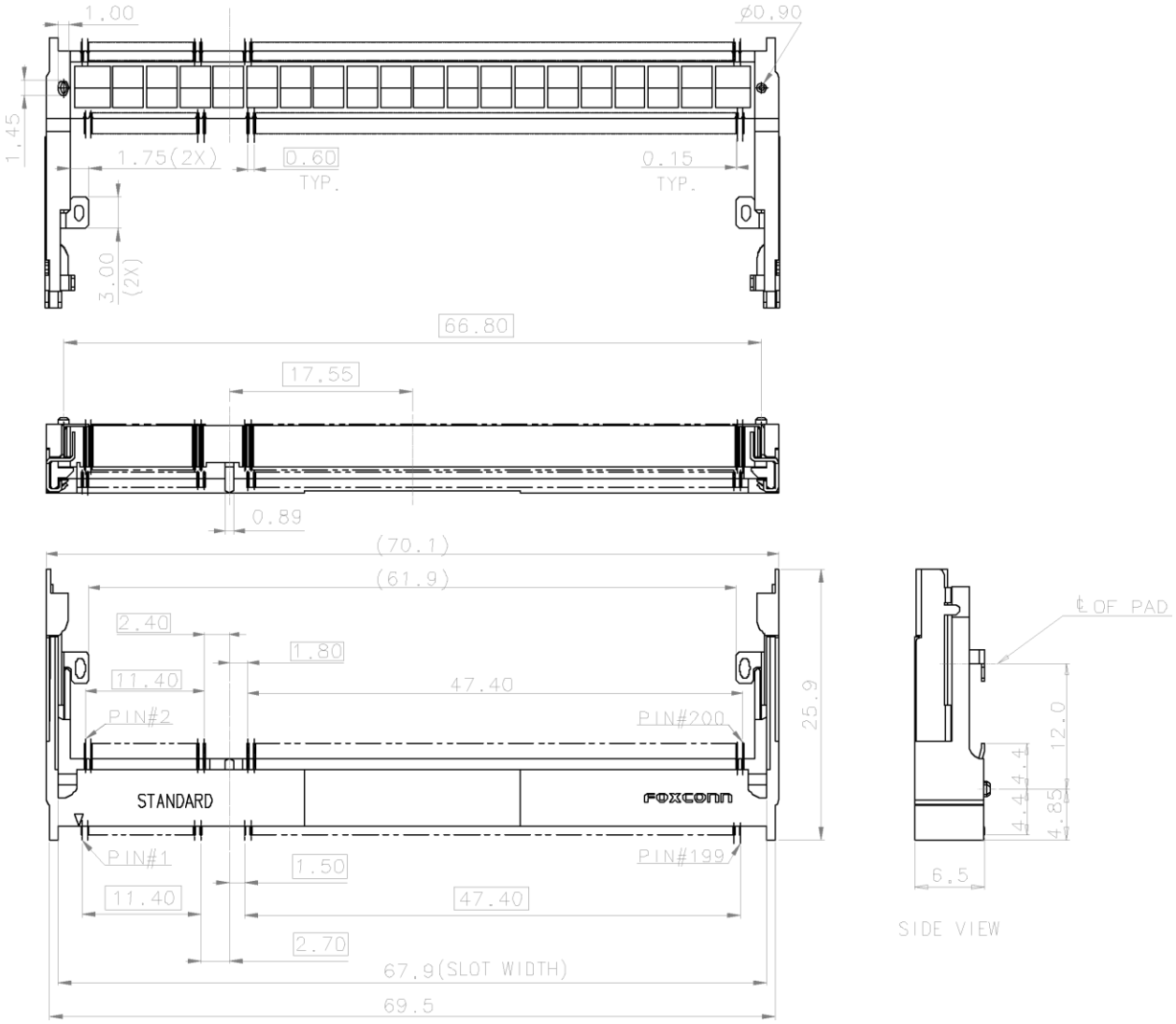
7.3 Module Connector DDR2 SO-DIMM for TDM-3730

To mount the TDM-3730 module on the baseboard it isrecommended to use a connector with the following specifications:

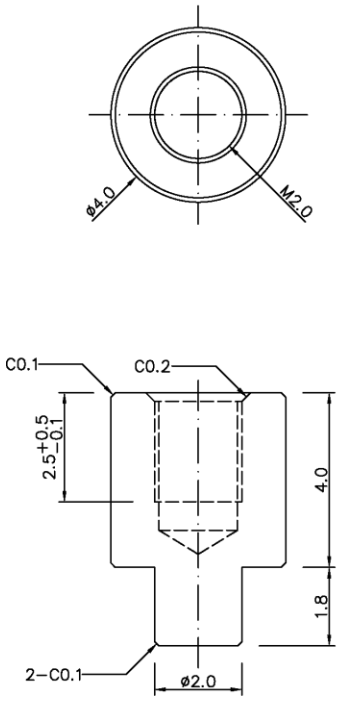
- DDR II SO-DIMM 200pin SMT
- Standard
- Recommended height 6.5 mm

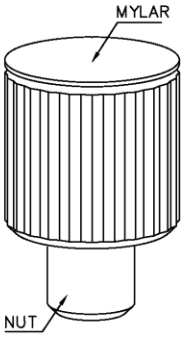
For example Foxconn AS0A426-N6SN-4F or Tyco 5-1746530-4

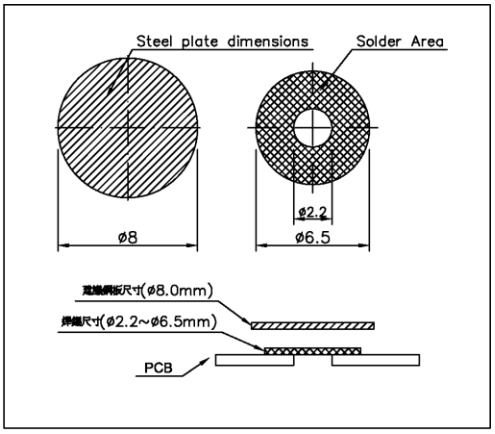
If you have difficulty purchasing these parts please contact sales@technexion.com, for assistance.



7.4 Nut to Fix TDM-3730 Module to the Baseboard







PCB Recommend Layout Pattern

Note 1: Always design the above mounting nut/pose on your custom baseboard and fasten the TDM-3730 to ensure a solid connection and counter vibration prone applications.

Note 2: On a custom baseboard always connect the mounting nut/pose to the baseboard general system GND section.

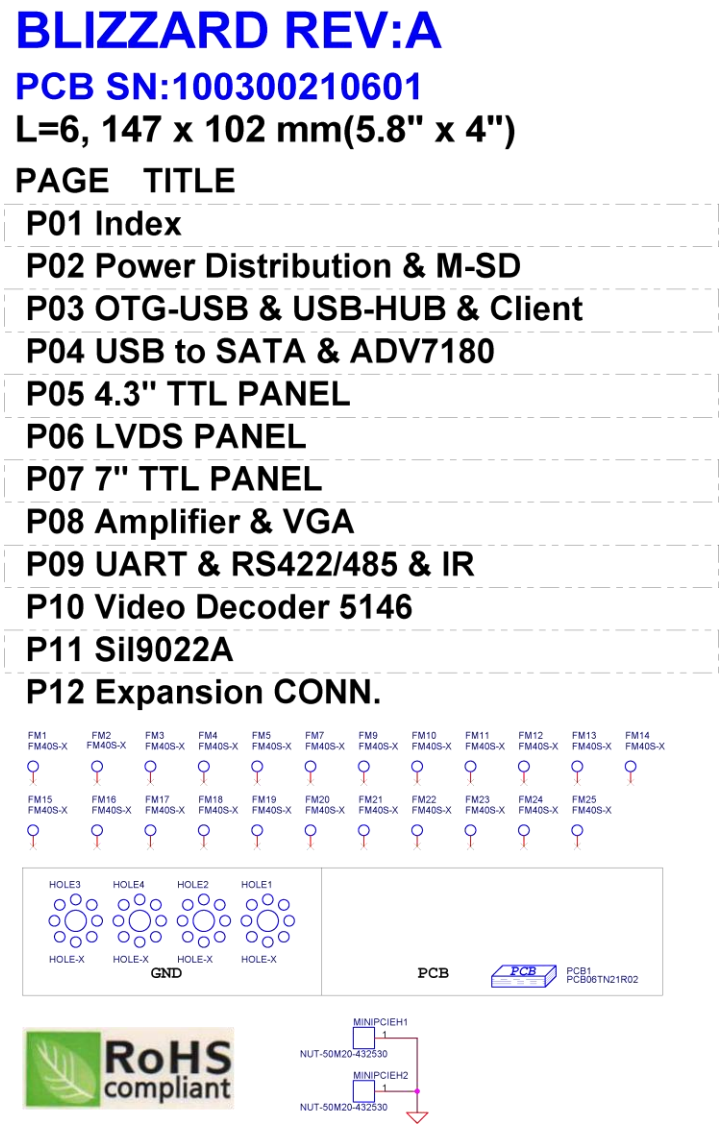
If you have difficulty purchasing these parts please contact sales@technexion.com, for assistance.

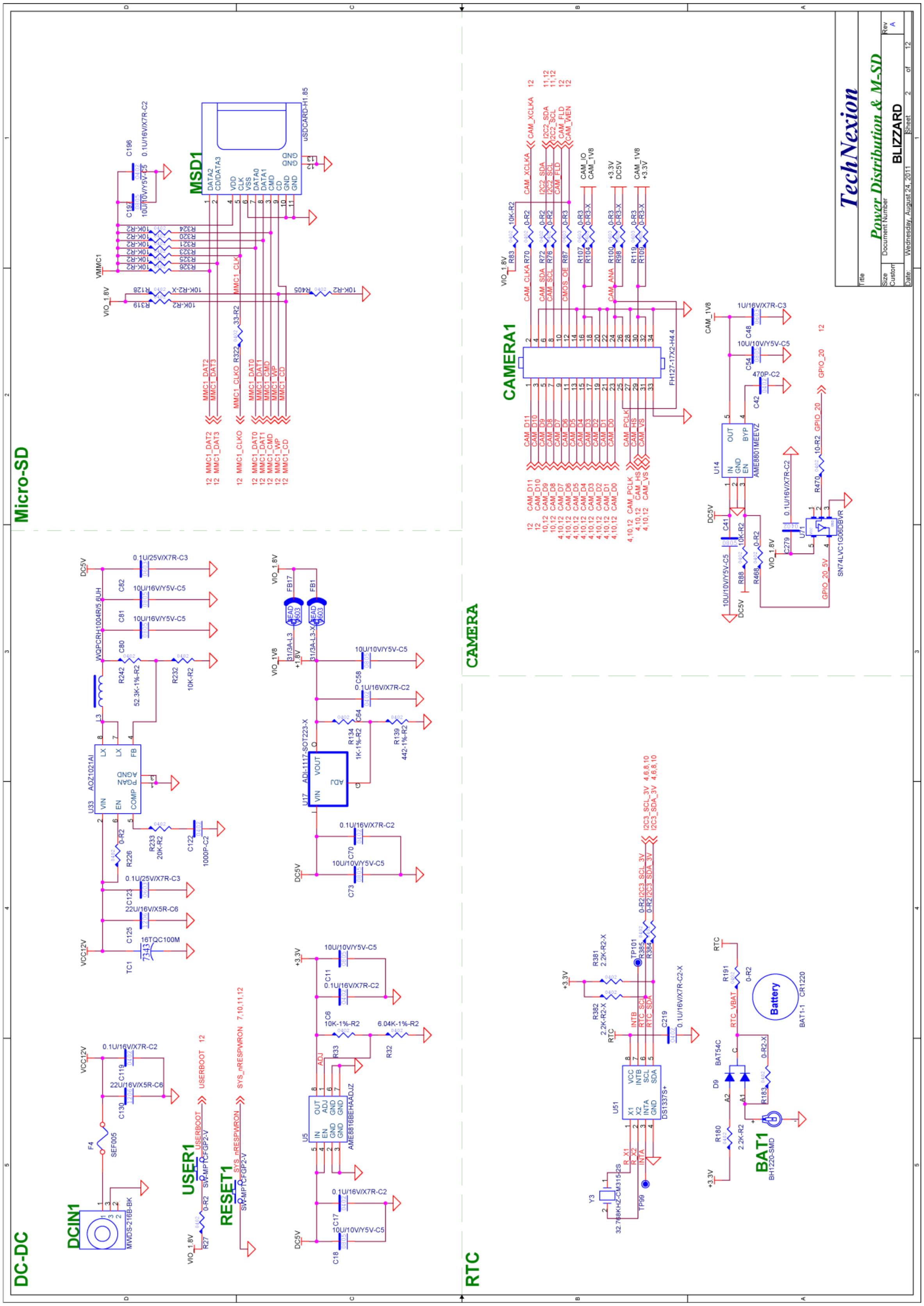
8 Note on schematic drawings

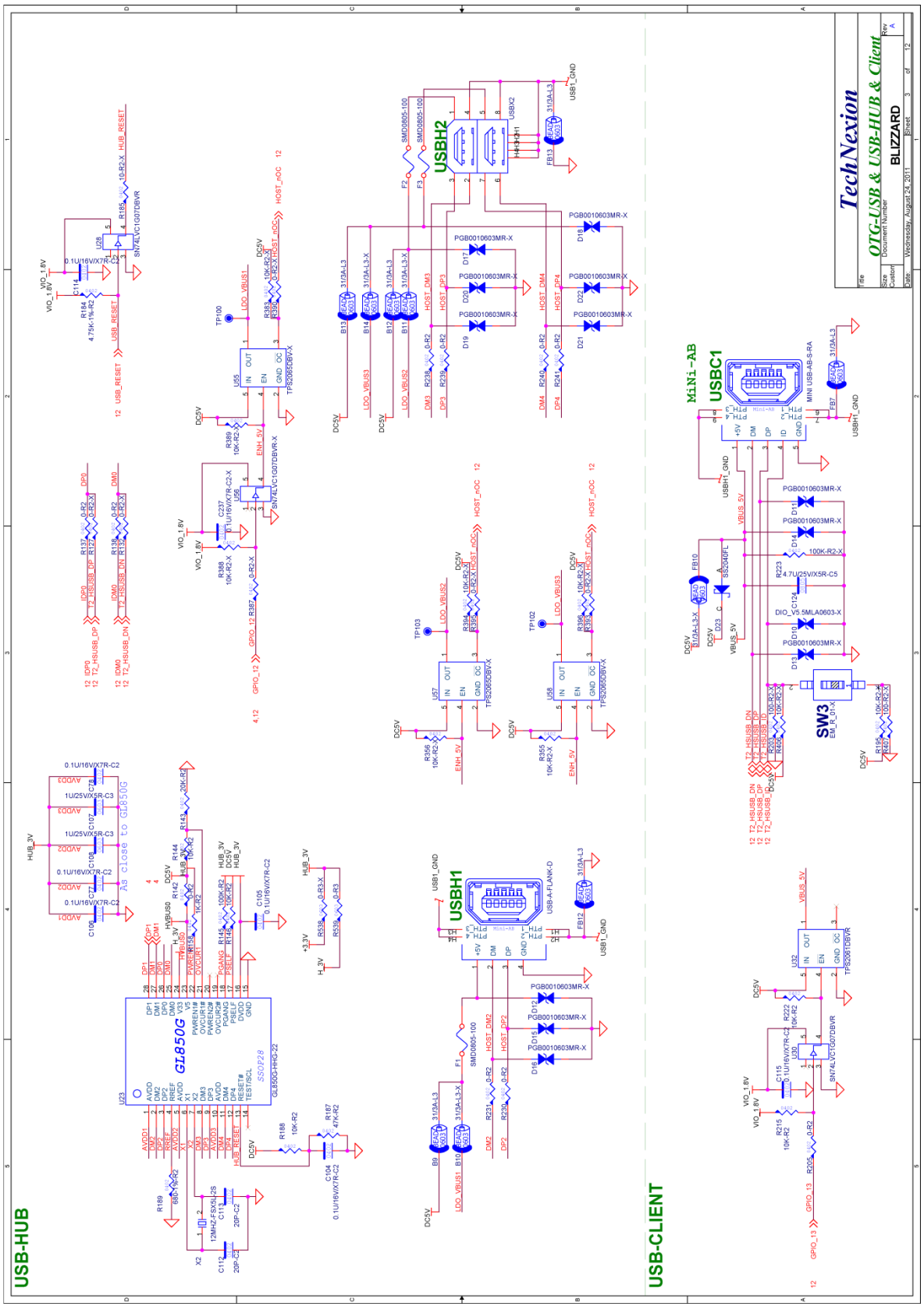
The manual will show some examples of schematics that are used on our baseboards, they might, however, not be suitable for your application.

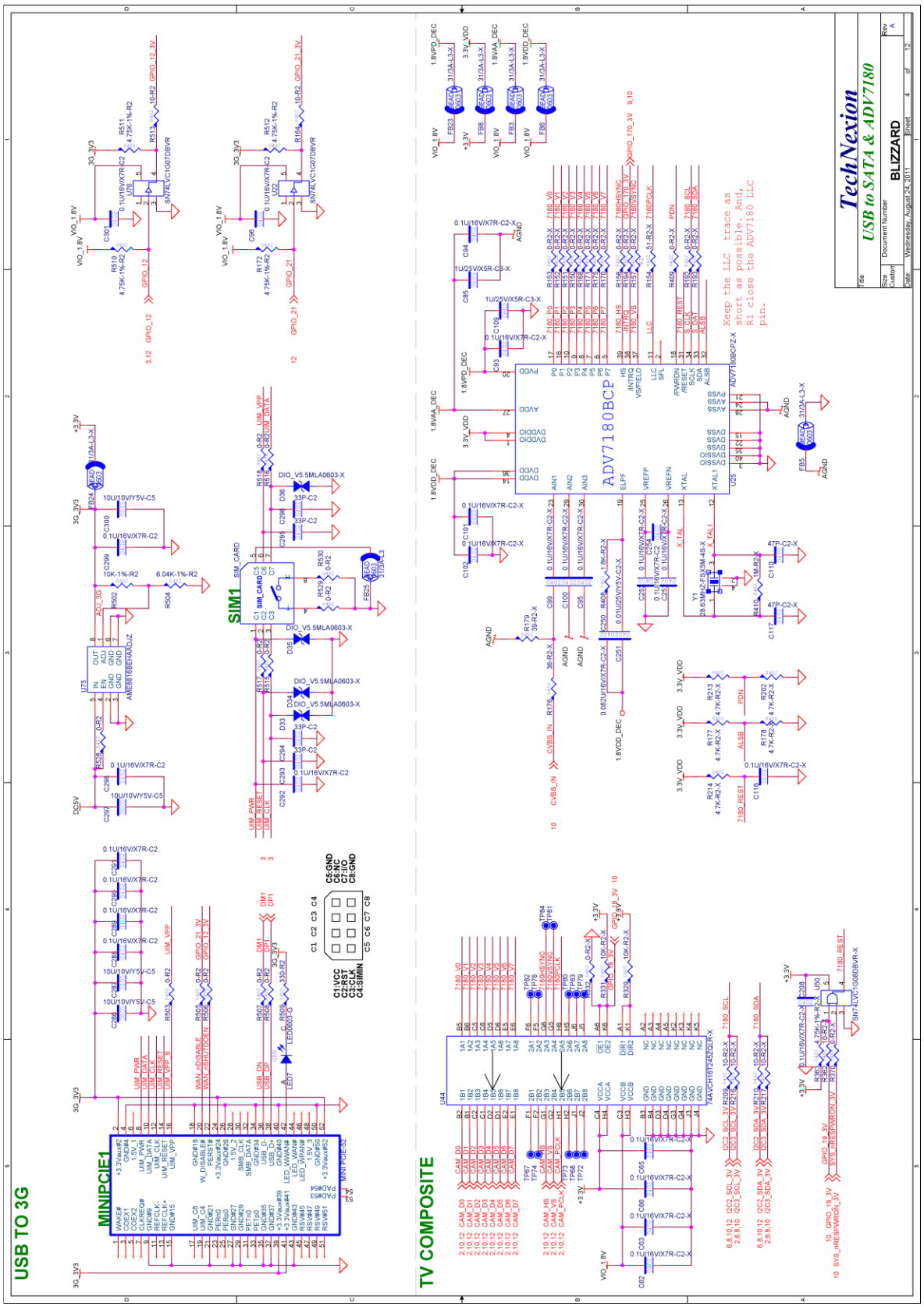
The schematics can be split up over several pages; there is NO guarantee that the shown examples are complete.

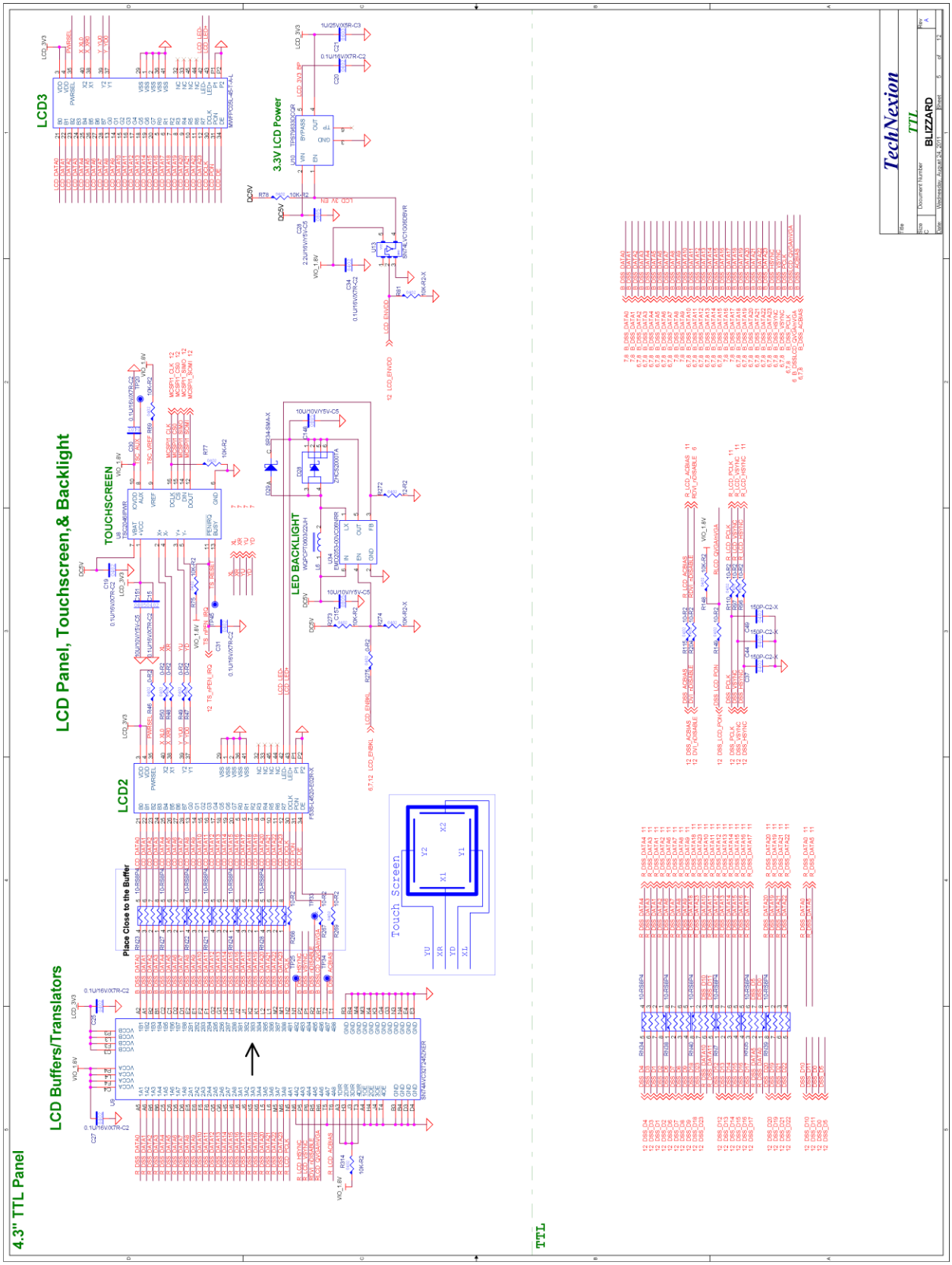
- The number behind a signal is a page number and indicates that the signal is also used on another page of the schematics.
- When a component name has the addition “-x” it means that the component was NOT mounted on the board

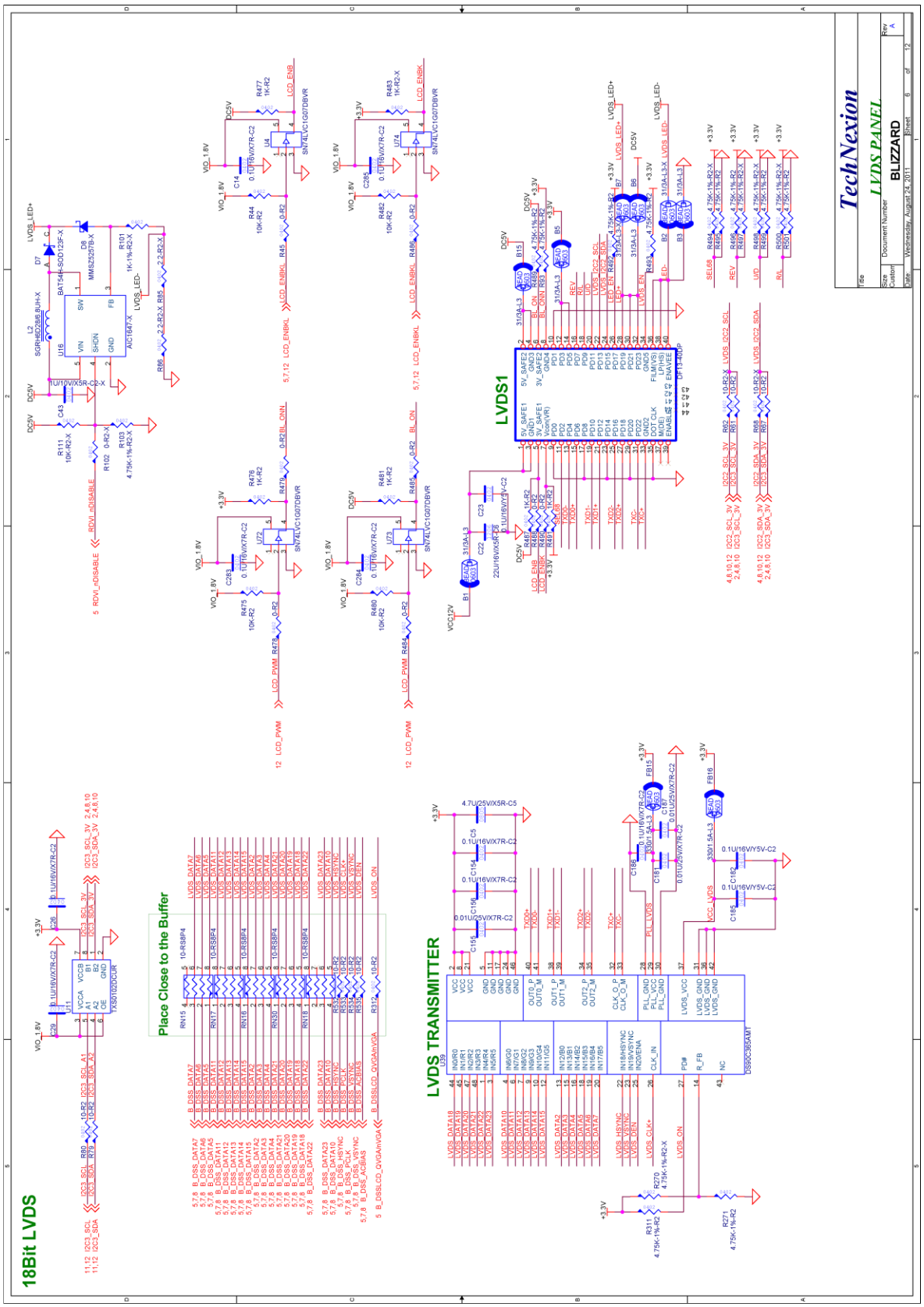


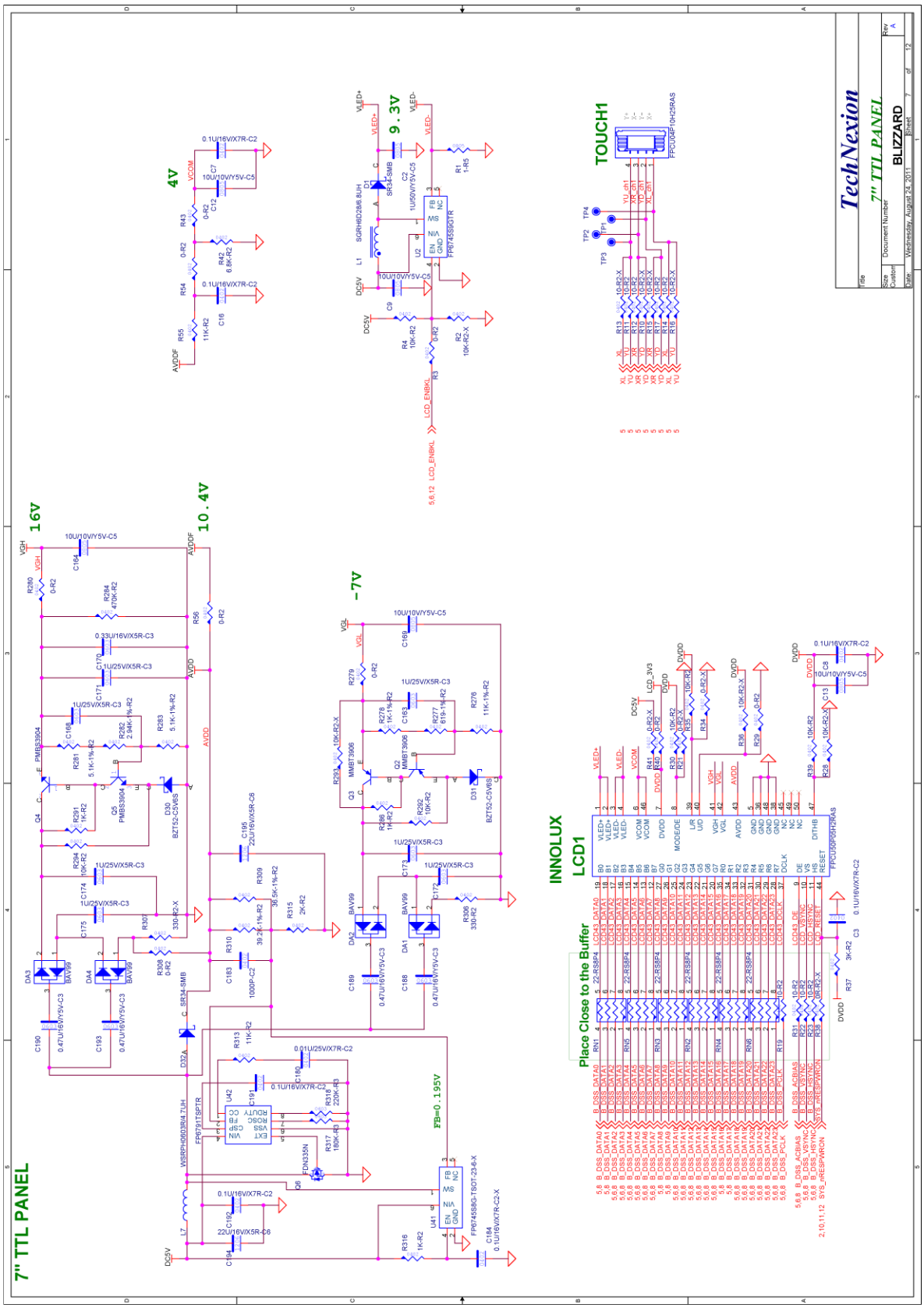

Micro-SD
MSD1
CAMERA1
CAMERA
DC-DC
DCIN1
USER1
RESET1
RTC
BAT1
TechNexion
Power Distribution & M-SD
BLIZZARD
Wednesday, August 24, 2011
Sheet 2 of 12
Rev A

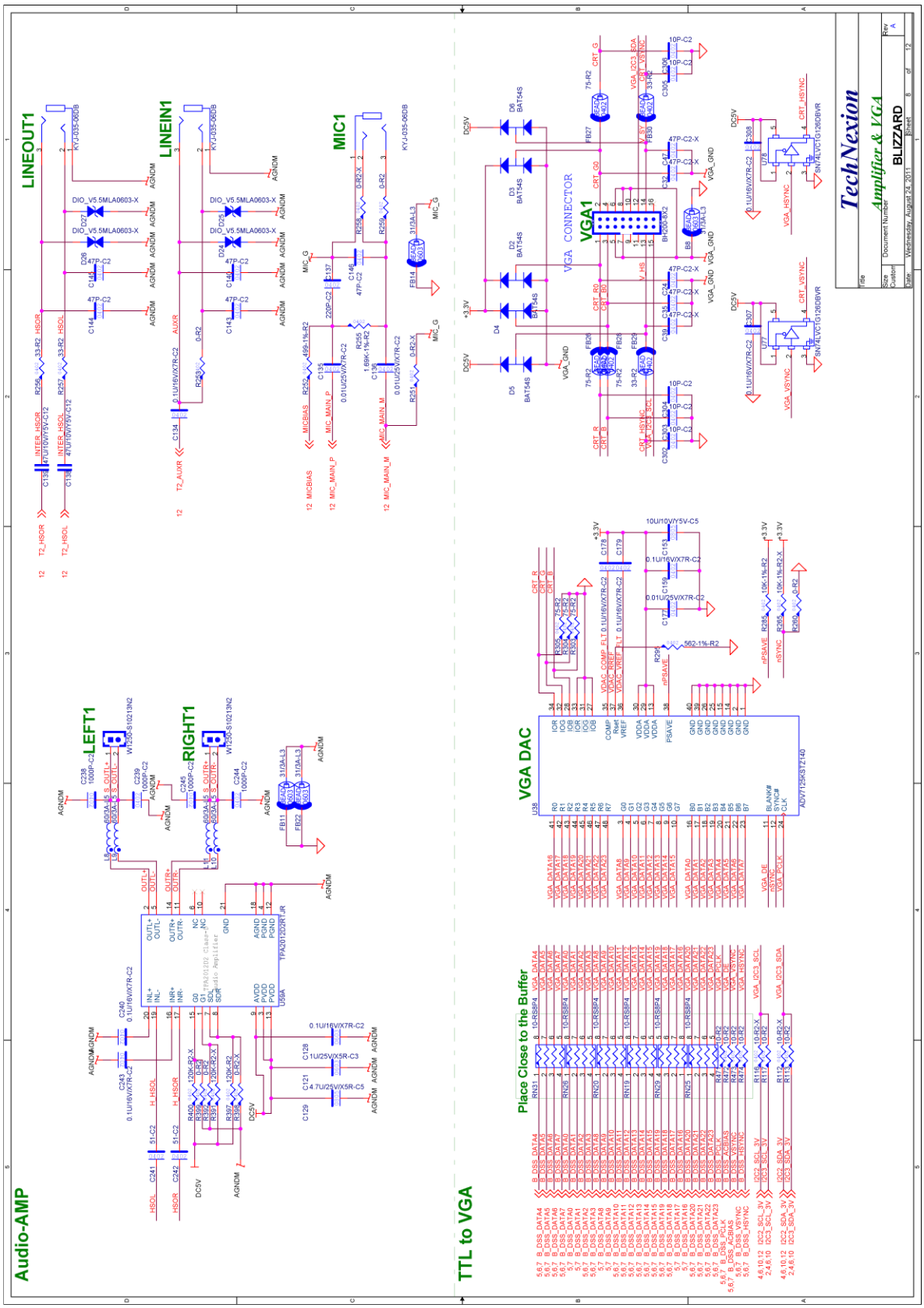

USB-HUB
USB-CLIENT
USBH2
USBH1
USBC1
MiNi-AB
SW3
GL850G
TechNexion
OTG-USB & USB-HUB & Client
BLIZZARD

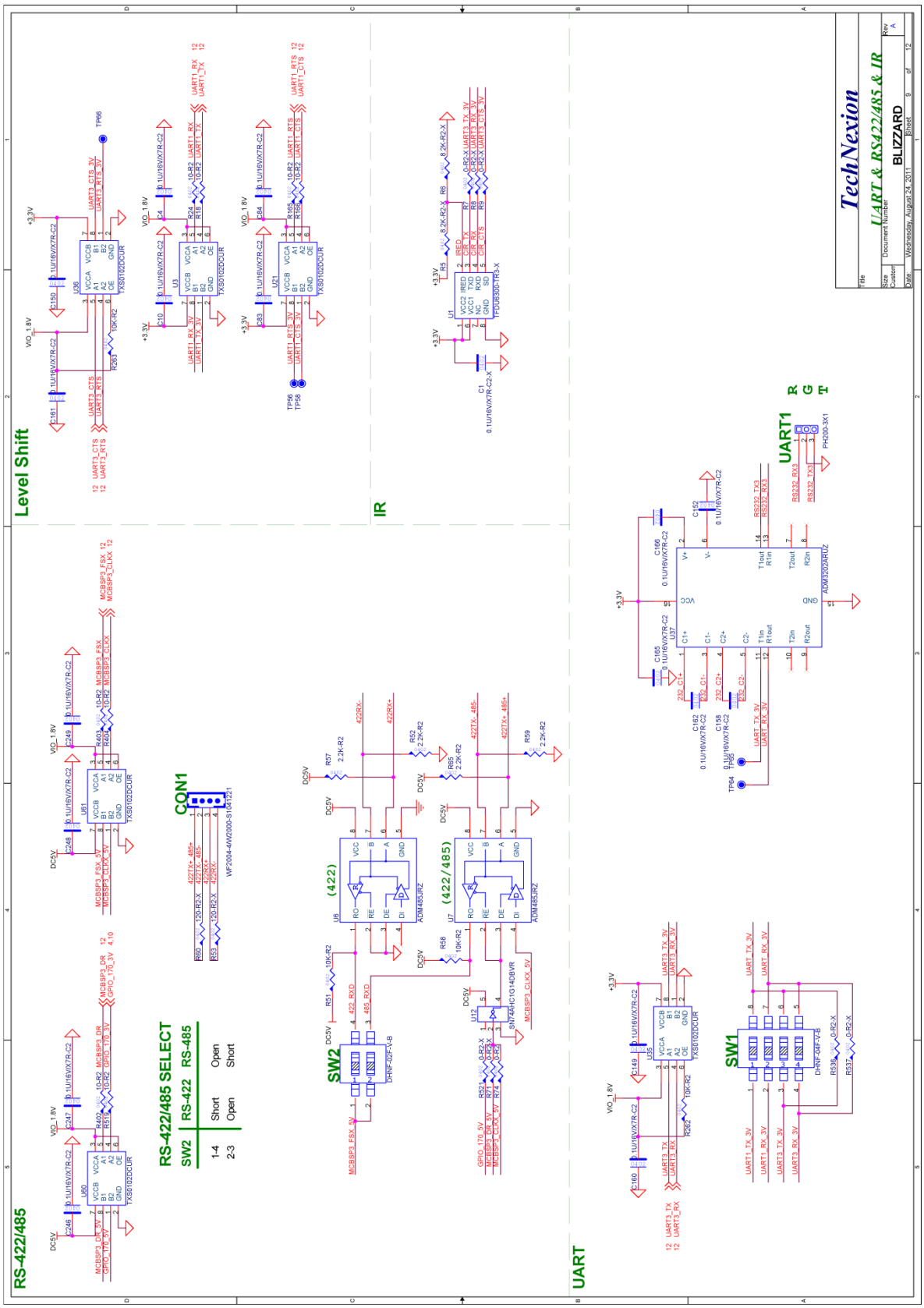

USB TO 3G
MINIPCIE1
MINI PCIE-2
SIM1
SIM_CARD
TV COMPOSITE
ADV7180BCP
U44
74AVCH16T245ZQCLR-X
AME8816BEFHADUZ
TechNexion
USB to SATA & ADV7180
BLIZZARD
Keep the I2C trace as short as possible. And, R1 close the ADV7180 I2C pin.

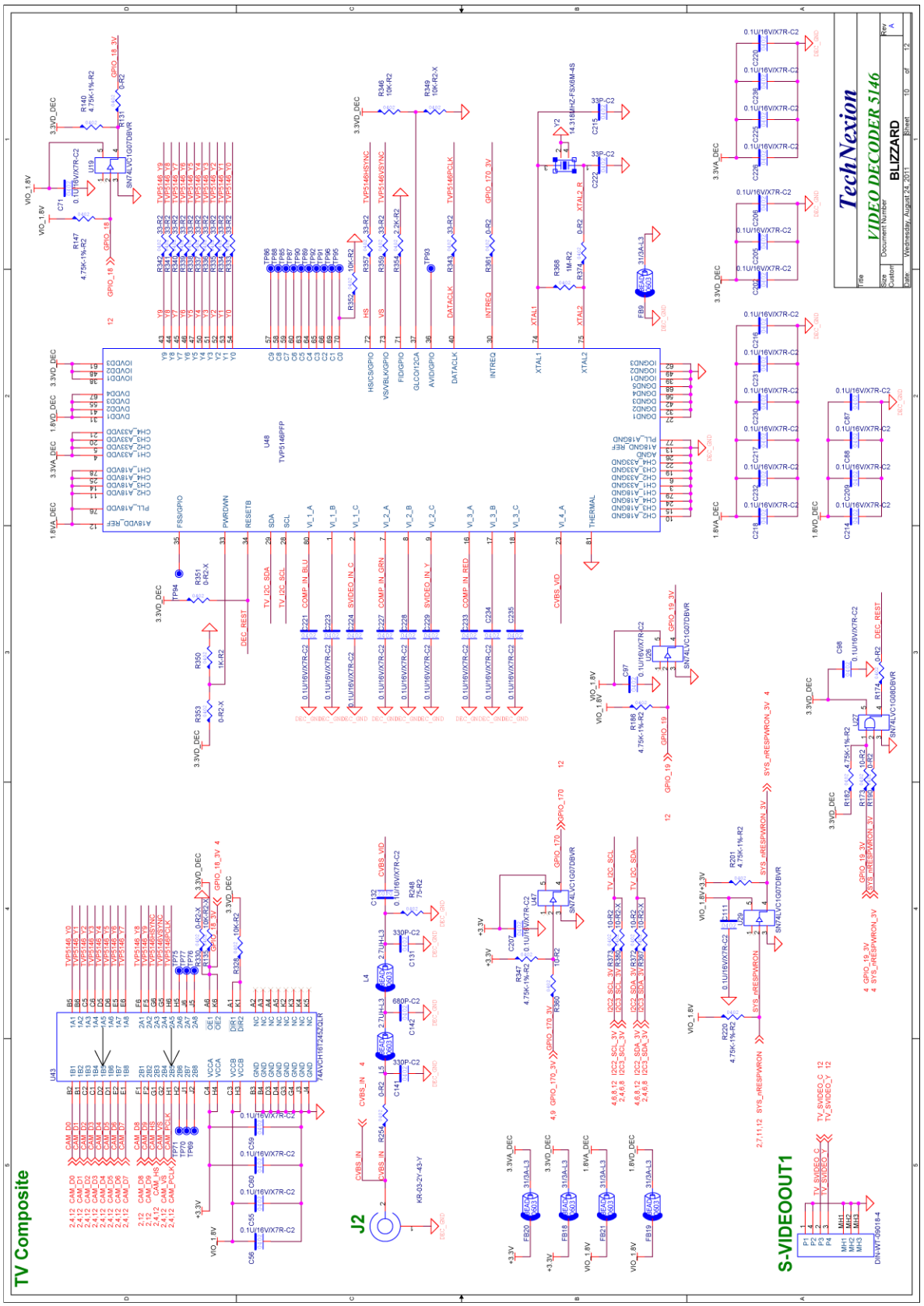

4.3" TTL Panel
LCD Panel, Touchscreen,& Backlight
LCD Buffers/Translators
LCD3
LCD2
TOUCHSCREEN
LED BACKLIGHT
3.3V LCD Power
Touch Screen
TechNexion
TTL
BLIZZARD

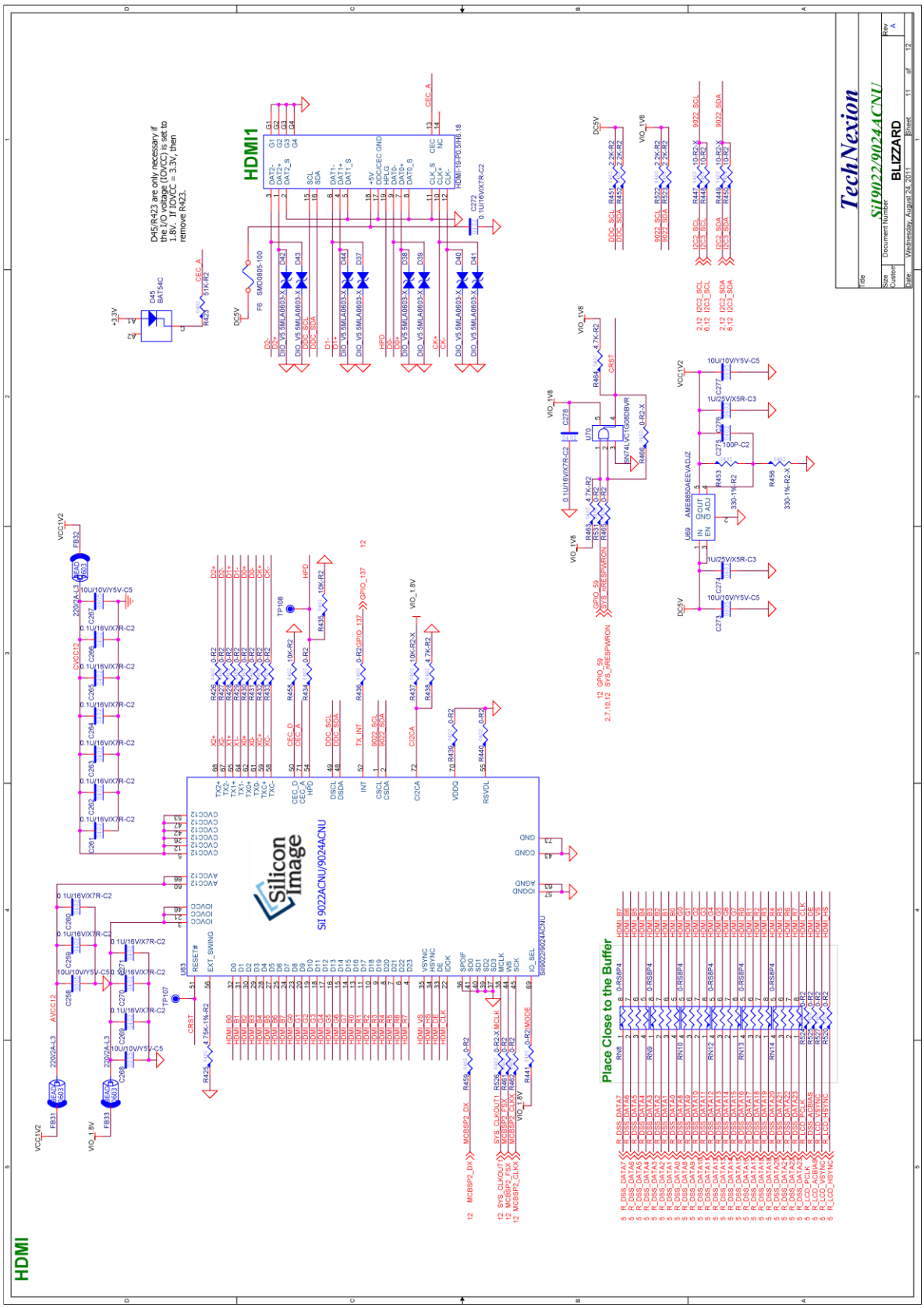

18Bit LVDS
LVDS TRANSMITTER
LVDS1
Place Close to the Buffer
TechNexion
LVDS PANEL
BLIZZARD

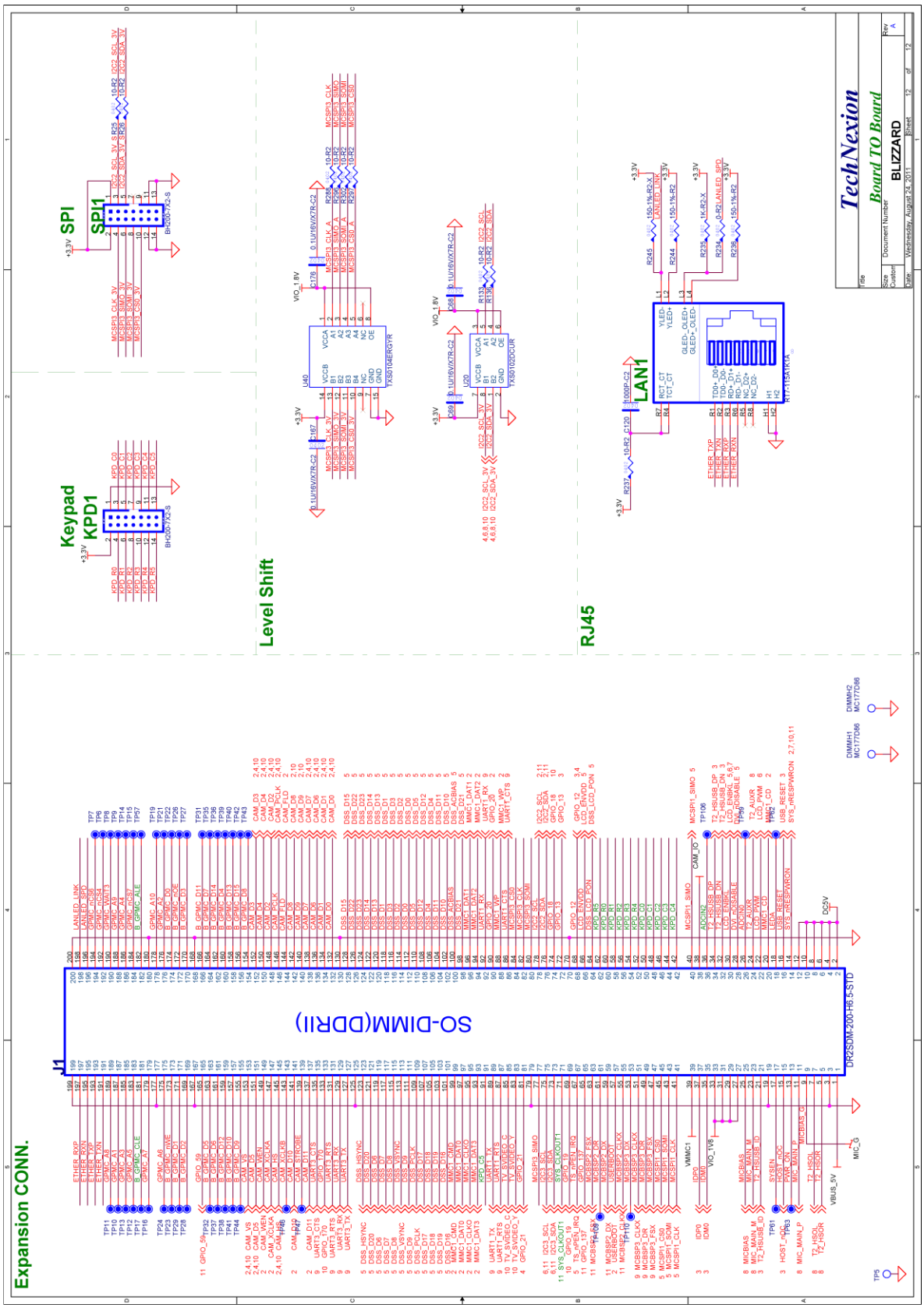

7" TTL PANEL
16V
10.4V
-7V
4V
9.3V
TOUCH1
INNOLUX
LCD1
Place Close to the Buffer
FB=0.195V
TechNexion
7" TTL PANEL
BLIZZARD


Audio-AMP
TTL to VGA
LINEOUT1
LINEIN1
MIC1
LEFT1
RIGHT1
VGA CONNECTOR
VGA1
VGA DAC
ADV7125KST240
TPA2013D2RGPR
Place Close to the Buffer
TechNexion
Amplifier & VGA
BLIZZARD
Wednesday, August 24, 2011


RS-422/485
Level Shift
IR
UART
RS-422/485 SELECT
SW2 RS-422 RS-485
1-4 Short Open
2-3 Open Short
CON1
SW2
SW1
UART1
(422)
(422/485)
TechNexion
UART & RS422/485 & IR
BLIZZARD


TechNexion
VIDEO DECODER 5146
BLIZZARD
TV Composite
S-VIDEOOUT1
J2
U48
TVP5146PFP
U43
74AVCH16T245ZQLR


HDMI
HDMI1
Silicon Image
SII 9022ACNU/9024ACNU
Place Close to the Buffer
TechNexion
SII9022/9024ACNU
BLIZZARD


Expansion CONN.
SO-DIMM(DDRII)
Keypad
KPD1
SPI
SPI1
Level Shift
RJ45
LAN1
TechNexion
Board TO Board
BLIZZARD

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TechNexion hardware products are warranted against defects in materials and workmanship. If TechNexion receives notice of such defects during the warranty period, TechNexion shall, at its option, either repair or replace hardware products that prove to be defective.

1. **Warranty Period**

   The warranty period shall commence on the invoice date. For TechNexion equipment the standard warranty period shall be two-year parts and labor.

2. **Warranty Coverage**

   2.1 This warranty does not apply to any Products that have been repaired or altered by other than TechNexion authorized service person or, which have been subjected to misuse, abuse, accident, or improper installation. TechNexion assumes no liability as a consequence of such events under the terms of this warranty.

   2.2 This warranty does not cover the damage due to the shipping of the Products and external causes, including accident, abuse, misuse or problems with electrical power, usage not in accordance with product instruction, and problems caused by use of parts and components not supplied by TechNexion upon request.

   2.3 This warranty does not cover any items that are in one or more of the following categories:

   a. Software and/or device drivers,
   b. External devices,
   c. Accessories or parts added to Products after the Products shipped from TechNexion and, Accessories, or parts that are not assembled in TechNexion facilities.
   d. All warranty is voided if the TechNexion warranty label or serial number is removed, illegible, or missing

11 Contact Information

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Fax: +886-2-8227 3590