



# BU808DFH

## HIGH VOLTAGE FAST-SWITCHING NPN POWER DARLINGTON TRANSISTOR

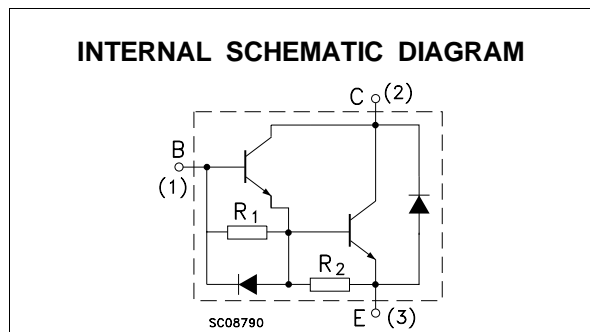
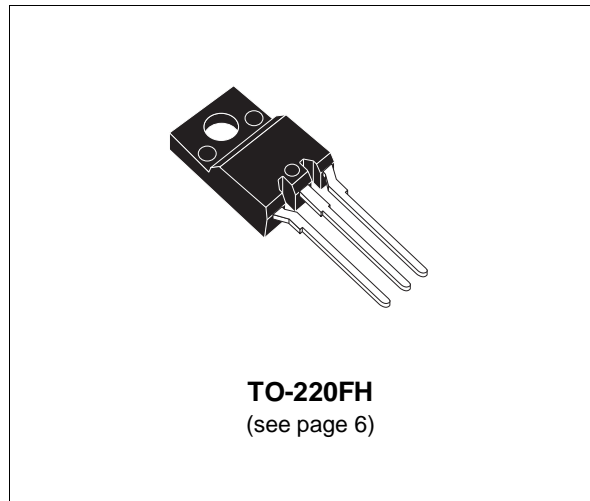
- NEW Fully Plastic TO-220 for HIGH VOLTAGE APPLICATIONS
- NPN MONOLITHIC DARLINGTON WITH INTEGRATED FREE-WHEELING DIODE
- HIGH VOLTAGE CAPABILITY ( $> 1400\text{ V}$ )
- HIGH DC CURRENT GAIN ( TYP. 150 )
- LOW BASE-DRIVE REQUIREMENTS
- DEDICATED APPLICATION NOTE AN1184
- FULLY INSULATED PACKAGE (U.L. COMPLIANT) FOR EASY MOUNTING
- CREEPAGE PATH  $> 4\text{ mm}$

### APPLICATIONS

- COST EFFECTIVE SOLUTION FOR HORIZONTAL DEFLECTION IN LOW END TV UP TO 21 INCHES.

### DESCRIPTION

The BU808DFH is a NPN transistor in monolithic Darlington configuration. It is manufactured using Multi-epitaxial Mesa technology for cost-effective high performance.



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CBO}$	Collector-Base Voltage ( $I_E = 0$ )	1400	V
$V_{CEO}$	Collector-Emitter Voltage ( $I_B = 0$ )	700	V
$V_{EBO}$	Emitter-Base Voltage ( $I_C = 0$ )	5	V
$I_C$	Collector Current	8	A
$I_{CM}$	Collector Peak Current ( $t_p < 5\text{ ms}$ )	10	A
$I_B$	Base Current	3	A
$I_{BM}$	Base Peak Current ( $t_p < 5\text{ ms}$ )	6	A
$P_{tot}$	Total Dissipation at $T_c = 25\text{ }^\circ\text{C}$	42	W
$V_{isol}$	Insulation Withstand Voltage (RMS) from All Three Leads to External Heatsink	2500	V
$T_{stg}$	Storage Temperature	-65 to 150	$^\circ\text{C}$
$T_j$	Max. Operating Junction Temperature	150	$^\circ\text{C}$

# BU808DFH

## THERMAL DATA

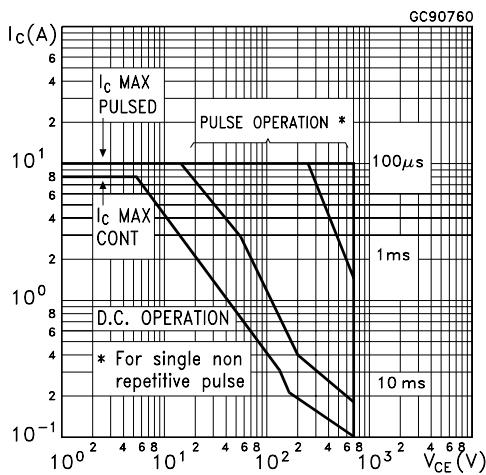
R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	2.98	°C/W
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## ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

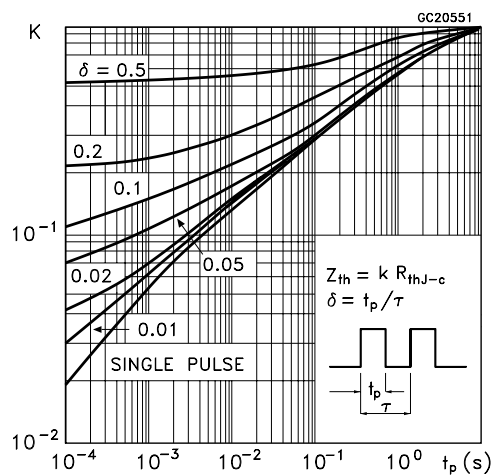
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I <sub>CES</sub>	Collector Cut-off Current (V <sub>BE</sub> = 0)	V <sub>CE</sub> = 1400 V			400	μA
I <sub>EBO</sub>	Emitter Cut-off Current (I <sub>C</sub> = 0)	V <sub>EB</sub> = 5 V			100	mA
V <sub>CE(sat)*</sub>	Collector-Emitter Saturation Voltage	I <sub>C</sub> = 5 A    I <sub>B</sub> = 0.5 A			1.6	V
V <sub>BE(sat)*</sub>	Base-Emitter Saturation Voltage	I <sub>C</sub> = 5 A    I <sub>B</sub> = 0.5 A			2.1	V
h <sub>FE*</sub>	DC Current Gain	I <sub>C</sub> = 5 A    V <sub>CE</sub> = 5 V I <sub>C</sub> = 5 A    V <sub>CE</sub> = 5 V    T <sub>C</sub> = 100 °C	60 20		230	
t <sub>s</sub> t <sub>f</sub>	INDUCTIVE LOAD Storage Time Fall Time	V <sub>CC</sub> = 150 V    I <sub>C</sub> = 5 A I <sub>B1</sub> = 0.5 A    V <sub>BE(off)</sub> = -5 V			3 0.8	μs μs
t <sub>s</sub> t <sub>f</sub>	INDUCTIVE LOAD Storage Time Fall Time	V <sub>CC</sub> = 150 V    I <sub>C</sub> = 5 A I <sub>B1</sub> = 0.5 A    V <sub>BE(off)</sub> = -5 V T <sub>C</sub> = 100 °C		2 0.8		μs μs
V <sub>F</sub>	Diode Forward Voltage	I <sub>F</sub> = 5 A			3	V

\* Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %

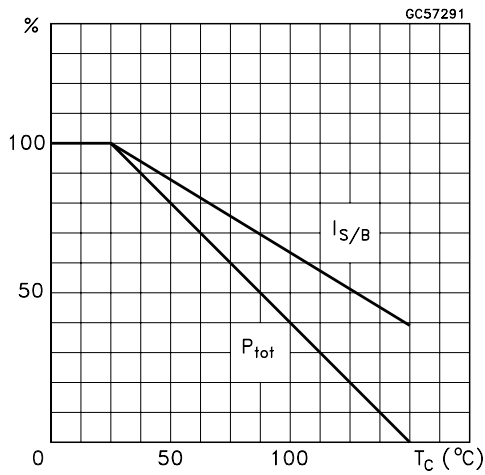
## Safe Operating Area



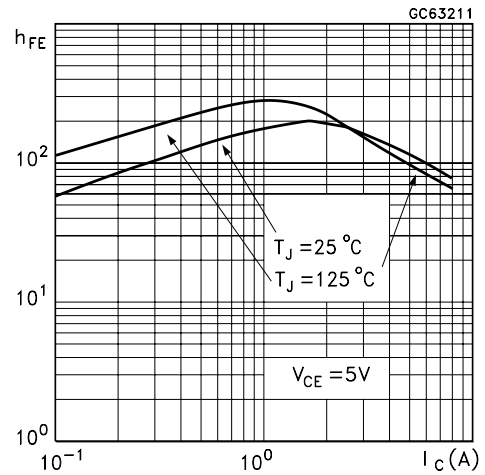
## Thermal Impedance



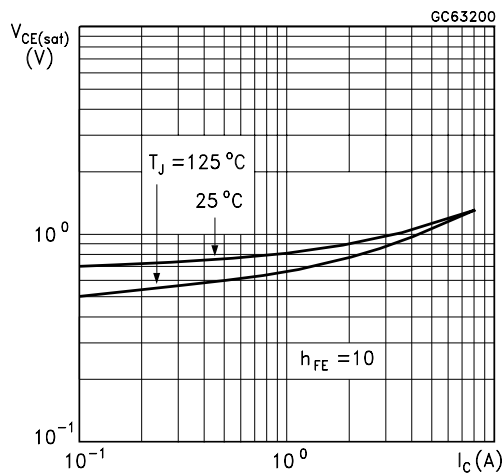
Derating Curve



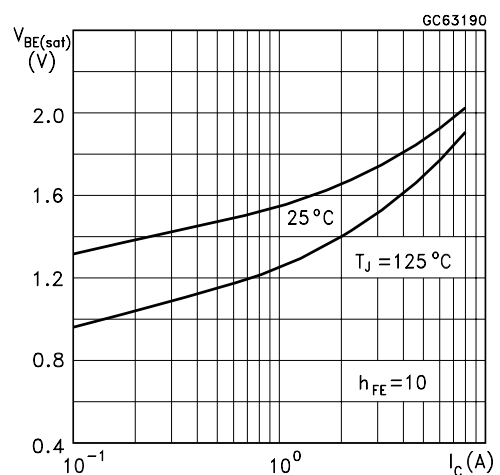
DC Current Gain



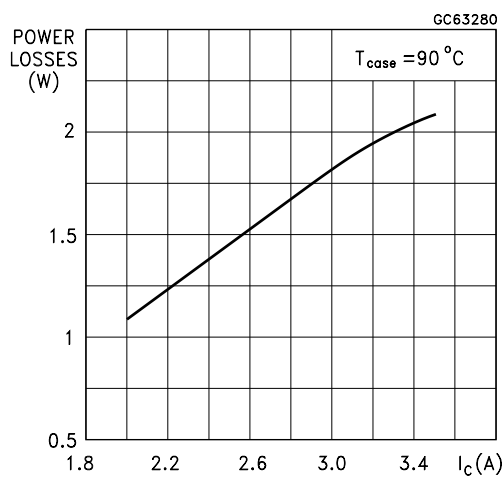
Collector Emitter Saturation Voltage



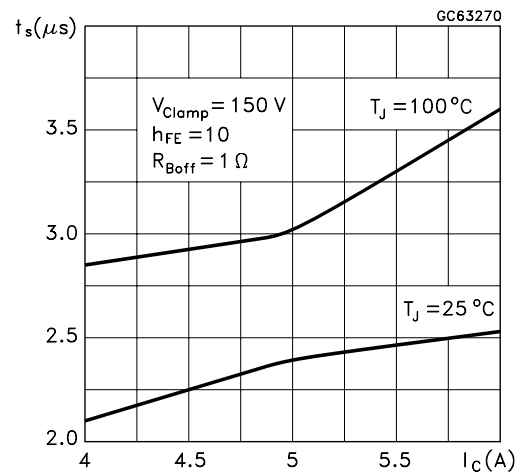
Base Emitter Saturation Voltage



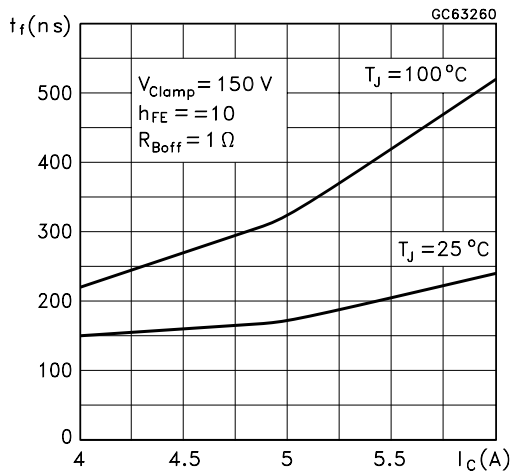
Power Losses at 16 KHz



Switching Time Inductive Load at 16KHz



Switching Time Inductive Load at 16KHZ

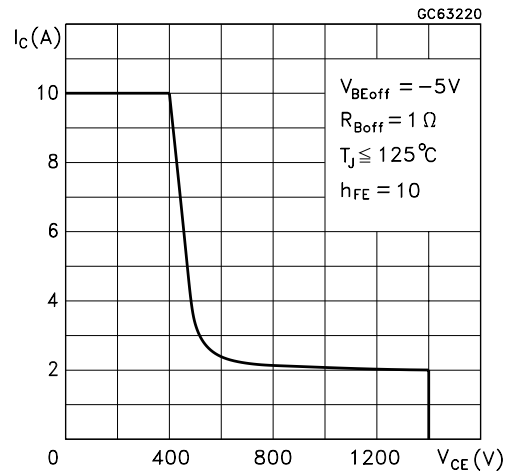


**BASE DRIVE INFORMATION**

In order to saturate the power switch and reduce conduction losses, adequate direct base current  $I_{B1}$  has to be provided for the lowest gain  $h_{FE}$  at  $100\ ^\circ\text{C}$  (line scan phase). On the other hand, negative base current  $I_{B2}$  must be provided to turn off the power transistor (retrace phase).

Most of the dissipation, in the deflection application, occurs at switch-off. Therefore it is essential to determine the value of  $I_{B2}$  which minimizes power losses, fall time  $t_f$  and, consequently,  $T_j$ . A new set of curves have been defined to give total power losses,  $t_s$  and  $t_f$  as a function of  $I_{B2}$  at both 16 KHz scanning frequencies for choosing the optimum negative

Reverse Biased SOA



drive. The test circuit is illustrated in figure 1.

Inductance  $L_1$  serves to control the slope of the negative base current  $I_{B2}$  to recombine the excess carrier in the collector when base current is still present, this would avoid any tailing phenomenon in the collector current.

The values of  $L$  and  $C$  are calculated from the following equations:

$$\frac{1}{2} L (I_C)^2 = \frac{1}{2} C (V_{CEfly})^2 \quad \omega = 2\pi f = \frac{1}{\sqrt{LC}}$$

Where  $I_C$  = operating collector current,  $V_{CEfly}$  = flyback voltage,  $f$  = frequency of oscillation during retrace.

Figure 1: Inductive Load Switching Test Circuits.

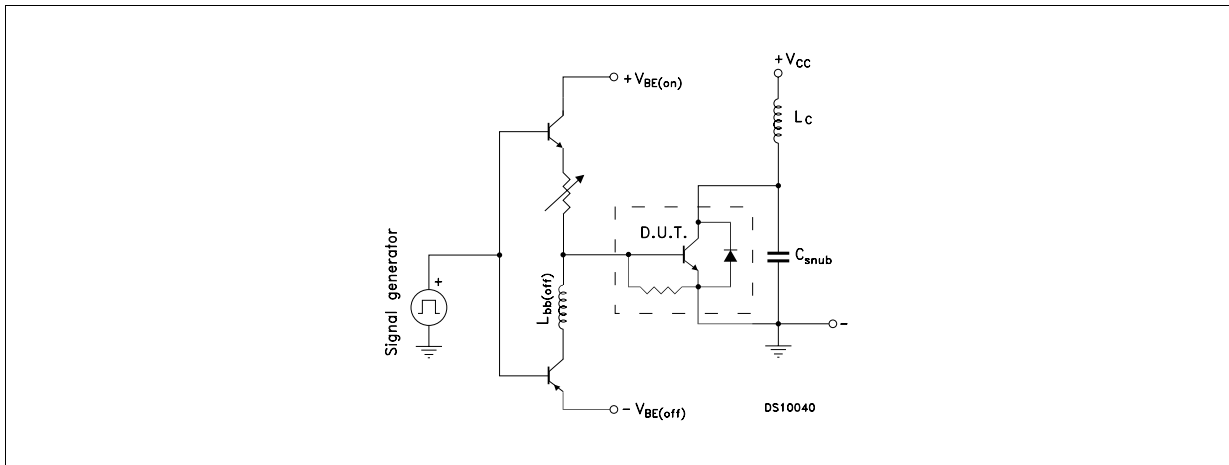
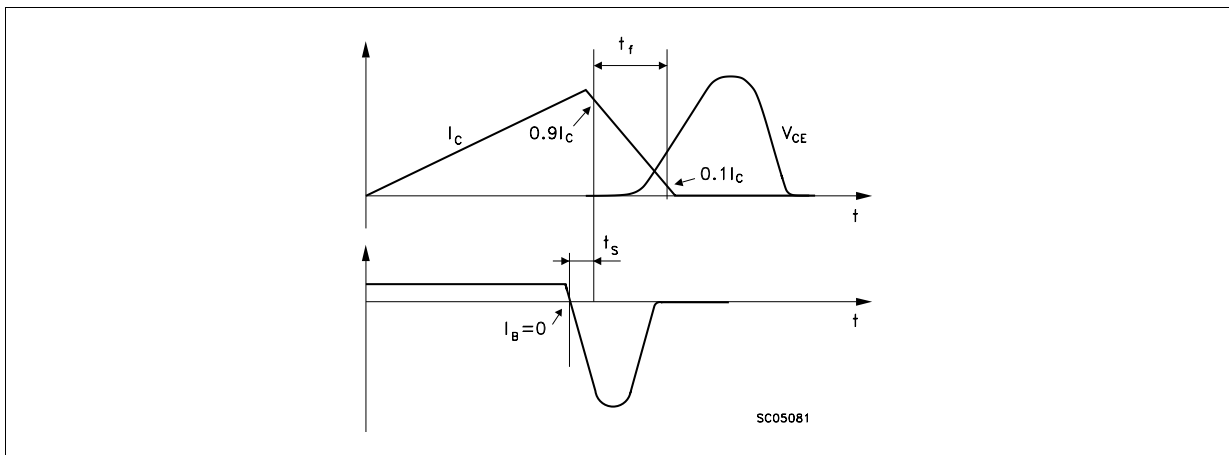
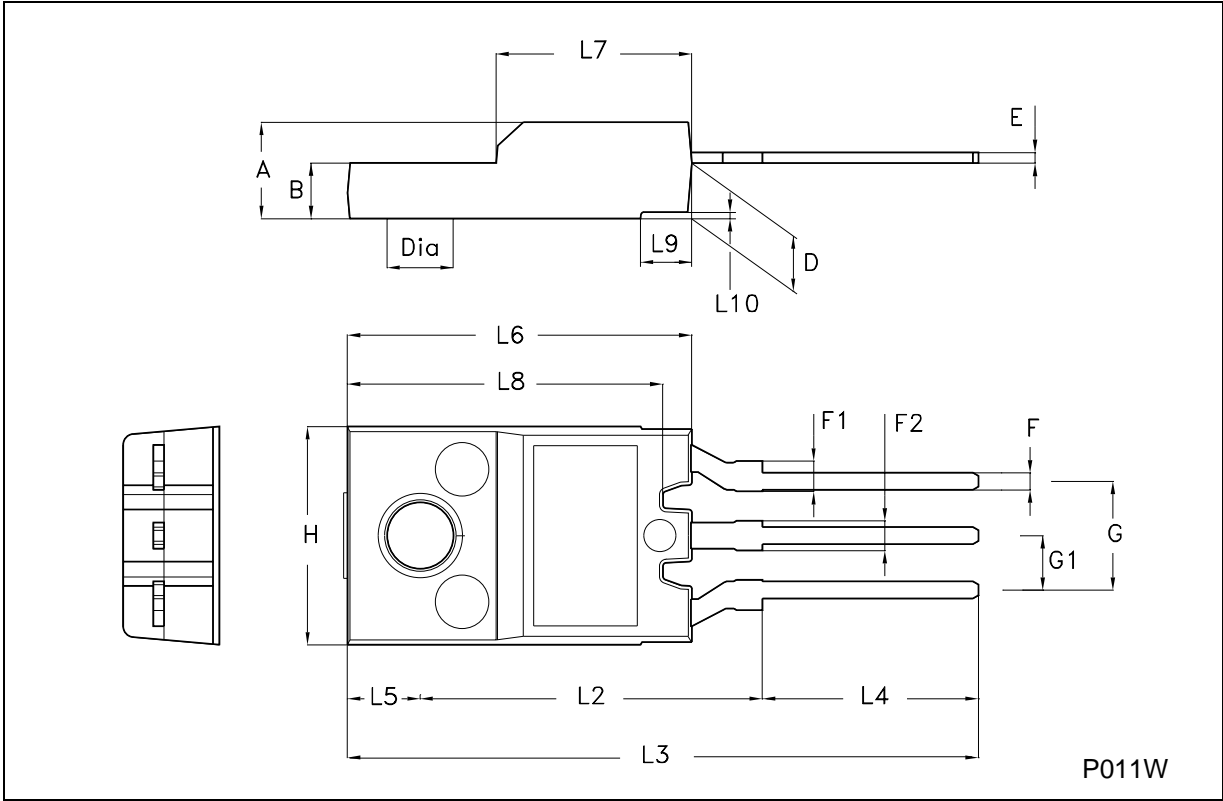


Figure 2: Switching Waveforms in a Deflection Circuit



**TO-220FH (Fully plastic High voltage) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.3		1.8	0.051		0.070
F2	1.3		1.8	0.051		0.070
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L5		3.4			0.134	
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
L8	14.5		15	0.570		0.590
L9		2.4			0.094	



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