



STH260N6F6-2 STP260N6F6

N-channel 60 V, 0.0016 Ω , 180 A TO-220, H²PAK-2
STripFET™ DeepGATE™ VI Power MOSFET

Preliminary data

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STH260N6F6-2	60 V	< 0.002 Ω	180 A
STP260N6F6	60 V	< 0.003 Ω	120 A

- N-channel enhancement mode
- 100% avalanche rated
- Low gate charge
- Very low on-resistance

Application

- Switching applications

Description

This STripFET™ DeepGATE™ Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance, with a new gate structure, providing superior switching performances.

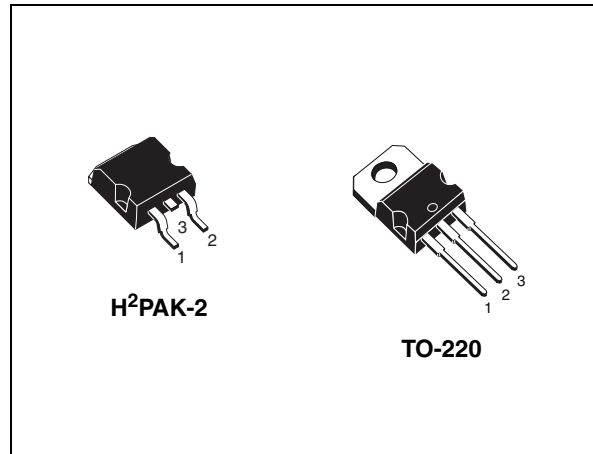


Figure 1. Internal schematic diagram

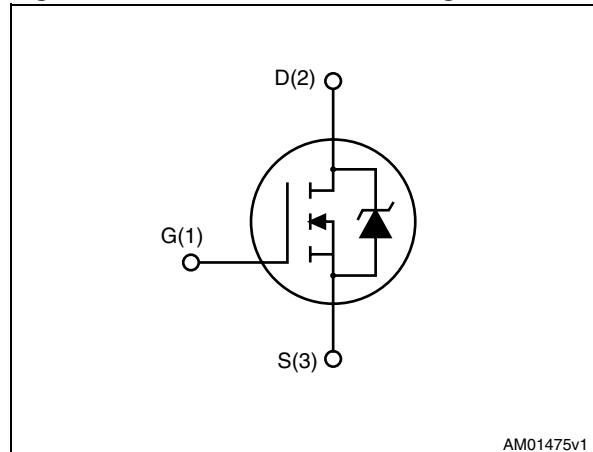


Table 1. Device summary

Order code	Marking	Package	Packaging
STH260N6F6-2	260N6F6	H ² PAK-2	Tape and reel
STP260N6F6	260N6F6	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	H ² PAK-2	
V _{DS}	Drain-source voltage (V _{GS} = 0)	75		V
V _{GS}	Gate-source voltage	± 20		V
I _D	Drain current (continuous) at T _C = 25 °C	120	180	A
I _D	Drain current (continuous) at T _C = 100 °C	134	170	A
I _{DM} ⁽¹⁾	Drain current (pulsed)	480	720	A
P _{TOT}	Total dissipation at T _C = 25 °C	300		W
	Derating factor	1	0.8	W/°C
E _{AS} ⁽²⁾	Single pulse avalanche energy	TBD		mJ
T _{stg}	Storage temperature	- 55 to 175		°C
T _j	Operating junction temperature			

1. Current limited by package.
2. Starting T_j = 25 °C, I_D = 35 A, V_{DD} = 50 V.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	H ² PAK-2	
R _{thj-case}	Thermal resistance junction-case max	0.5		°C/W
R _{thj-a}	Thermal resistance junction-ambient max	62.5		°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max		35	°C/W
T _l	Maximum lead temperature for soldering purpose	300		°C

1. When mounted on FR-4 board of 1 inch², 2 oz Cu.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$			1	μA
		$V_{DS} = \text{max rating}$, $T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	For H ² PAK-2 $V_{GS} = 10\text{ V}$, $I_D = 90\text{ A}$		1.6	2	m Ω
		For TO-220 $V_{GS} = 10\text{ V}$, $I_D = 60\text{ A}$		2.4	3	

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit		
C_{iss}	Input capacitance			10500		pF		
C_{oss}	Output capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	780	-	pF		
C_{rss}	Reverse transfer capacitance						440	pF
Q_g	Total gate charge	$V_{DD} = 30\text{ V}$, $I_D = 120\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 3)	-	150	-	nC		
Q_{gs}	Gate-source charge						TBD	nC
Q_{gd}	Gate-drain charge						TBD	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$ t_r	Turn-on delay time	$V_{DD} = 30\text{ V}$, $I_D = 60\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2)	-	TBD	-	ns	
	Rise time						TBD
$t_{d(off)}$ t_f	Turn-off-delay time						TBD
	Fall time	TBD	ns				

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current	For TO-220	-		120	A
		For H ² PAK-2	-		180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)	TO-220	-		480	A
		H ² PAK-2	-		720	A
$V_{SD}^{(2)}$	Forward on voltage	For TO-220 $I_{SD} = 120\text{ A}, V_{GS} = 0$	-		TBD	V
		For H ² PAK-2 $I_{SD} = 180\text{ A}, V_{GS} = 0$				
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 120\text{ A}, V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 4)	-	TBD TBD TBD		ns nC A

1. Current limited by package.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

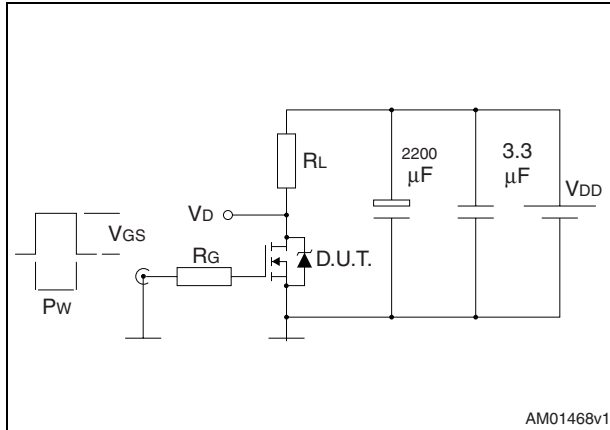


Figure 3. Gate charge test circuit

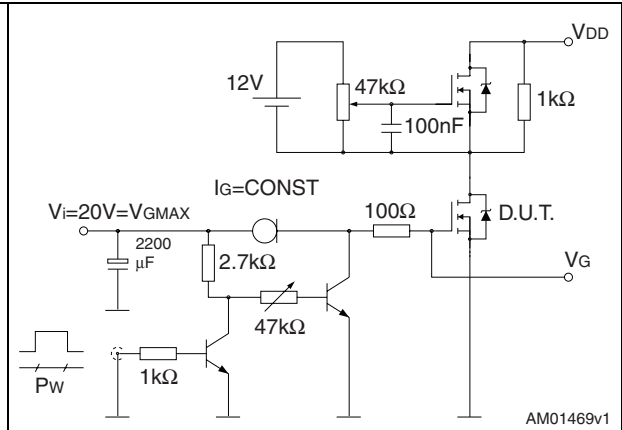


Figure 4. Test circuit for inductive load switching and diode recovery times

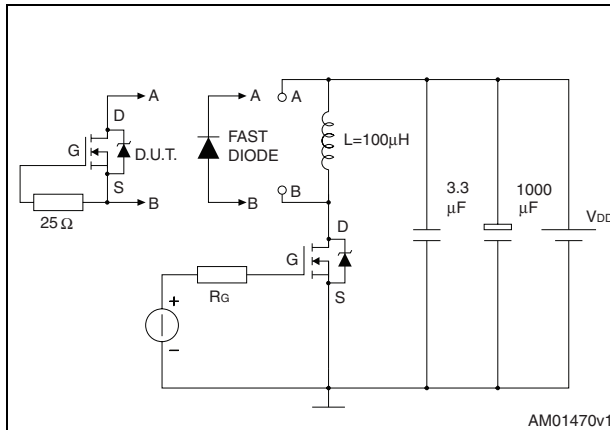


Figure 5. Unclamped inductive load test circuit

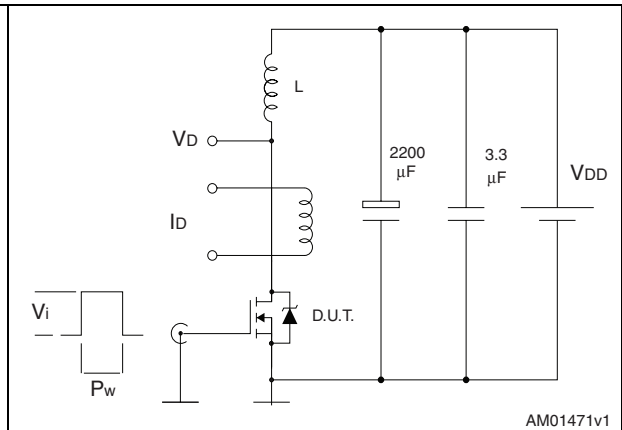


Figure 6. Unclamped inductive waveform

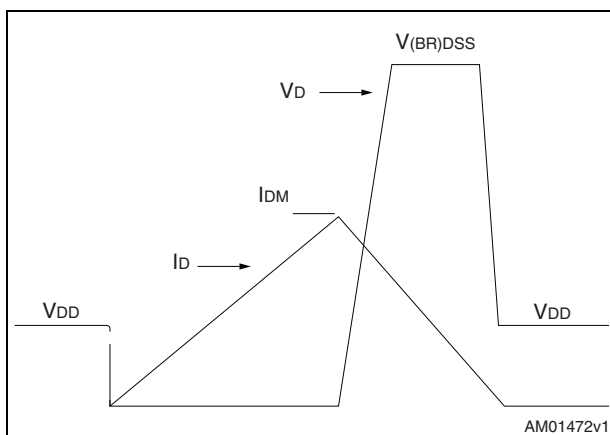
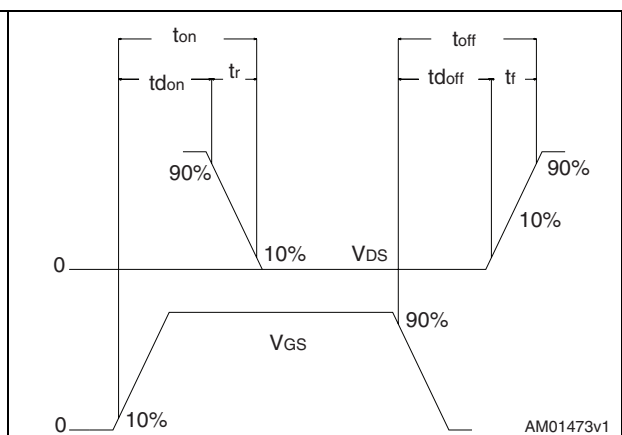


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. H²PAK 2 leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.171		7.971
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	7.45		7.85
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 8. H²PAK 2 leads drawing

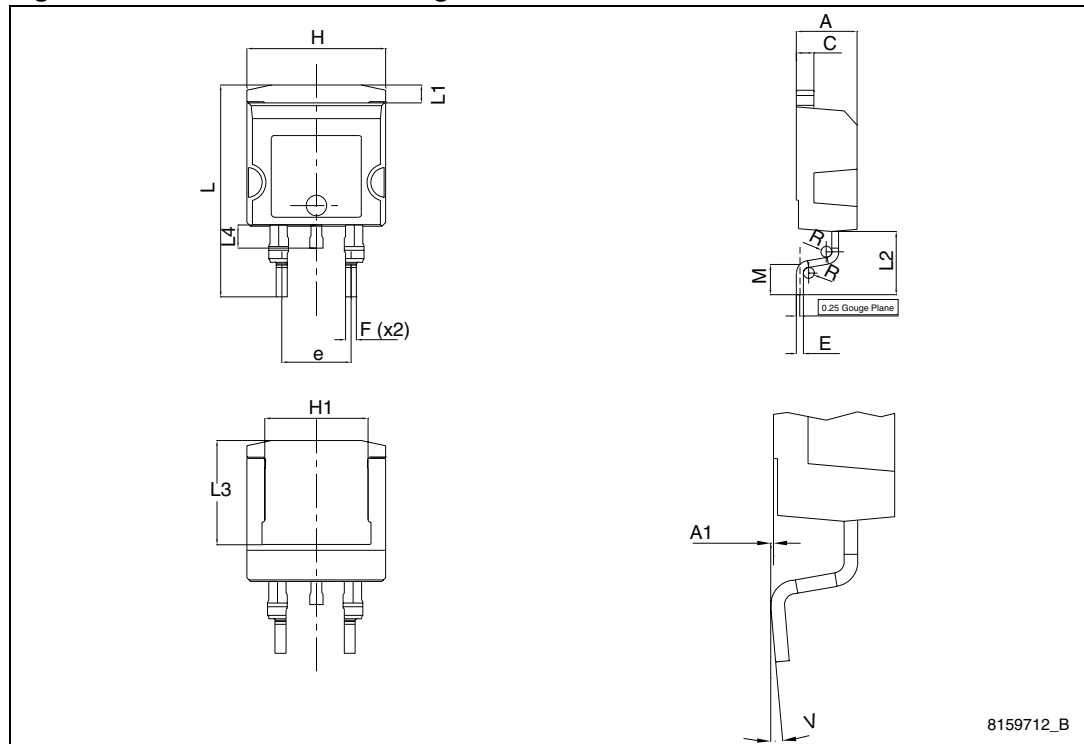
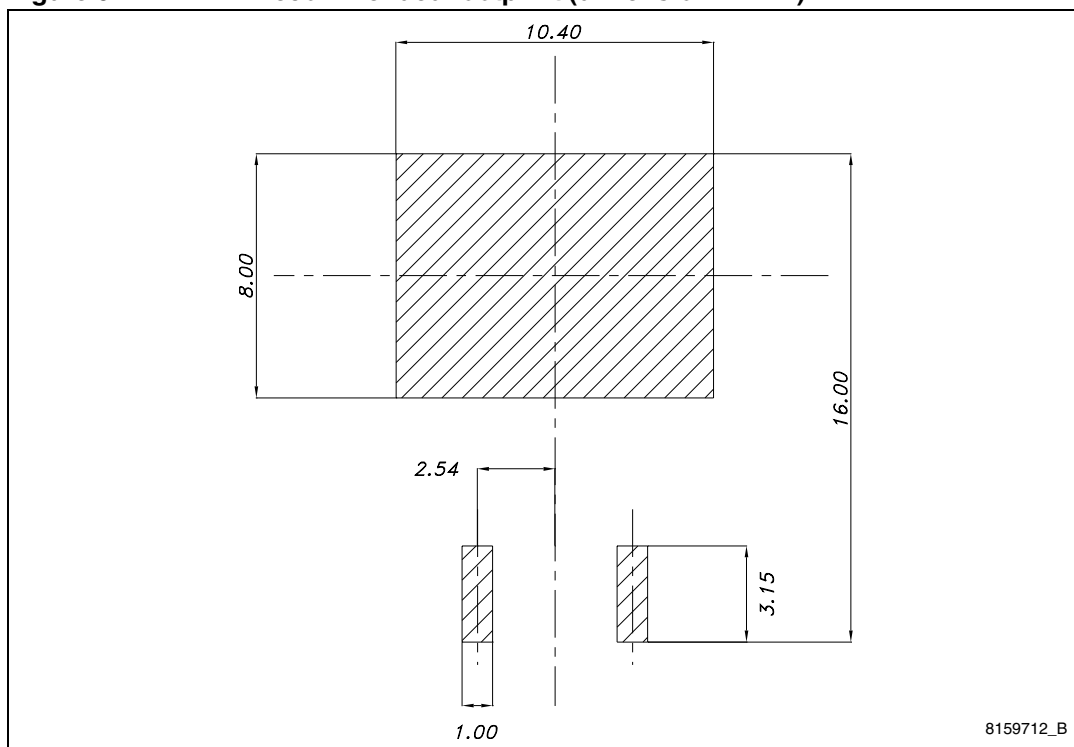


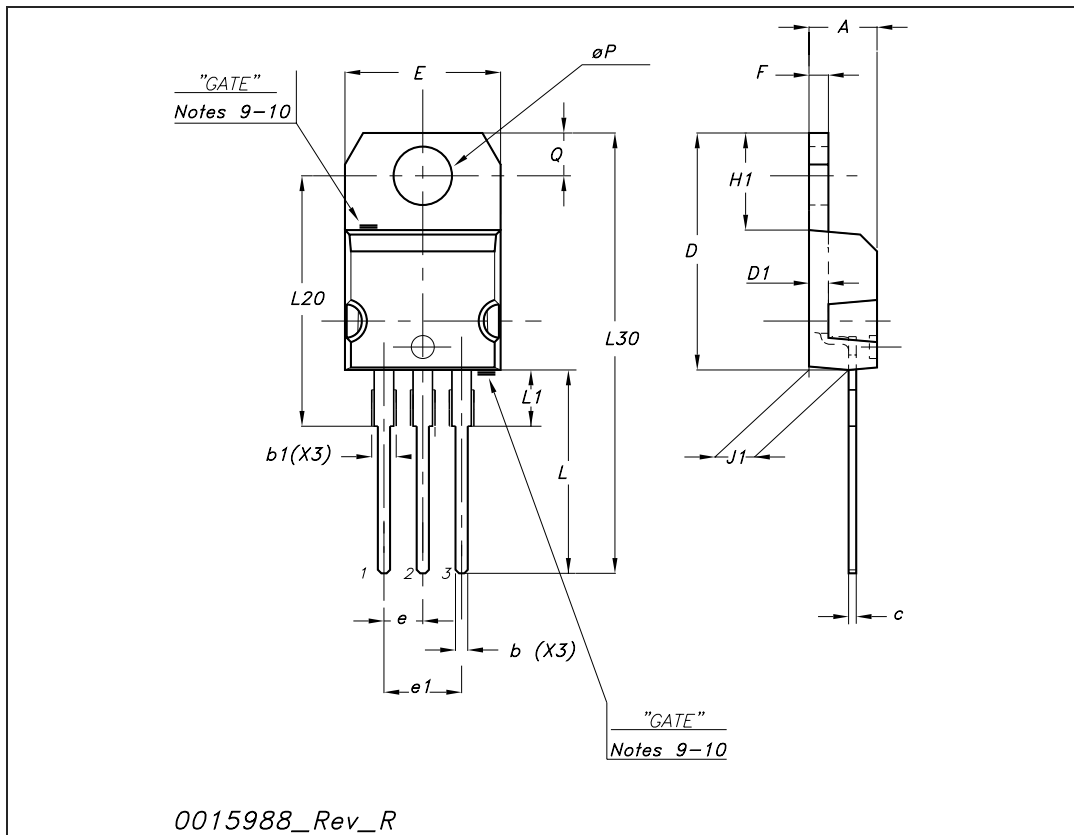
Figure 9. H²PAK2 recommended footprint (dimension in mm)



8159712_B

TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
07-May-2010	1	First release.

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