TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS032C – Revised October 2003

CD4027B Types

CMOS Dual J-K Master-Slave Flip-Flop

High-Voltage Types (20-Volt Rating)

■ CD4027B is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA-CD4013B dual D-type flip-flop.

The CD4027B is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

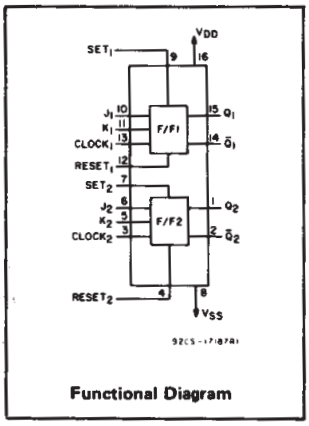
The CD4027B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

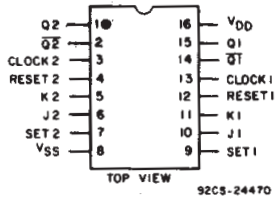
- Set-Reset capability
- Static flip-flop operation – retains state indefinitely with clock level either "high" or "low"
- Medium speed operation – 16 MHz (typ.) clock toggle rate at 10 V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Registers, counters, control circuits



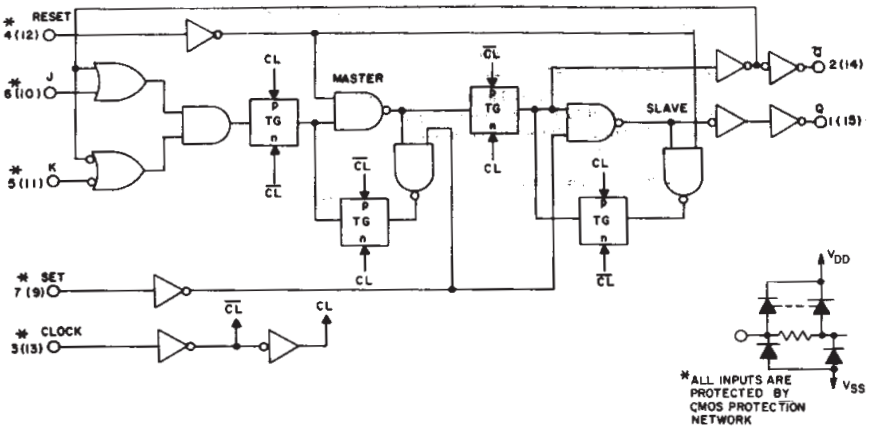
Functional Diagram



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C



PRESENT STATE						NEXT STATE	
INPUTS				OUTPUT	CL*	OUTPUTS	
J	K	S	R	Q		Q	Q̄
1	X	0	0	0	↑	1	0
X	0	0	0	1	↑	1	0
0	X	0	0	0	↑	0	1
X	1	0	0	1	↑	0	1
X	X	0	0	X	↓		← NO CHANGE
X	X	1	0	X	X	1	0
X	X	0	1	X	X	0	1
X	X	1	1	X	X	1	1

LOGIC 1 = HIGH LEVEL
LOGIC 0 = LOW LEVEL
↑ = LEVEL CHANGE
X = DON'T CARE

92CM-27551R1

Fig. 1 – Logic diagram and truth table for CD4027B (one of two identical J-K flip flops).

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS All Packages Min.	LIMITS All Packages Max.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)		–	3	18	V
Data Setup Time	t_S	5	200	–	ns
		10	75	–	
		15	50	–	
Clock Pulse Width	t_W	5	140	–	ns
		10	60	–	
		15	40	–	
Clock Input Frequency (Toggle Mode)	f_{CL}	5		3.5	MHz
		10	dc	8	
		15		12	
Clock Rise or Fall Time	t_rCL*, t_fCL	5	–	45	μs
		10	–	5	
		15	–	2	
Set or Reset Pulse Width	t_W	5	180	–	ns
		10	80	–	
		15	50	–	

* If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

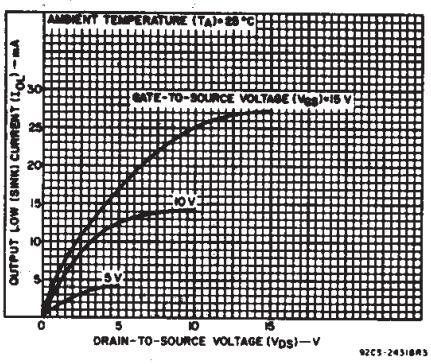


Fig.2 – Typical output low (sink) current characteristics.

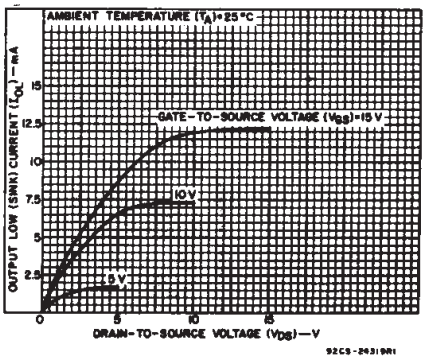


Fig.3 – Minimum output low (sink) current characteristics.

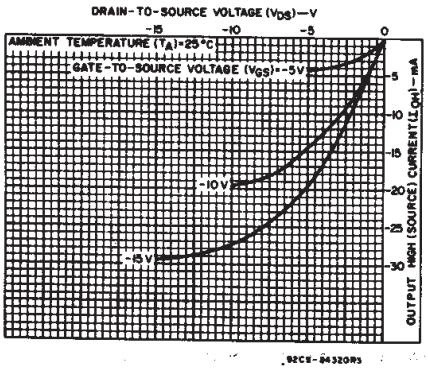


Fig.4 – Typical output high (source) current characteristics.

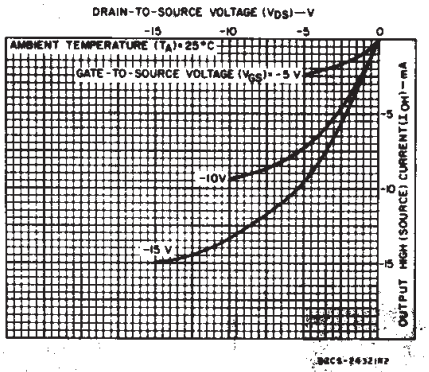


Fig.5 – Minimum output high (source) current characteristics.

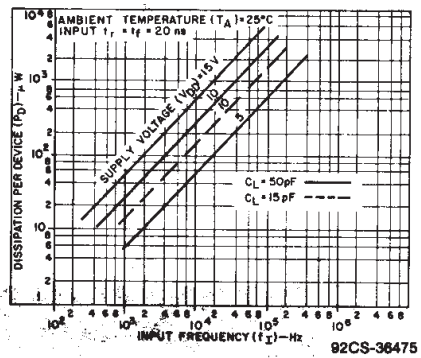


Fig.6 – Typical power dissipation vs. frequency.

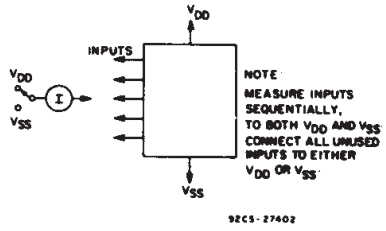


Fig.7 – Input current test circuit.

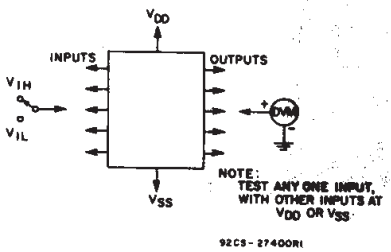


Fig.8 – Input-voltage test circuit.

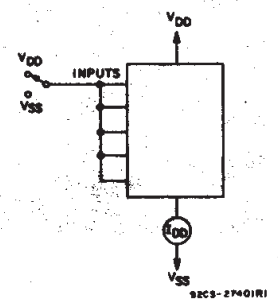
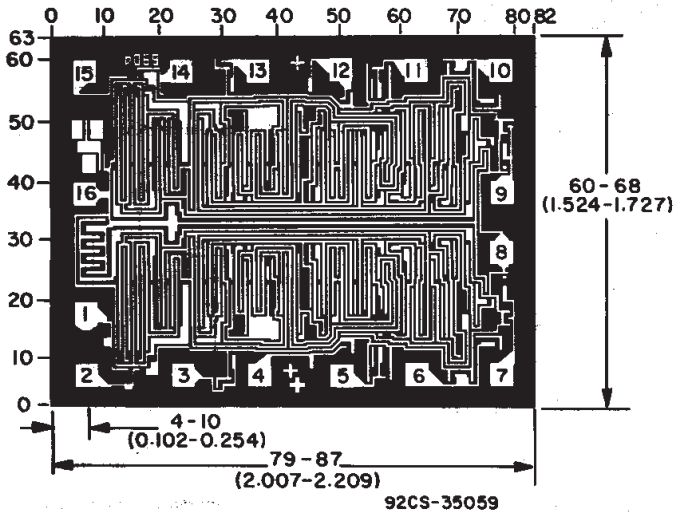


Fig.9 – Quiescent device current test circuit.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA



Dimensions in millimeters are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3}).

Dimensions and Pad Layout for CD4027BH

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS All Packages Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Q or $\bar{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to Q or Reset to $\bar{Q}$ t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to $\bar{Q}$ or Reset to Q t_{PHL}	5	–	200	400	ns
	10	–	85	170	
	15	–	60	120	
Transition Time t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency# (Toggle Mode) f_{CL}	5	3.5	7	–	MHz
	10	8	16	–	
	15	12	24	–	
Minimum Clock Pulse Width t_W	5	–	70	140	ns
	10	–	30	60	
	15	–	20	40	
Minimum Set or Reset Pulse Width t_W	5	–	90	180	ns
	10	–	40	80	
	15	–	25	50	
Minimum Data Setup Time t_S	5	–	100	200	ns
	10	–	35	75	
	15	–	25	50	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}	5	–	–	45	μs
	10	–	–	5	
	15	–	–	2	
Input Capacitance C_I		–	5	7.5	pF

Input t_r, t_f = 5 ns.

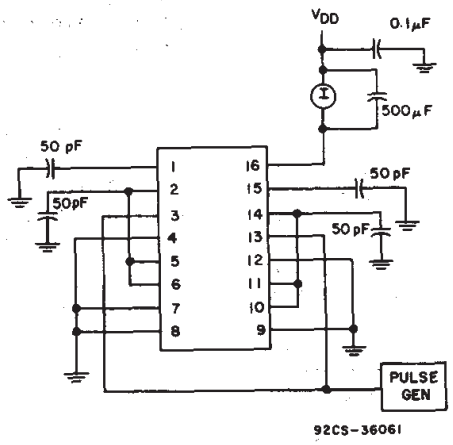


Fig. 13—Dynamic power dissipation test circuit.

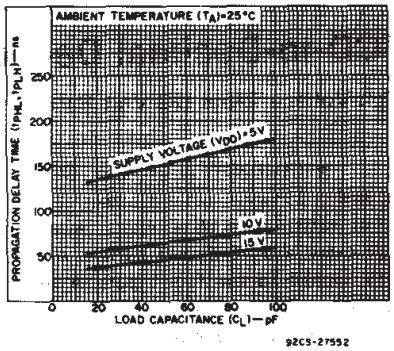


Fig. 10 – Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to $\bar{Q}$.

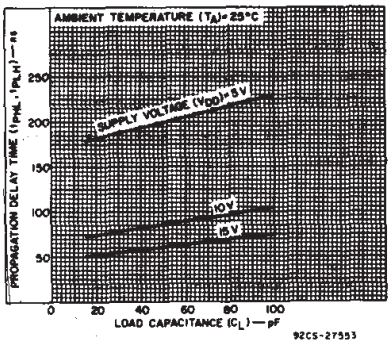


Fig. 11 – Typical propagation delay time vs. load capacitance (SET to $\bar{Q}$ or RESET to Q).

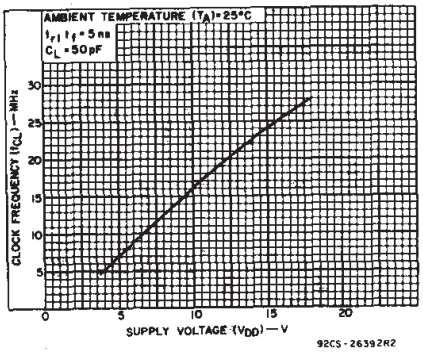
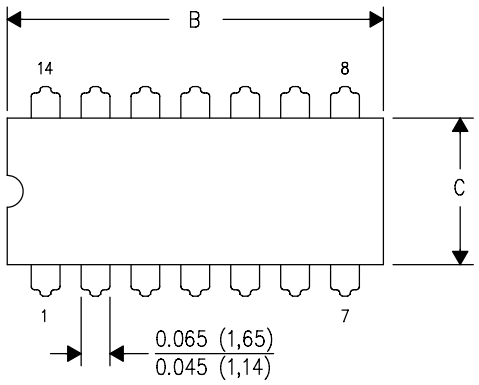


Fig. 12 – Typical maximum clock frequency vs. supply voltage (toggle mode).

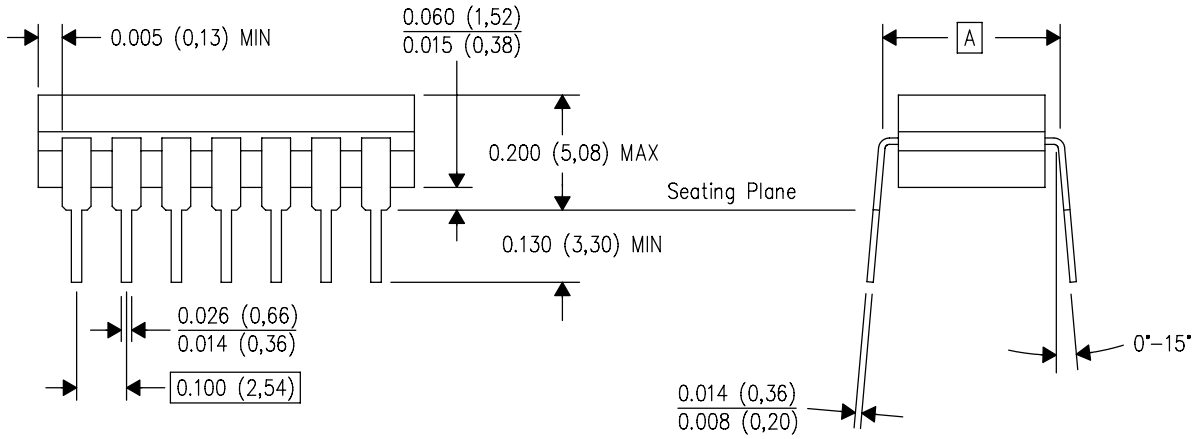
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



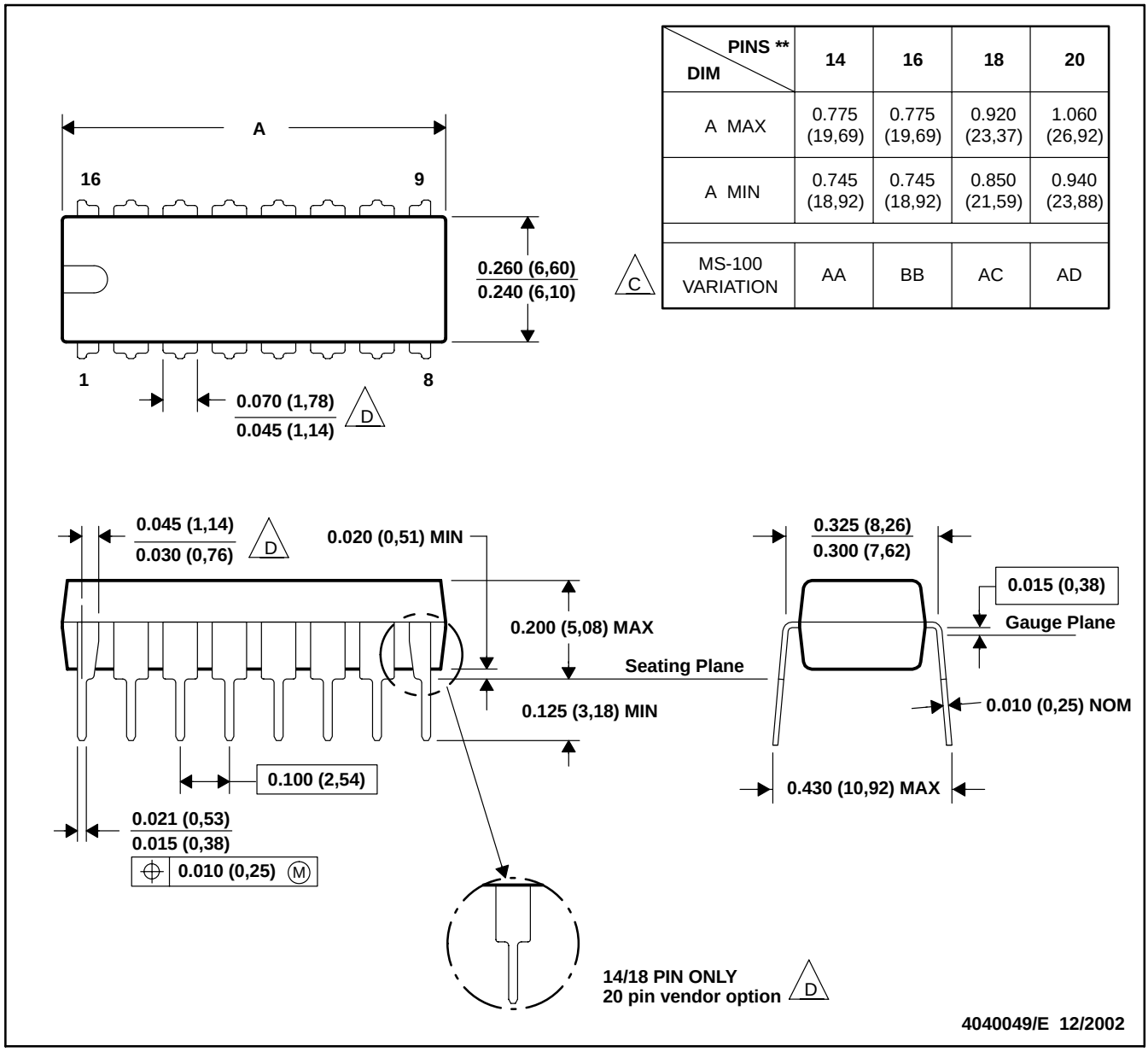
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).

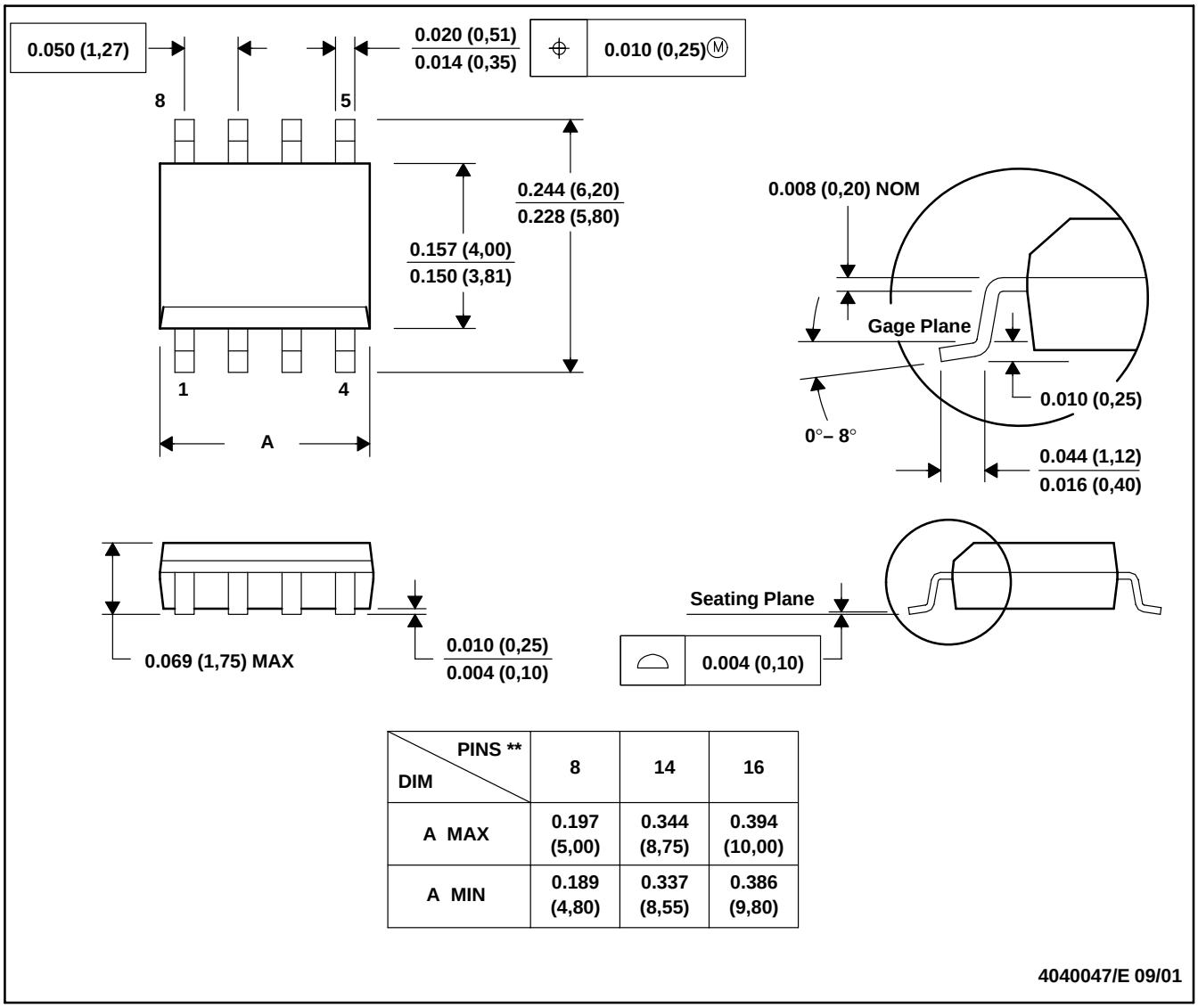
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

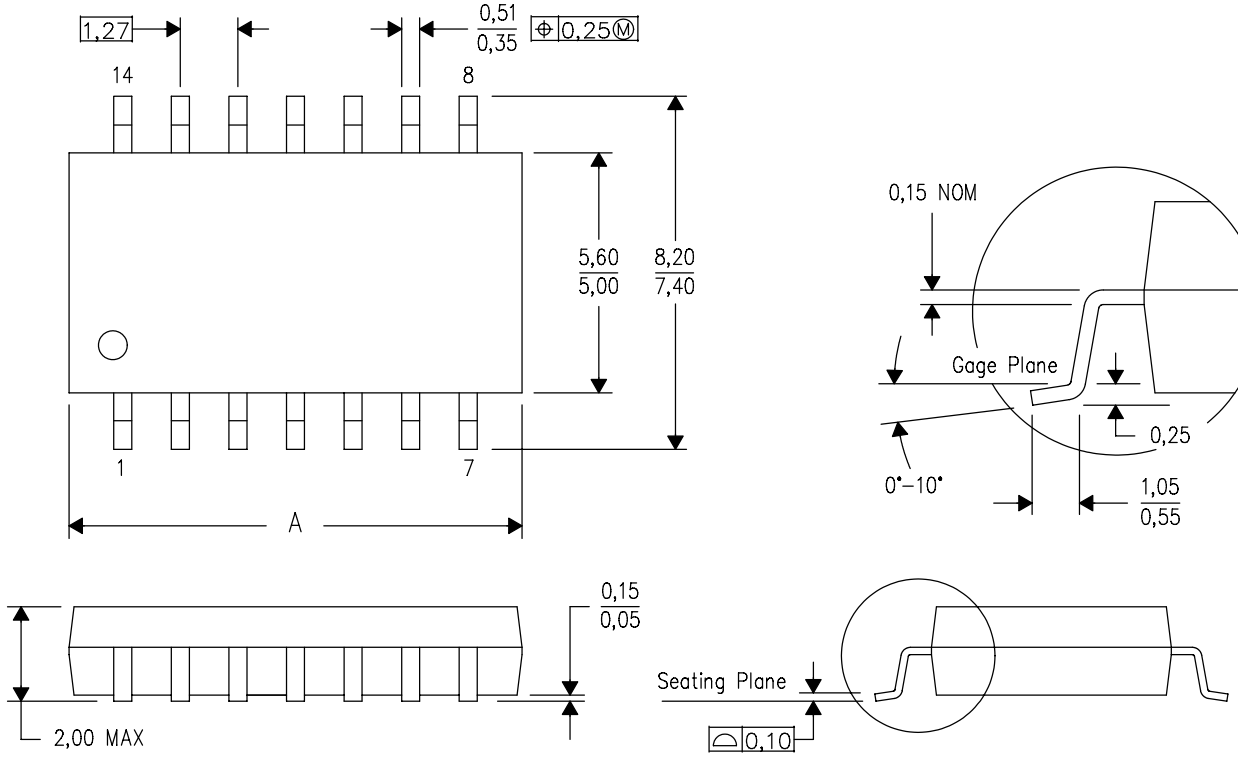
4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



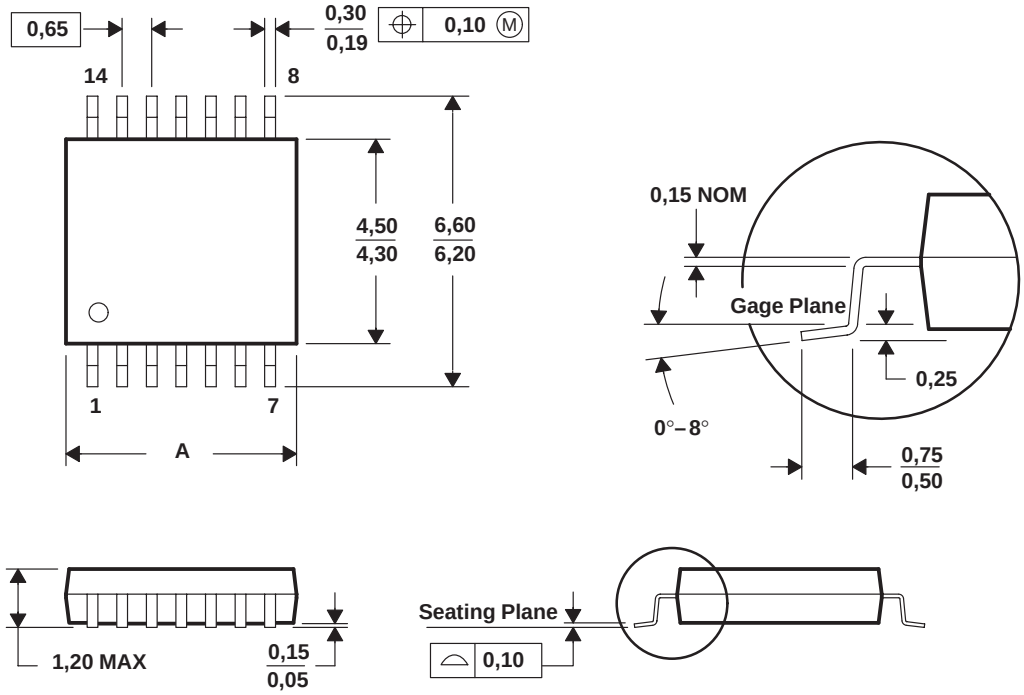
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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