SCHS228A - SEPTEMBER 1998 - REVISED NOVEMBER 2002

- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Greater Noise Immunity Than Standard Inverters
- Operates With Much Slower Than Standard Input Rise and Fall Slew Rates
- Balanced Propagation Delays
- ±24-mA Output Drive Current
  - Fanout to 15 F Devices
- SCR Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

#### **E OR M PACKAGE** (TOP VIEW) 14 🛮 V<sub>CC</sub> 1Y [ 13 6A 2 2A 🛮 3 12 6Y 2Y 👖 5A 4 3A 🛮 5 □ 5Y 3Y **[** 6 9**∏** 4A GND [] 7 8 **∏** 4Y

### description/ordering information

The CD74AC14 contains six independent inverters. This device performs the Boolean function  $Y = \overline{A}$ .

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going  $(V_{T+})$  and negative-going  $(V_{T-})$  signals.

#### **ORDERING INFORMATION**

TA	PACKA	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – E	Tube	CD74AC14E	CD74AC14E
–55°C to 125°C	C to 125°C SOIC – M		CD74AC14M	AC14M
			CD74AC14M96	AC 14IVI

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

### logic diagram, each inverter (positive logic)





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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 6 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): E package	80°C/W
M package	86°C/W
Storage temperature range, T <sub>stg</sub>	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

				T <sub>A</sub> = 25°C		–55°C to 125°C		–40°C to 85°C	
			MIN	MAX	MIN	MAX	MIN	MAX	
VCC	V <sub>CC</sub> Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
VI	Input voltage		0	VCC	0	VCC	0	VCC	V
٧o	V <sub>O</sub> Output voltage		0	VCC	0	VCC	0	VCC	V
ЮН	High-level output current $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$			-24		-24		-24	mA
loL	ow-level output current V <sub>CC</sub> = 4.5 V to 5.5 V			24		24		24	mA
Δt/Δν	Input transition rise or fall rate $V_{CC} = 1.5 \text{ V to } 5.5 \text{ V}$			150		150		150	ms/V

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		Vcc	T <sub>A</sub> =	T <sub>A</sub> = 25°C		–55°C to 125°C		–40°C to 85°C	
				MIN	MAX	MIN	MAX	MIN	N MAX	
V <sub>T+</sub> Positive-going threshold			5 V	2.6	3.4	2.6	3.4	2.6	3.4	V
VT- Negative-going threshold			5 V	1.6	2.4	1.6	2.4	1.6	2.4	٧
$\Delta V_T$ Hysteresis $(V_{T+} - V_{T-})$			5 V	0.5		0.5		0.5		V
	V <sub>I</sub> = V <sub>T+</sub>		1.5 V	1.4		1.4		1.4		
		$I_{OH} = -50 \mu A$	3 V	2.9		2.9		2.9		٧
			4.5 V	4.4		4.4		4.4		
Voн		$I_{OH} = -4 \text{ mA}$	3 V	2.58		2.4		2.48		
		$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.7		3.8		
	$I_{OH} = -50 \text{ mA}^{\dagger}$ 5.5 V			3.85						
		$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V					3.85		
			1.5 V		0.1		0.1		0.1	
		$I_{OL} = 50 \mu A$	3 V		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1	
VOL	$V_I = V_{T-}$	$I_{OL} = 12 \text{ mA}$	3 V		0.36		0.5		0.44	V
		$I_{OL} = 24 \text{ mA}$	4.5 V		0.36		0.5		0.44	
		$I_{OL} = 50 \text{ mA}^{\dagger}$	5.5 V				1.65			
		$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V						1.65	
lį	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μΑ
ICC	$V_I = V_{CC}$ or GND,	I <sub>O</sub> = 0	5.5 V		4		80		40	μΑ
Ci					10		10		10	pF

Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

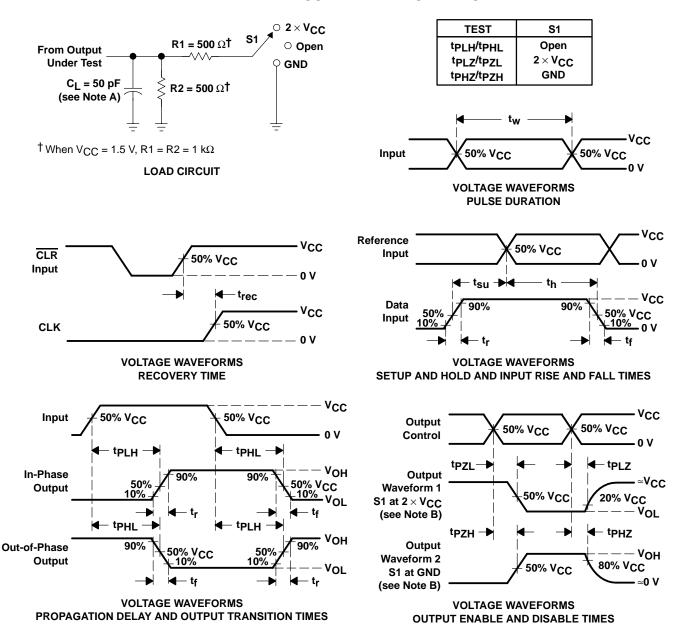
PARAMETER	FROM (INPUT)	TO -55°C TO 125°C (OUTPUT)			–40°C TO 85°C		UNIT
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	
<sup>t</sup> PLH	^	<b>V</b>	2.6	10.5	2.7	9.5	no
t <sub>PHL</sub>	χ.	ī	2.6	10.5	2.7	9.5	ns

## operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	45	pF



#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \ \Omega$ ,  $t_f = 3 \ ns$ ,  $t_f = 3 \ ns$ . Phase relationships between waveforms are arbitrary.
  - D. For clock inputs, f<sub>max</sub> is measured with the input duty cycle at 50%.
  - E. The outputs are measured one at a time with one input transition per measurement.
  - F. tpLH and tpHL are the same as tpd.
  - G. tpzL and tpzH are the same as ten.
  - H. tpLz and tpHz are the same as tdis.

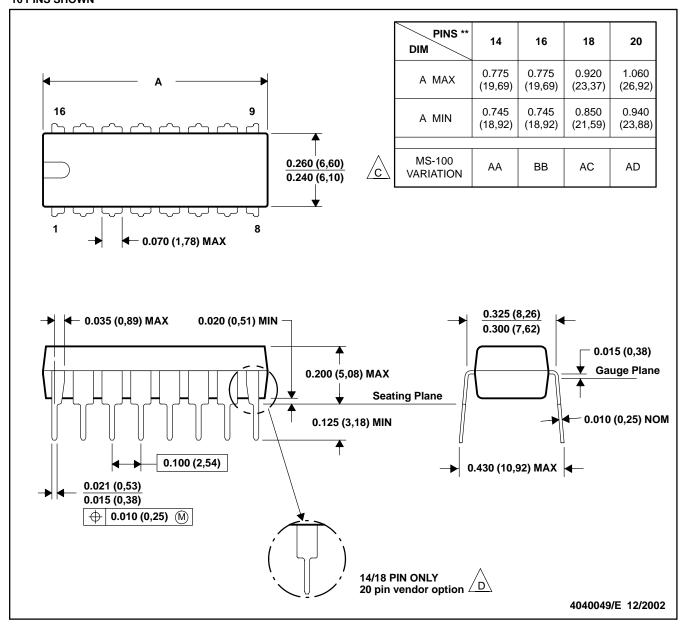
Figure 1. Load Circuit and Voltage Waveforms



#### N (R-PDIP-T\*\*)

### 16 PINS SHOWN

#### PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

Falls within JEDEC MS-001, except 18 and 20 pin minimum body Irngth (Dim A).

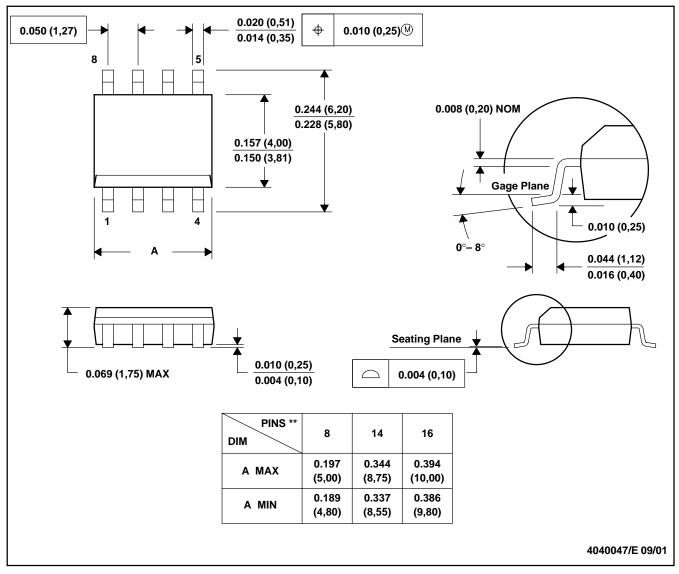
The 20 pin end lead shoulder width is a vendor option, either half or full width.



#### D (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

#### **8 PINS SHOWN**



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012

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