

# 4-Mbit (512K x 8) Static RAM

## Features

- Pin- and function-compatible with CY7C1049B
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 90 \text{ mA @ } 10 \text{ ns}$
- Low CMOS Standby power
  - $I_{SB2} = 10 \text{ mA}$
- 2.0V Data Retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in lead-free 36-Lead (400-Mil) Molded SOJ package

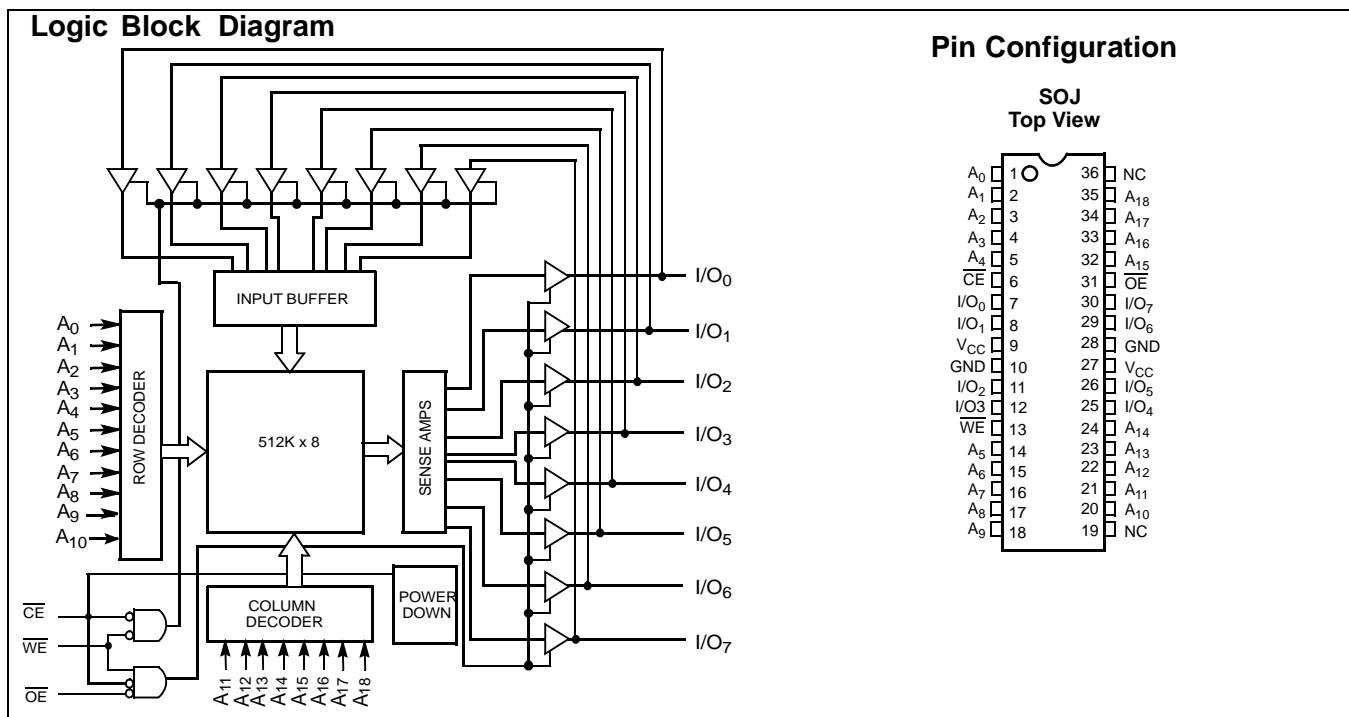
## Functional Description<sup>[1]</sup>

The CY7C1049D is a high-performance CMOS static RAM organized as 512K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1049D is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.



## Selection Guide

	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	90	mA
Maximum CMOS Standby Current	10	mA

### Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[2]</sup> .... -0.5V to +6.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	4.5V-5.5V

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit
			Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>IH</sub> <sup>[2]</sup>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub> <sup>[2]</sup>	Input LOW Voltage <sup>[2]</sup>		-0.5	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND < V <sub>I</sub> < V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND < V <sub>OUT</sub> < V <sub>CC</sub> , Output Disabled	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	100 MHz	90	mA
			83 MHz	80	mA
			66 MHz	70	mA
			40 MHz	60	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , CE > V <sub>IH</sub> , V <sub>IN</sub> > V <sub>IH</sub> or V <sub>IN</sub> < V <sub>IL</sub> , f = f <sub>MAX</sub>		20	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE > V <sub>CC</sub> - 0.3V, V <sub>IN</sub> > V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> < 0.3V, f = 0		10	mA

### Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	8	pF
C <sub>OUT</sub>	I/O Capacitance		8	pF

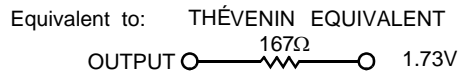
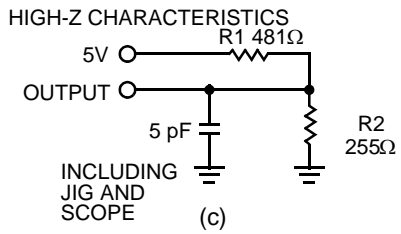
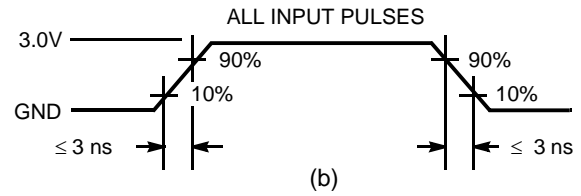
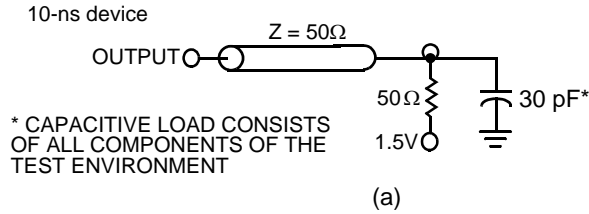
### Thermal Resistance<sup>[3]</sup>

Parameter	Description	Test Conditions	SOJ Package	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient) <sup>[3]</sup>	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.91	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case) <sup>[3]</sup>		36.73	°C/W

**Notes:**

- Minimum voltage is -2.0V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 2V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms<sup>[4]</sup>



Switching Characteristics<sup>[5]</sup> Over the Operating Range

Parameter	Description	-10		Unit
		Min.	Max.	
<b>Read Cycle</b>				
$t_{power}$	$V_{CC}$ (typical) to the First Access <sup>[6]</sup>	100		μs
$t_{RC}$	Read Cycle Time	10		ns
$t_{AA}$	Address to Data Valid		10	ns
$t_{OHA}$	Data Hold from Address Change	3		ns
$t_{ACE}$	CE LOW to Data Valid		10	ns
$t_{DOE}$	OE LOW to Data Valid		5	ns
$t_{LZOE}$	OE LOW to Low Z <sup>[8]</sup>	0		ns
$t_{HZOE}$	OE HIGH to High Z <sup>[7, 8]</sup>		5	ns
$t_{LZCE}$	CE LOW to Low Z <sup>[8]</sup>	3		ns
$t_{HZCE}$	CE HIGH to High Z <sup>[7, 8]</sup>		5	ns
$t_{PU}$	CE LOW to Power-Up	0		ns
$t_{PD}$	CE HIGH to Power-Down		10	ns
<b>Write Cycle<sup>[9, 10]</sup></b>				
$t_{WC}$	Write Cycle Time	10		ns
$t_{SCE}$	CE LOW to Write End	7		ns
$t_{AW}$	Address Set-Up to Write End	7		ns
$t_{HA}$	Address Hold from Write End	0		ns

Notes:

- AC characteristics (except High-Z) for 10-ns parts are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c)
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of CE LOW, and WE LOW. CE and WE must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 (WE controlled, OE LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

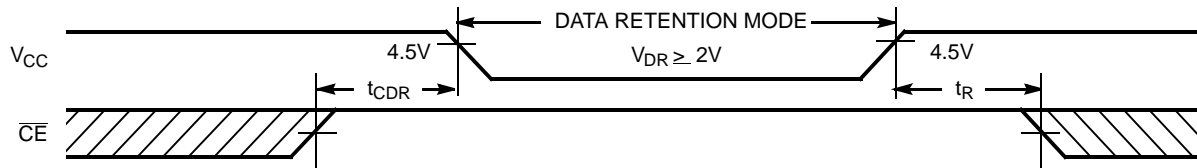
**Switching Characteristics<sup>[5]</sup>** Over the Operating Range (continued)

Parameter	Description	-10		Unit
		Min.	Max.	
t <sub>SA</sub>	Address Set-Up to Write Start	0		ns
t <sub>PWE</sub>	WE Pulse Width	7		ns
t <sub>SD</sub>	Data Set-Up to Write End	6		ns
t <sub>HD</sub>	Data Hold from Write End	0		ns
t <sub>LZWE</sub>	WE HIGH to Low Z <sup>[8]</sup>	3		ns
t <sub>HZWE</sub>	WE LOW to High Z <sup>[7, 8]</sup>		5	ns

**Data Retention Characteristics** Over the Operating Range

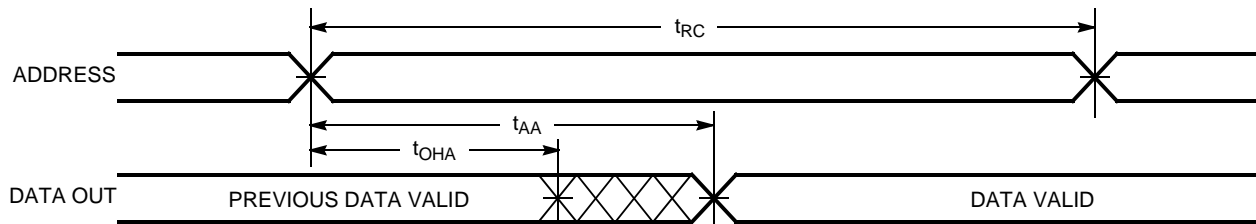
Parameter	Description	Conditions <sup>[12]</sup>	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		2.0		V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = V <sub>DR</sub> = 2.0V, CE ≥ V <sub>CC</sub> - 0.3V		10	mA
t <sub>CDR</sub> <sup>[3]</sup>	Chip Deselect to Data Retention Time	V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V	0		ns
t <sub>R</sub> <sup>[11]</sup>	Operation Recovery Time		t <sub>RC</sub>		ns

**Data Retention Waveform**



**Switching Waveforms**

**Read Cycle No. 1<sup>[13, 14]</sup>**

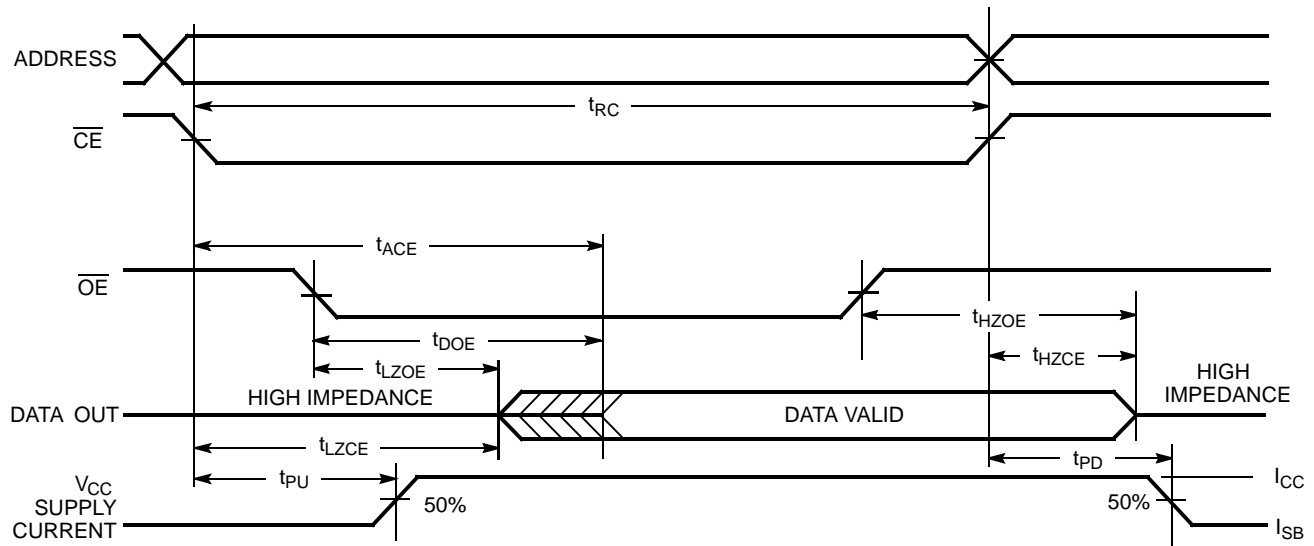


**Notes:**

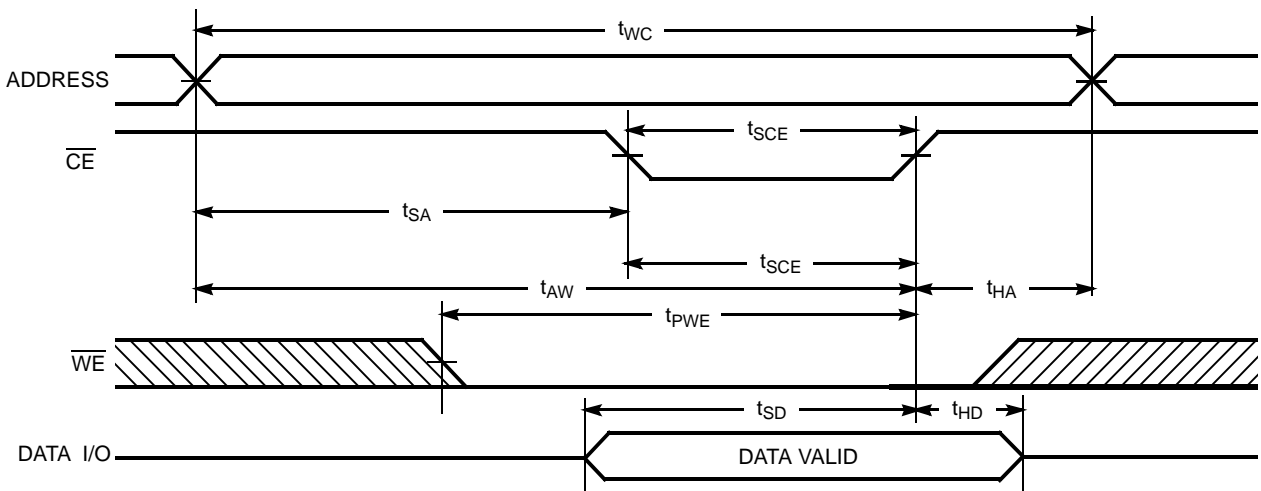
- 11. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 50 μs or stable at V<sub>CC(min.)</sub> ≥ 50 μs
- 12. No input may exceed V<sub>CC</sub> + 0.5V<sub>CC</sub>.
- 13. Device is continuously selected. OE, CE = V<sub>IL</sub>.
- 14. WE is HIGH for read cycle.

Switching Waveforms(continued)

Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[14, 15]</sup>



Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[16, 17]</sup>

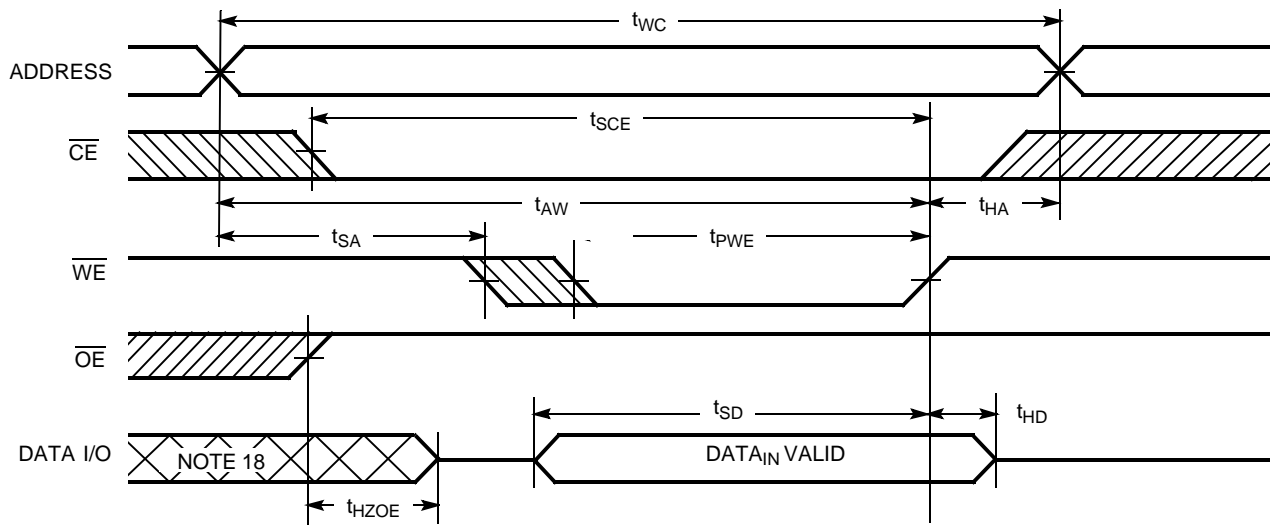


Notes:

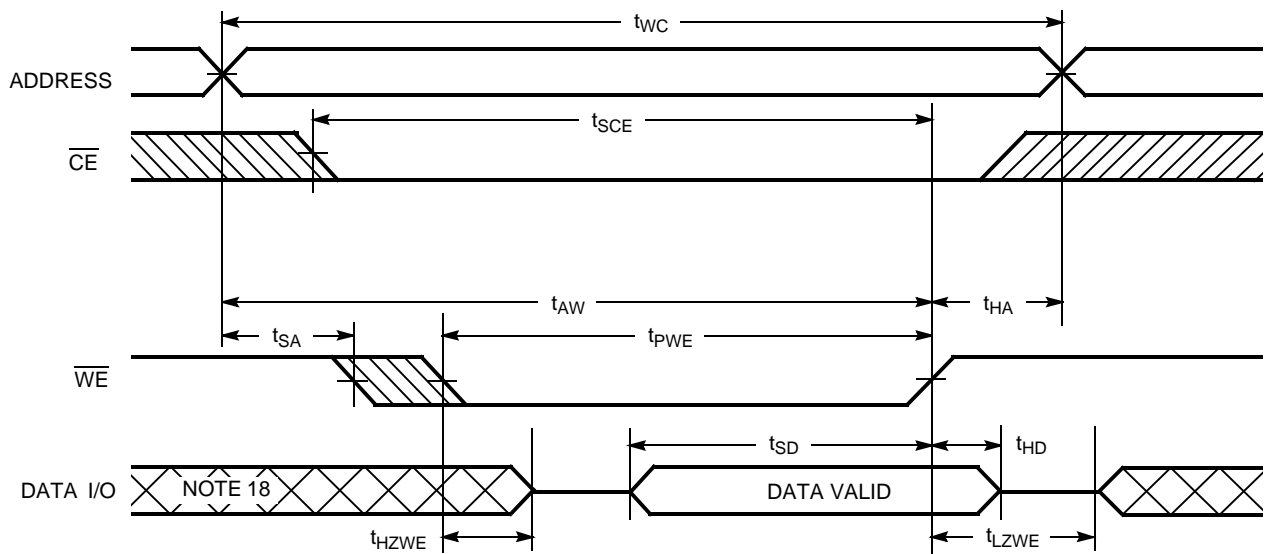
- 15. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- 16. Data I/O is high impedance if  $OE = V_{IH}$ .
- 17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

Switching Waveforms(continued)

Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[16, 17]</sup>



Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[17]</sup>



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	High-Z	Power-down	Standby (I <sub>SB</sub> )
L	L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	X	L	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	High-Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

Notes:

18. During this period the I/Os are in the output state and input signals should not be applied.

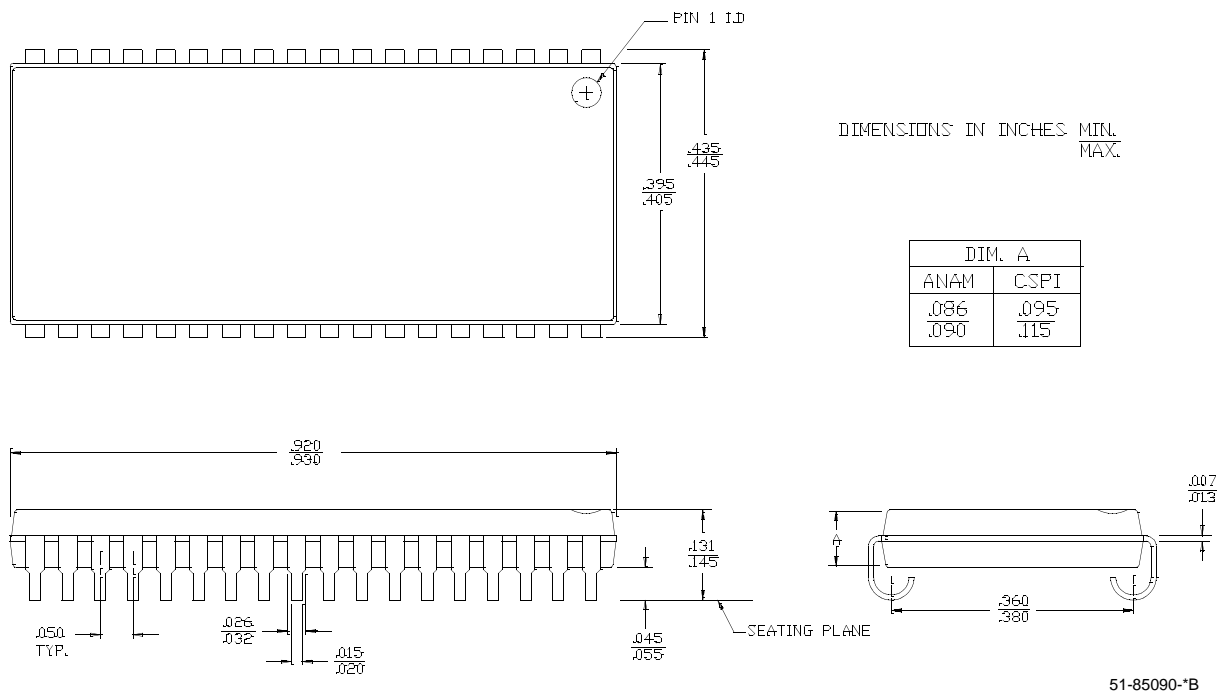
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1049D-10VXI	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-Free)	Industrial

Please contact your local Cypress sales representative for availability of these parts.

**Package Diagram**

**36-Lead (400-Mil) Molded SOJ (51-85090)**



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Document History Page

Document Title: CY7C1049D 4-Mbit (512K x 8) Static RAM				
Document Number: 38-05474				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Datasheet for C9 IPP
*A	233729	See ECN	RKF	1.AC, DC parameters are modified as per EROS(Spec # 01-2165) 2.Pb-free offering in the 'ordering information'
*B	351096	See ECN	PCI	Changed from Advance to Preliminary Removed 17, 20 ns Speed bin Added footnote # 4 Redefined I <sub>CC</sub> values for Com'l and Ind'l temperature ranges I <sub>CC</sub> (Com'l): Changed from 67 and 54 mA to 75 and 70 mA for 12 and 15 ns speed bins respectively I <sub>CC</sub> (Ind'l): Changed from 80, 67 and 54 mA to 90, 85 and 80 mA for 10, 12 and 15 ns speed bins respectively Added V <sub>IH(max)</sub> spec in Note# 2 Modified Note# 10 on t <sub>R</sub> Changed t <sub>SCE</sub> from 8 to 7 ns for 10 ns speed bin Changed reference voltage level for measurement of Hi-Z parameters from ±500 mV to ±200 mV Added Truth Table on page# 6 Removed L-Version Added 10 ns parts in the Ordering Information Table Added Lead-Free Product Information Shaded Ordering Information Table
*C	446328	See ECN	NXR	Converted from Preliminary to Final Removed -12 and -15 speed bins Removed Commercial Operating Range product information Changed Maximum Rating for supply voltage from 7V to 6V Updated Thermal Resistance table Changed t <sub>HZWE</sub> from 6 ns to 5 ns Updated footnote #7 on High-Z parameter measurement Replaced Package Name column with Package Diagram in the Ordering Information table