

# 1M x 16 Static RAM

## Features

- **High speed**  
—  $t_{AA} = 8, 10, 12 \text{ ns}$
- **Low active power**  
— 1080 mW (max.)
- **Operating voltages of  $3.3 \pm 0.3V$**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{CE}_1$  and  $\overline{CE}_2$  features**

## Functional Description

The CY7C1061AV33 is a high-performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

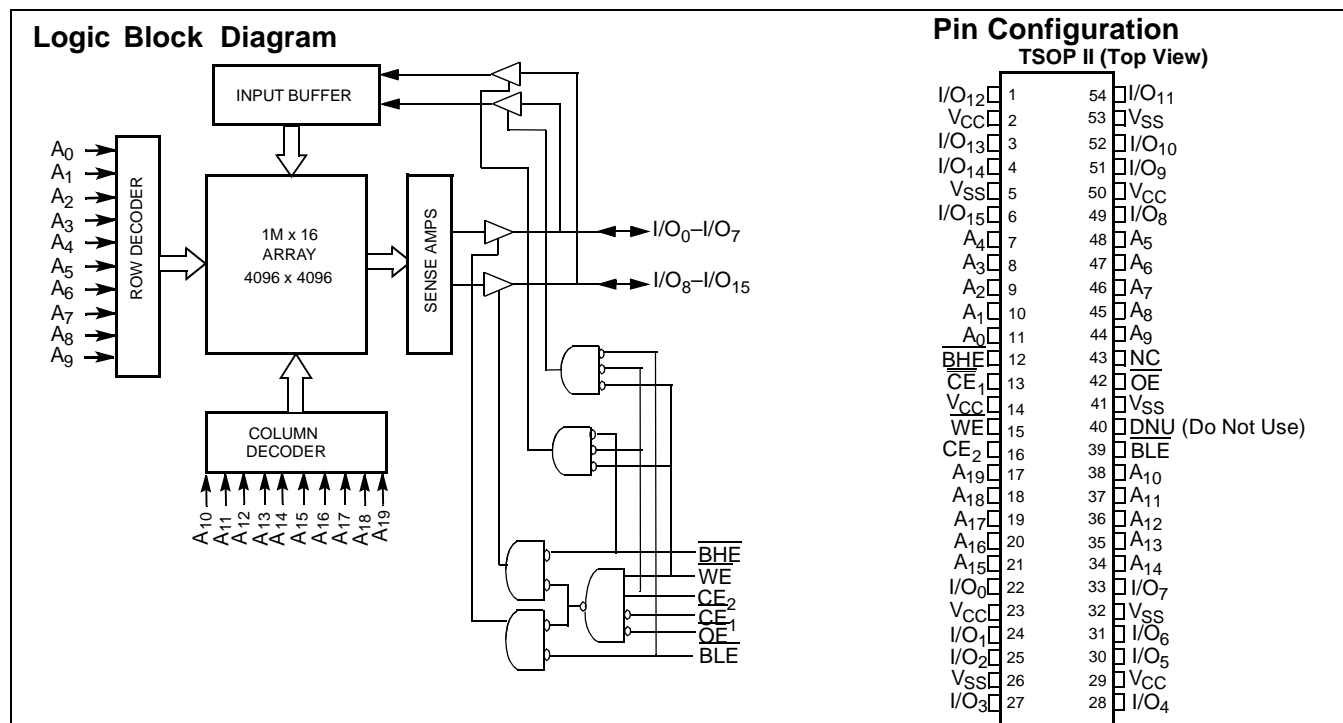
Writing to the device is accomplished by enabling the chip ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) while forcing the Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location

specified on the address pins (A<sub>0</sub> through A<sub>19</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>).

Reading from the device is accomplished by enabling the chip by taking  $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH while forcing the Output Enable (OE) LOW and the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

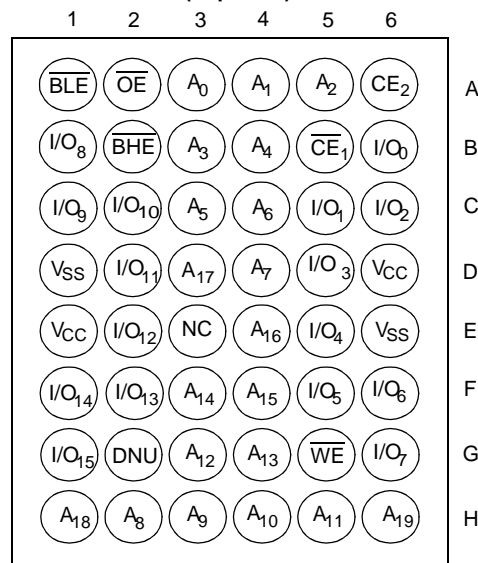
The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH/ $\overline{CE}_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a Write operation ( $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH, and WE LOW).

The CY7C1061AV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and a 48-ball fine-pitch ball grid array (FBGA) package.



## Selection Guide

		-8	-10	-12	Unit
Maximum Access Time		8	10	12	ns
Maximum Operating Current	Commercial	300	275	260	mA
	Industrial	300	275	260	
Maximum CMOS Standby Current	Commercial/Industrial	50	50	50	mA

**Pin Configurations**
**48-ball FBGA**
**(Top View)**


**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> .... -0.5V to +4.6V

DC Voltage Applied to Outputs  
in High-Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

**Operating Range**

Range	Ambient Temperature	$V_{CC}$
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

**DC Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	-8		-10		-12		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = −4.0 mA	2.4		2.4		2.4		V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	V	
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		−0.3	0.8	−0.3	0.8	−0.3	0.8	V	
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	−1	+1	−1	+1	−1	+1	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	−1	+1	−1	+1	−1	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Commercial		300		275		260	mA
			Industrial		300		275		260	mA
I <sub>SB1</sub>	Automatic CE Power-down Current —TTL Inputs	CE <sub>2</sub> ≤ V <sub>IL</sub> Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		70		70		70	mA	
I <sub>SB2</sub>	Automatic CE Power-down Current —CMOS Inputs	CE <sub>2</sub> ≤ 0.3V Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> − 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	Commercial/ Industrial		50		50		50	mA

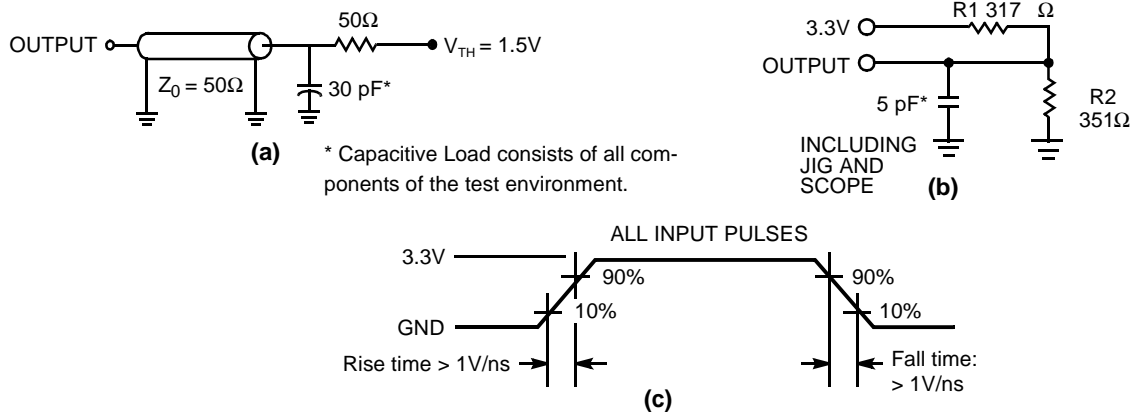
**Capacitance<sup>[2]</sup>**

Parameter	Package	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Z54	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	6	pF
	BA48			8	pF
C <sub>OUT</sub>	Z54	I/O Capacitance		8	pF
	BA48			10	pF

**Notes:**

- $V_{IL} (\text{min.}) = -2.0V$  for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms<sup>[3]</sup>



### AC Switching Characteristics Over the Operating Range<sup>[4]</sup>

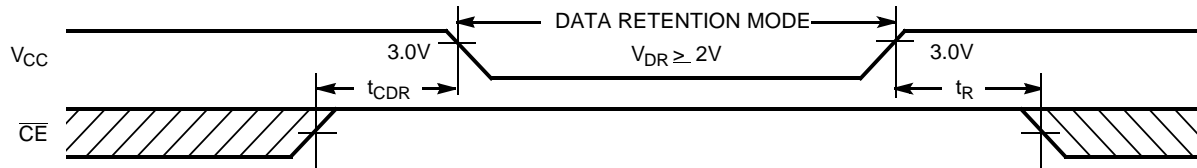
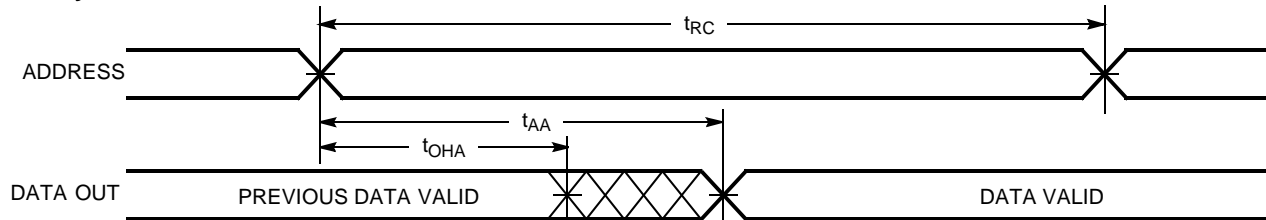
Parameter	Description	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t <sub>power</sub>	V <sub>CC</sub> (typical) to the first access <sup>[5]</sup>	1		1		1		ms
t <sub>RC</sub>	Read Cycle Time	8		10		12		ns
t <sub>AA</sub>	Address to Data Valid		8		10		12	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW / CE <sub>2</sub> HIGH to Data Valid		8		10		12	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		5		5		6	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z	1		1		1		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[6]</sup>		5		5		6	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW/CE <sub>2</sub> HIGH to Low-Z <sup>[6]</sup>	3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH/CE <sub>2</sub> LOW to High-Z <sup>[6]</sup>		5		5		6	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW/CE <sub>2</sub> HIGH to Power-Up <sup>[7]</sup>	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH/CE <sub>2</sub> LOW to Power-Down <sup>[7]</sup>		8		10		12	ns
t <sub>DBE</sub>	Byte Enable to Data Valid		5		5		6	ns
t <sub>LZBE</sub>	Byte Enable to Low-Z	1		1		1		ns
t <sub>HZBE</sub>	Byte Disable to High-Z		5		5		6	ns
Write Cycle <sup>[8, 9]</sup>								
t <sub>WC</sub>	Write Cycle Time	8		10		12		ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW/CE <sub>2</sub> HIGH to Write End	6		7		8		ns

#### Notes:

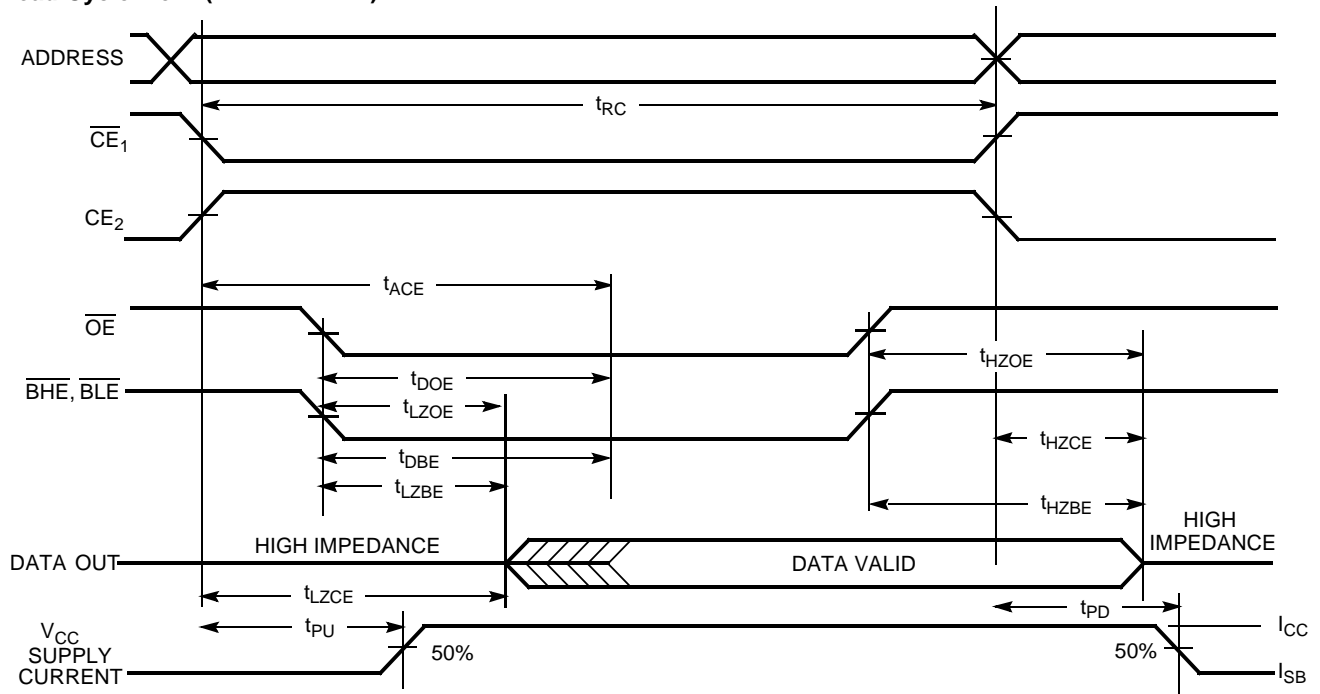
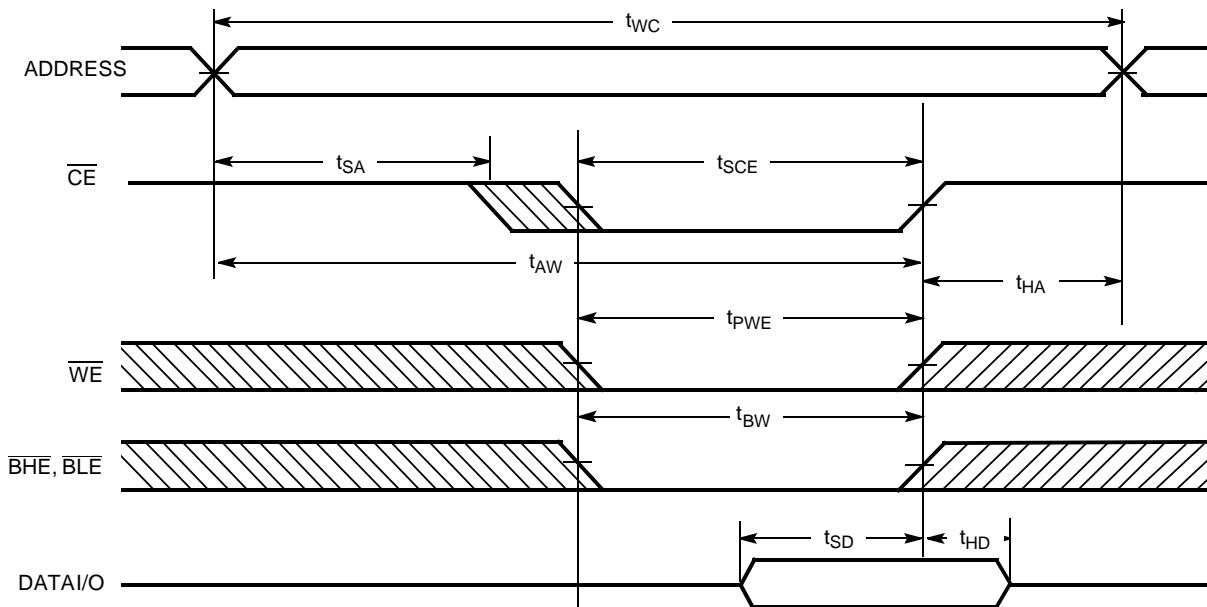
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0V). As soon as 1ms ( $T_{power}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation can begin including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0V) voltage.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and specified transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
- This part has a voltage regulator which steps down the voltage from 3V to 2V internally.  $t_{power}$  time has to be provided initially before a Read/Write operation is started.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$  and  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ ,  $t_{LZBE}$  are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW ( $CE_2$  HIGH) and  $\overline{WE}$  LOW. Chip enables must be active and  $\overline{WE}$  and byte enables must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**AC Switching Characteristics** Over the Operating Range (continued)<sup>[4]</sup>

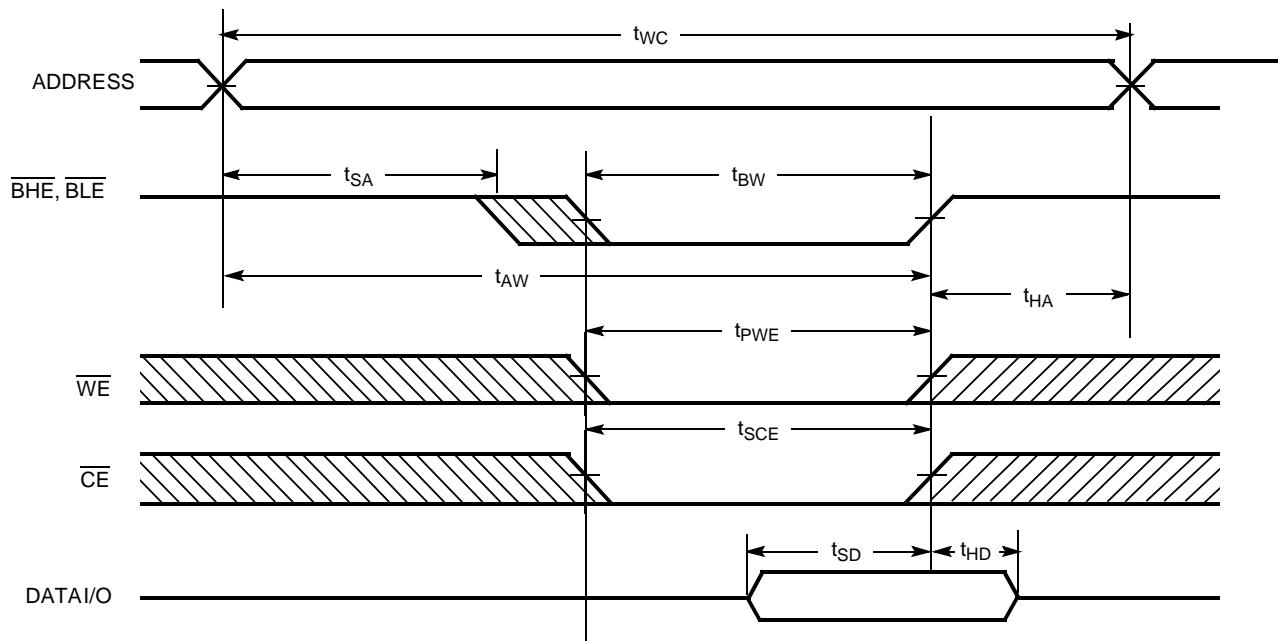
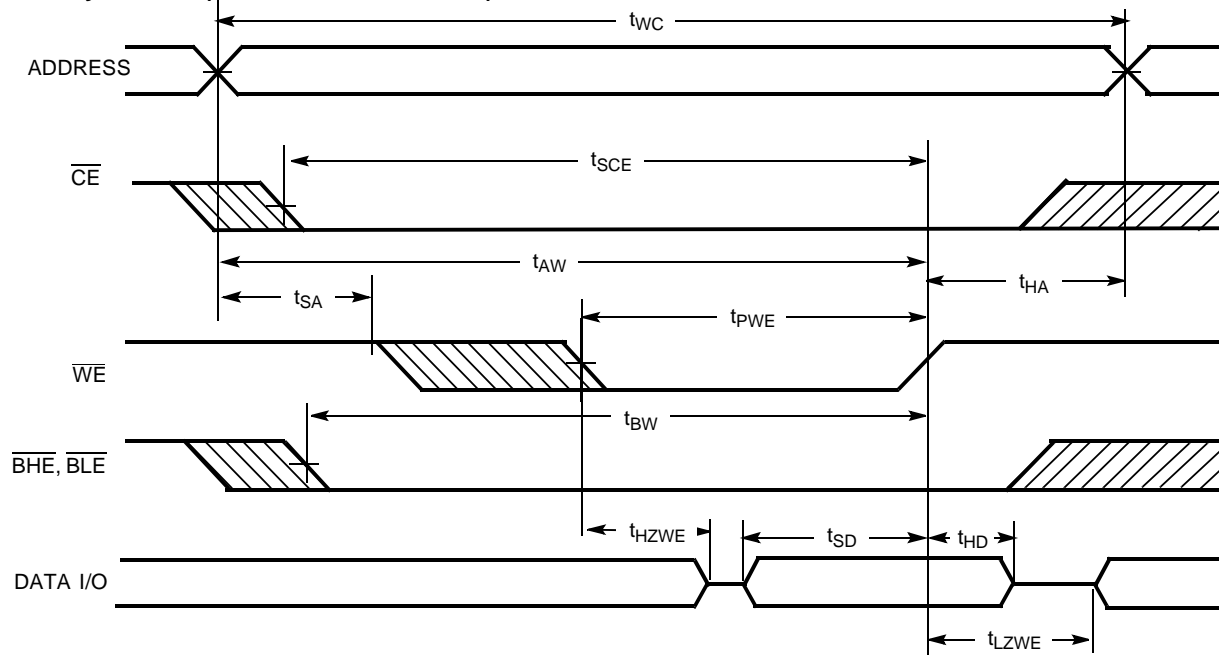
Parameter	Description	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{AW}$	Address Set-up to Write End	6		7		8		ns
$t_{HA}$	Address Hold from Write End	0		0		0		ns
$t_{SA}$	Address Set-up to Write Start	0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	6		7		8		ns
$t_{SD}$	Data Set-up to Write End	5		5.5		6		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[6]</sup>	3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[6]</sup>		5		5		6	ns
$t_{BW}$	Byte Enable to End of Write	6		7		8		ns

**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No. 1<sup>[10, 11]</sup>**

**Notes:**

10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BHE} = V_{IL}$ .  $CE2 = V_{IH}$ .  
 11.  $\overline{WE}$  is HIGH for Read cycle.

**Switching Waveforms (continued)**
**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[11, 12]</sup>**

**Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[13, 14, 15]</sup>**

**Notes:**

12. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
13. Data I/O is high-impedance if  $\overline{OE}$  or BHE and/or BLE =  $V_{IH}$ .
14. If  $\overline{CE}_1$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
15.  $\overline{CE}$  is a shorthand combination of both  $\overline{CE}_1$  and  $CE_2$  combined. It is active LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) <sup>[13, 14, 15]</sup>**


**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	X	High-Z	High-Z	Power-down	Standby (I <sub>SB</sub> )
X	L	X	X	X	X	High-Z	High-Z	Power-down	Standby (I <sub>SB</sub> )
L	H	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I <sub>CC</sub> )
L	H	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I <sub>CC</sub> )
L	H	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I <sub>CC</sub> )
L	H	X	L	L	L	Data In	Data In	Write All Bits	Active (I <sub>CC</sub> )
L	H	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I <sub>CC</sub> )
L	H	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I <sub>CC</sub> )
L	H	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code <sup>[16]</sup>	Package Name	Package Type	Operating Range
8	CY7C1061AV33-8ZC	Z54-II	54-pin TSOP II	Commercial
	CY7C1061AV33-8ZI			Industrial
	CY7C1061AV33-8BAC	BA48G	48-ball Mini BGA	Commercial
	CY7C1061AV33-8BAI			Industrial
10	CY7C1061AV33-10ZC	Z54-II	54-pin TSOP II	Commercial
	CY7C1061AV33-10ZI			Industrial
	CY7C1061AV33-10BAC	BA48G	48-ball Mini BGA	Commercial
	CY7C1061AV33-10BAI			Industrial
12	CY7C1061AV33-12ZC	Z54-II	54-pin TSOP II	Commercial
	CY7C1061AV33-12ZI			Industrial
	CY7C1061AV33-12BAC	BA48G	48-ball Mini BGA	Commercial
	CY7C1061AV33-12BAI			Industrial

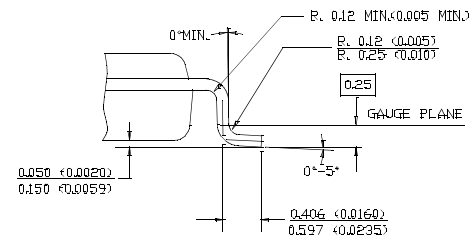
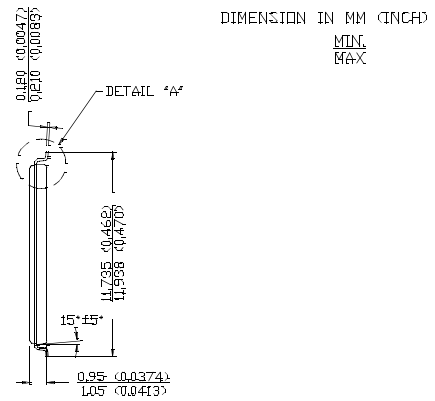
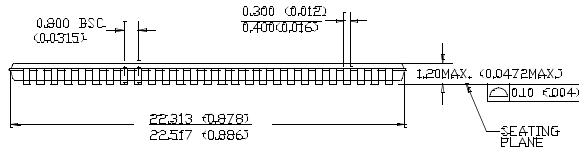
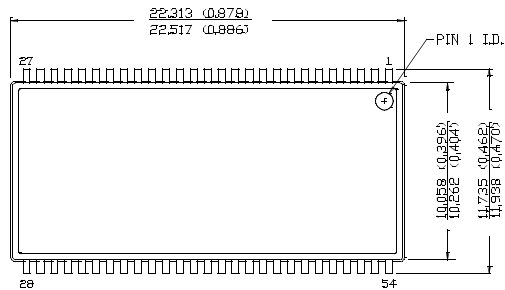
**Note:**

16. Contact a Cypress representative for availability of the 48-ball Mini BGA (BA48) package.



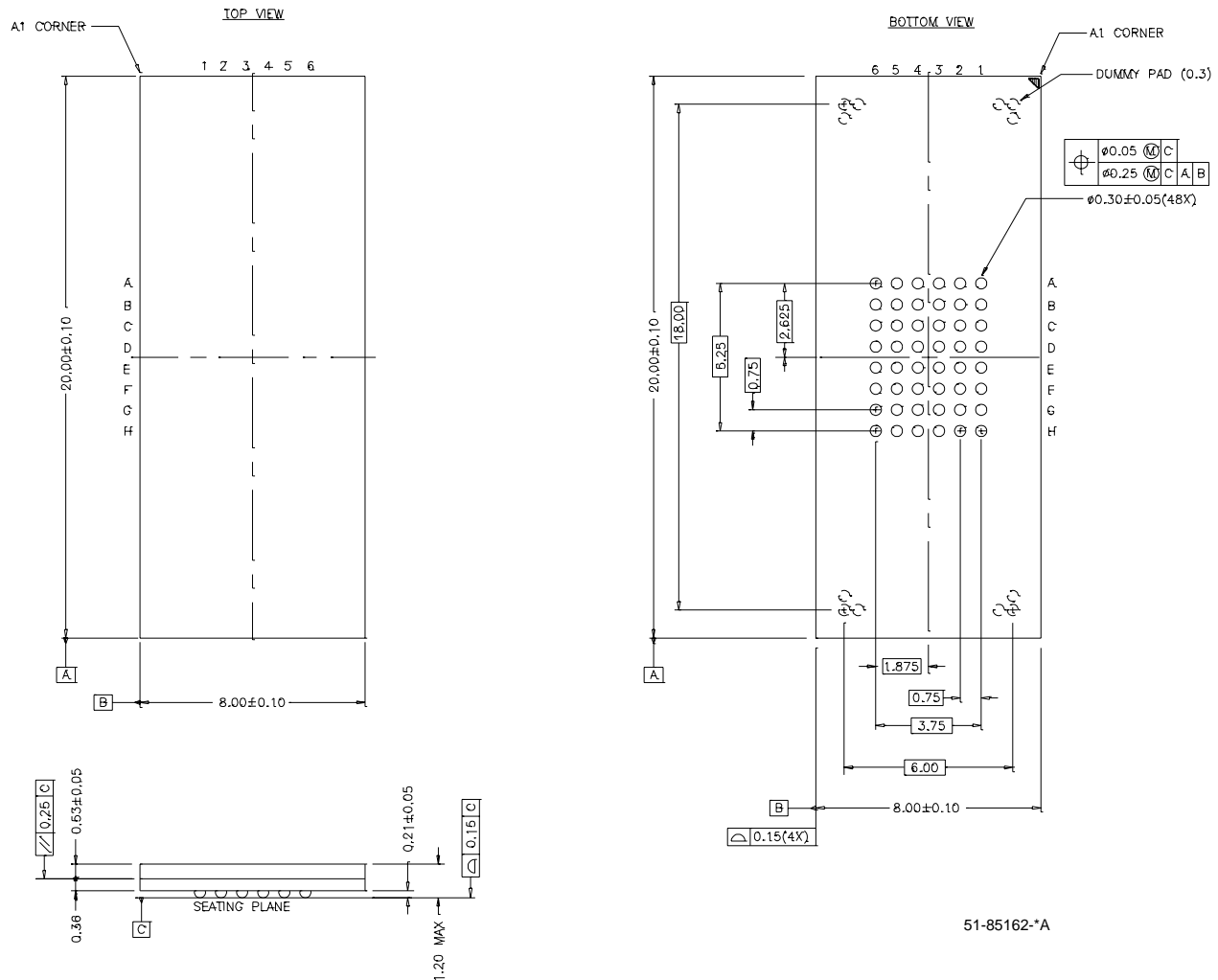
Package Diagrams

54-lead Thin Small Outline Package, Type II Z54-II



DETAIL "A"

51-85160-\*\*

**Package Diagrams (continued)**
**48-ball (8 mm x 20 mm x 1.2 mm) FBGA BA48G**


51-85162-\*A

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**Document History Page**

Document Title: CY7C1061AV33 1M x 16 Static RAM Document Number: 38-05256				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	113725	03/28/02	NSL	New Data Sheet
*A	117058	07/31/02	DFP	Removed 15-ns bin.
*B	117989	08/30/02	DFP	Added 8-ns bin. Changed Icc for 8, 10, 12 bins. $t_{power}$ changed from 1 $\mu$ s to 1 ms. Load Cap Comment changed (for Tx line load). $t_{SD}$ changed to 5.5 ns for the 10-ns bin. Changed some 8-ns bin numbers ( $t_{HZ}$ , $t_{DOE}$ , $t_{DBE}$ ). Removed hz<Iz comments from data sheet.
*C	120383	11/06/02	DFP	Final data sheet. Added note 3 to "AC Test Loads and Waveforms" and note 7 to $t_{pu}$ and $t_{pd}$ . Updated Input/Output Caps (for 48BGA only) to 8 pF/10 pF and for the 54-pin TSOP to 6/8 pF.
*D	124439	2/25/03	MEG	Changed ISB1 from 100 mA to 70 mA. Shaded fBGA production ordering information.