16-BIT, HIGH-SPEED, LOW-NOISE, VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **16-Bit Monotonic**
- **±5-V Rail-to-Rail Output**
- **Very Low Glitch: 0.5 nV-s**
- **Fast Settling: 0.65 µs**
- **Fast Slew Rate: 35 V/µs**
- **Low Noise: 20 nV/$\sqrt{\text{Hz}}$**
- **±25-mA Load Drive**
- **±5-V Dual Power Supply**
- **Single External Reference**
- **Power-On Reset to Midscale**
- **3-MSPS Update Rate**
- **SPI Interface, Up to 50 MHz**
- **1.8 V–5 V Logic Compatible**
- **2s Complement Data Format**
- **Hardware Reset to Midscale**
- **TSSOP-16 Package**

APPLICATIONS

- **Industrial Process Control**
- **CRT Projection TV Digital Convergence**
- **Waveform Generation**
- **Automated Test Equipment**
- **Ultrasound**

DESCRIPTION

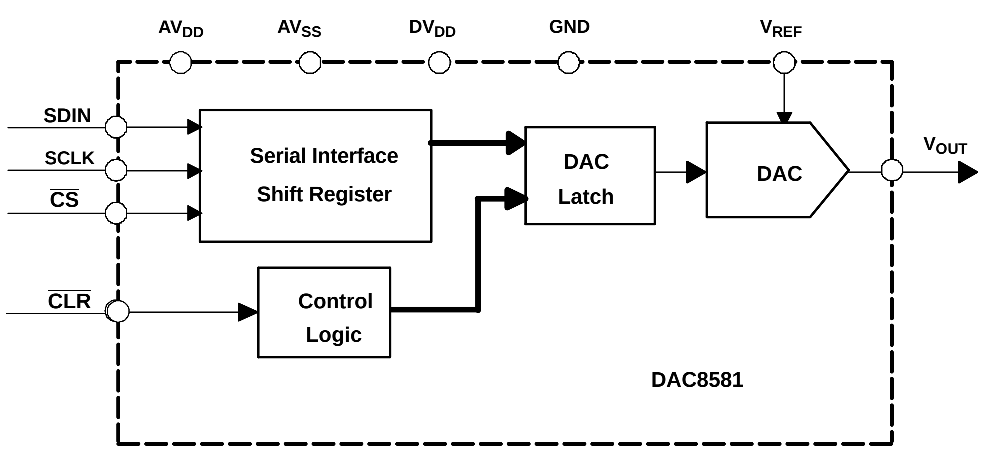
DAC8581 is a 16-bit, high-speed, low-noise DAC operating from dual ±5-V power supplies. DAC8581 is monotonic, has exceptionally low noise and exceptionally low glitch. The DAC8581's high-performance, rail-to-rail output buffer is capable of settling within 0.65µs for a 10-V step. Small-signal settling time is well under 0.3 µs, supporting data update rates up to 3 MSPS. A power-on-reset circuit sets the output at midscale voltage on power up.

The DAC8581 is simple to use, with a single external reference and a standard 3-wire SPI interface that allows clock rates up to 50 MHz.

Also see the DAC8580, a member of the same family. The DAC8580 combines DAC8581 performance with an on-chip, 16X over-sampling digital filter.

The DAC8581 is specified over –40°C-to-85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM OF DAC8581



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. This device is rated at 1500 V HBM and 1000 V CDM.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	PACKAGE ORDERING MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DAC8581	16-TSSOP	PW	–40°C to 85°C	D8581I	DAC8581IPW	90-Piece Tube
					DAC8581IPWR	2000-Piece Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		UNIT
AV_{DD} or DV_{DD} to AV_{SS}		–0.3 V to 12 V
Digital iput voltage to AV_{SS}		–0.3 V to 12 V
V_{OUT} or V_{REF} to AV_{SS}		–0.3 V to 12 V
DGND and AGND to AV_{SS}		–0.3 V to 6 V
Operating temperature range		–40°C to 85°C
Storage temperature range		–65°C to 150°C
Junction temperature range (T_J max)		150°C
Power dissipation	Thermal impedance (θ_{JA})	118°C/W
	Thermal impedance (θ_{JC})	29°C/W
Lead temperature, soldering	Vapor phase (60s)	215°C
	Infrared (15s)	220°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX}, $+AV_{DD}$ = +5 V, $-AV_{DD}$ = –5 V, DV_{DD} = +5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE					
Resolution		16			Bits
Linearity error	V_{REF} = 4.096 V		±0.03	±0.1	%FS
Differential linearity error			±0.25	±0.5	LSB
Gain error		1	2	3	%FS
Gain drift			±5		ppm/°C
Bipolar zero error			–5	±25	mV
Bipolar zero drift			±20		µV/°C
Total drift			±10		ppm/°C
OUTPUT CHARACTERISTICS					
Voltage output(1)	V_{REF} up to 6 V, when AV_{DD} = 6 V, AV_{SS} = –6 V	$-V_{REF}$		V_{REF}	V
Output impedance			1		Ω
Maximum output current			±25		mA
Settling time	C_L <200 pF, R_L = 2 kΩ, to 0.1% FS, 8-V step		0.65		µs
	To 0.003% FS		1		
Slew rate(2)			35		V/µs
Code change glitch	1 LSB change around major carry		0.5		nV-S
Overshoot	Full-scale change		50		mV
Digital feedthrough(3)			0.5		nV-S
SNR	Digital sine wave input, Fout = 1 kHz, BW = 10 kHz, 2 MSPS update rate		108		dB
THD	Digital sine wave input, Fout = 20 kHz, 8-Vpp output, 2-MSPS update rate		–72		dB
Output voltage noise	0.1 Hz to 10 Hz		25		µVpp
	At 10-kHz offset frequency		25		nV/rtHz
	At 100-kHz offset frequency		20		nV/rtHz
Power supply rejection	VDD varies ±10%		0.75		mV/V
REFERENCE					
Reference input bandwidth	Large signal: 2-Vpp sine wave on 4 V DC		3		MHz
	Small signal: 100-mVpp sine wave on 4 V DC		10		MHz
Reference input voltage range		3		AV_{DD}	V
Reference input impedance			5		kΩ
Reference input capacitance			5		pF
DIGITAL INPUTS					
V_{IH}				0.7 x DV_{DD}	V
V_{IL}		GND		0.3 x DV_{DD}	
Input current				±1	µA
Input capacitance				10	pF
Power-on delay	From V_{DD} high to $\overline{CS}$ low		20		µs

(1) Output can reach $\pm V_{DD}$ unloaded, can reach $\pm(V_{DD} - 0.2$ V) for 600-Ω loading.
(2) Slew rate is measure from 10% to 90% of transition when the output changes from 0 to full scale.
(3) Digital feedthrough is defined as the impulse injected into the analog output from the digital input. It is measured when the DAC output does not change, $\overline{CS}$ is held high, and while SCLK and SDIN signals are toggled.

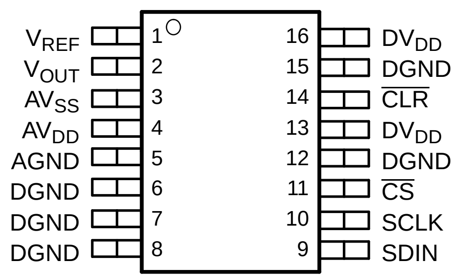
ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, $+AV_{DD} = +5$ V, $–AV_{DD} = –5$ V, $DV_{DD} = +5$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY					
$+AV_{DD}$		4.0	5	6.0	V
$–AV_{DD}$		–4.0	–5	–6.0	V
DV_{DD}		1.8		AV_{DD}	V
I_{DVDD}			10	20	µA
I_{DD}	Iref and IDV_{DD} included		17	24	mA
I_{SS}			–23	–32	mA
TEMPERATURE RANGE					
Specified performance		–40		85	°C

PIN CONFIGURATION (TOP VIEW)

(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		
NAME	**NO.**	
V_{REF}	1	Reference input voltage.
VOUT	2	DAC output voltage. Output swing is $\pm V_{REF}$
AV_{SS}	3	Negative analog supply voltage, tie to –5 V
AV_{DD}	4	Positive analog supply voltage, tie to +5 V
AGND	5	The ground reference point of all analog circuitry of the device. Tie to 0 V.
DGND	6, 7, 8, 15	Tie to DGND to ensure correct operation.
SDIN	9	Digital input, serial data. Ignored when $\overline{CS}$ is high.
SCLK	10	Digital input, serial bit clock. Ignored when $\overline{CS}$ is high.
$\overline{CS}$	11	Digital input. Chip Select ($\overline{CS}$) signal. Active low. When $\overline{CS}$ is high, SCLK and SDI are ignored. When $\overline{CS}$ is low, data can be transferred into the device.
DGND	12	Ground reference for digital circuitry. Tie to 0 V.
DV_{DD}	13	Positive digital supply, 1.8 V–5.5 V compatible
$\overline{CLR}$	14	Digital input for forcing the output to midscale. Active low. When pin $\overline{CLR}$ is low during 16^{th} SCLK following the falling edge of $\overline{CS}$, the falling edge of 16^{th} SCLK sets DAC Latch to midcode, and the DAC output to 0 V. When pin $\overline{CLR}$ is High, the falling edge of 16th SCLK updates DAC latch with the value of input shift register, and changes DAC output to corresponding level.
DV_{DD}	16	Tie to DV_{DD} to ensure correct operation.

TIMING REQUIREMENTS(1)

PARAMETER		MIN	MAX	UNIT
t_{sck}	SCLK period	20		ns
t_{wsck}	SCLK high or low time	10		ns
t_{Lead}	Delay from falling $\overline{CS}$ to first rising SCLK	20		ns
t_{td}	$\overline{CS}$ High between two active Periods	20		ns
t_{su}	Data setup time (Input)	5		ns
t_hi	Data hold time (input)	5		ns
t_r	Rise time		30	ns
t_f	Fall time		30	ns
t_{wait}	Delay from 16th falling edge of SCLK to $\overline{CS}$ low	100		ns
t_{UPDAC}	Delay from 16th falling edge of SCLK to DAC output	1		µs
	V_{DD} High to $\overline{CS}$ Low (power-up delay)	100		µs

(1) Assured by design. Not production tested.

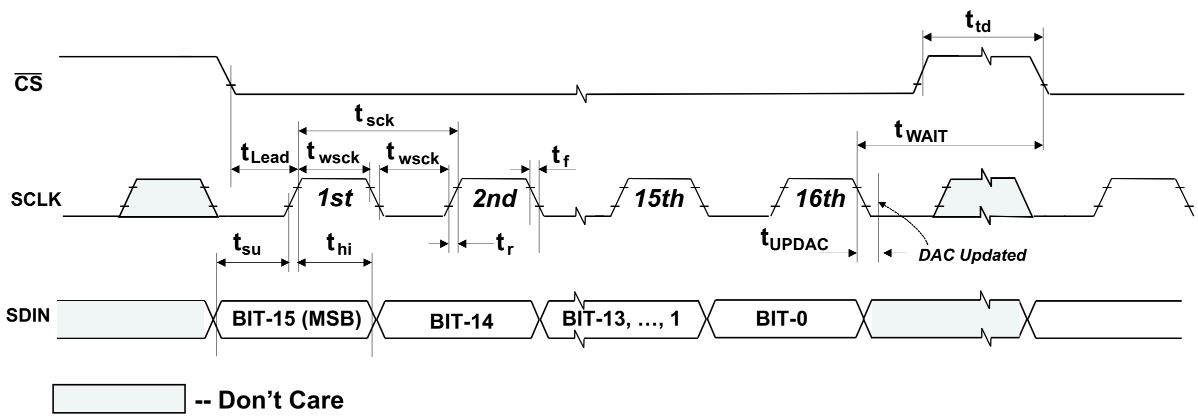


Figure 1. DAC8581 Timing Diagram

TYPICAL CHARACTERISTICS

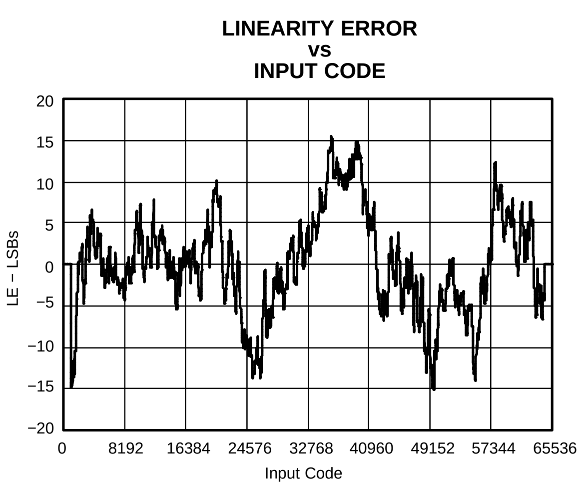


Figure 2.

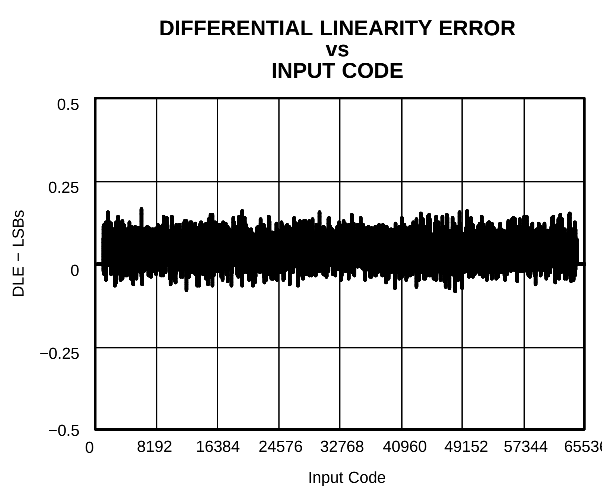


Figure 3.

TYPICAL CHARACTERISTICS (continued)

INTEGRAL NONLINEARITY ERROR vs VREF

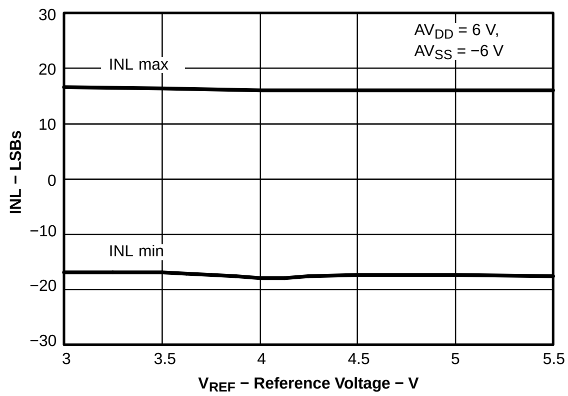


Figure 4.

INTEGRAL NONLINEARITY ERROR vs SUPPLY VOLTAGE

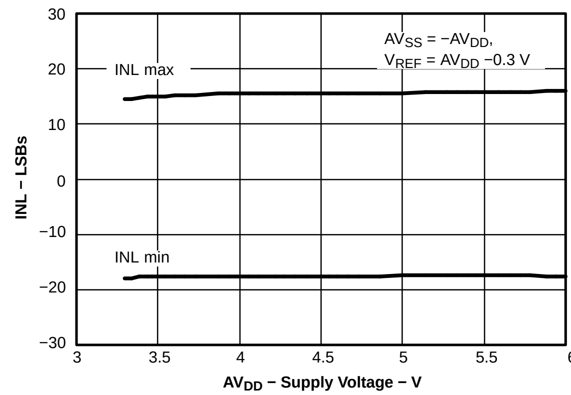


Figure 5.

OFFSET ERROR vs TEMPERATURE

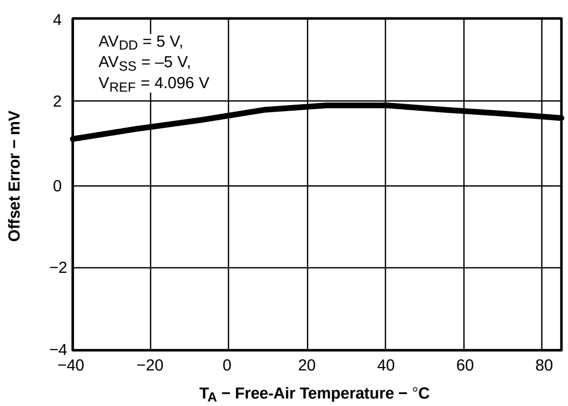


Figure 6.

GAIN ERROR vs TEMPERATURE

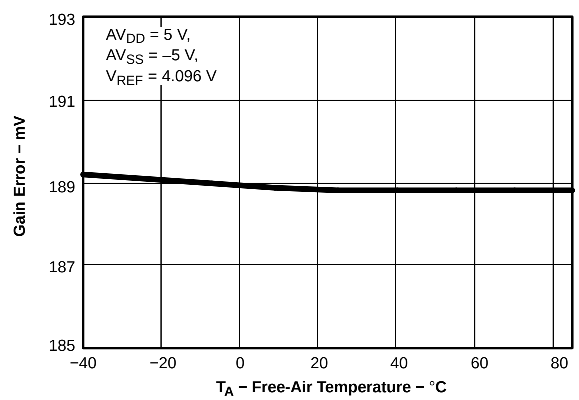


Figure 7.

POSITIVE SUPPLY CURRENT - I_{DD} vs TEMPERATURE

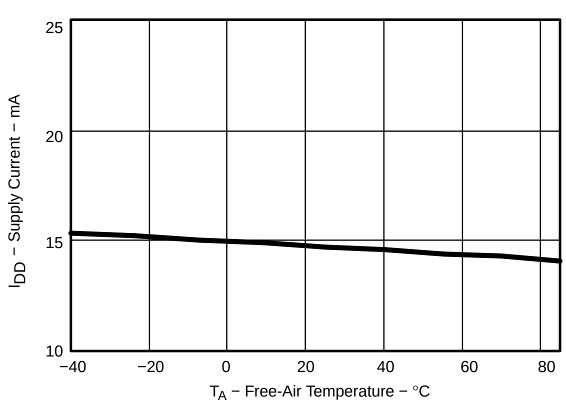


Figure 8.

NEGATIVE SUPPLY CURRENT - I_{SS} vs TEMPERATURE

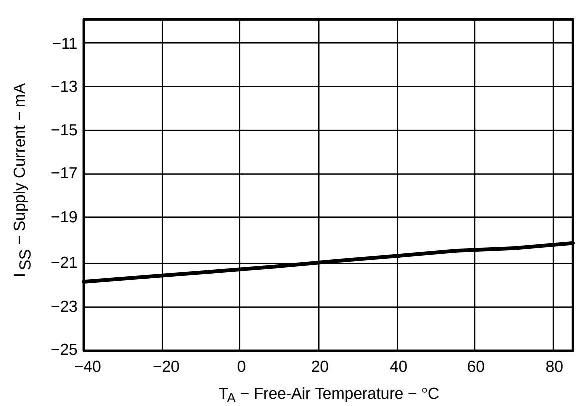


Figure 9.

TYPICAL CHARACTERISTICS (continued)

POSITIVE SUPPLY CURRENT - I_{DD} vs CODE

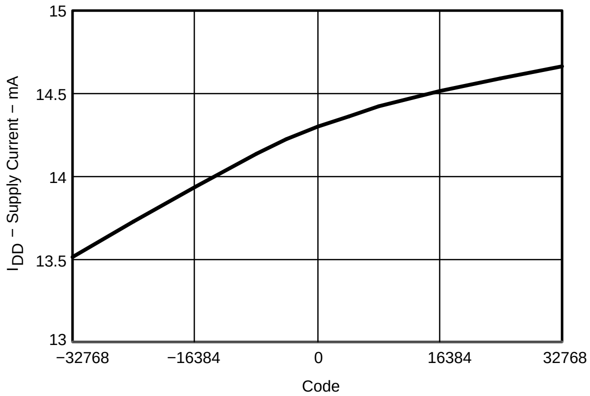


Figure 10.

NEGATIVE SUPPLY CURRENT - I_{SS} vs CODE

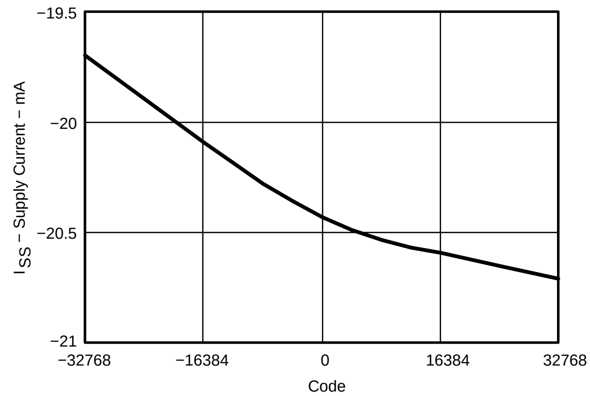


Figure 11.

LARGE-SIGNAL SETTLING

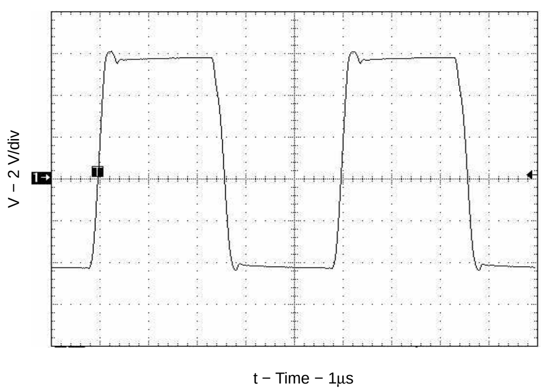


Figure 12.

SMALL-SIGNAL SETTLING

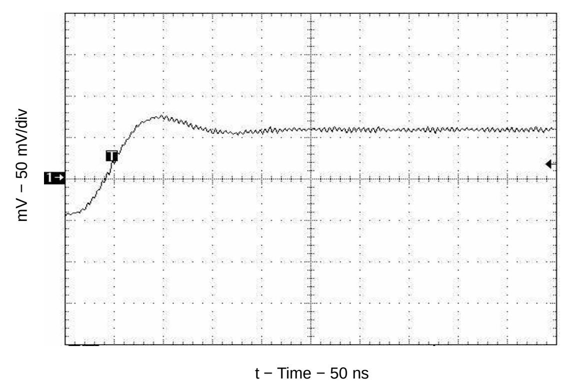


Figure 13.

DIGITAL FEEDTHROUGH AND MIDCODE GLITCH

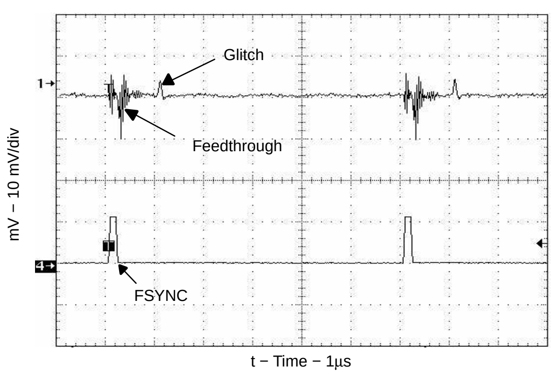


Figure 14.

OUTPUT VOLTAGE NOISE

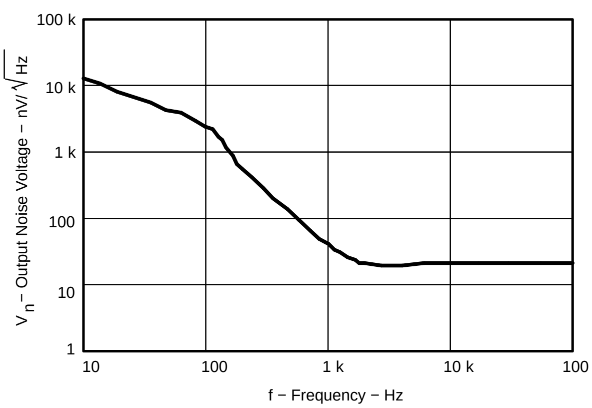


Figure 15.

TYPICAL CHARACTERISTICS (continued)

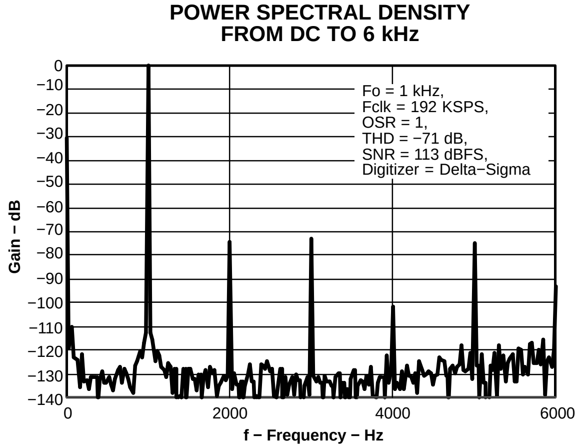


Figure 16.

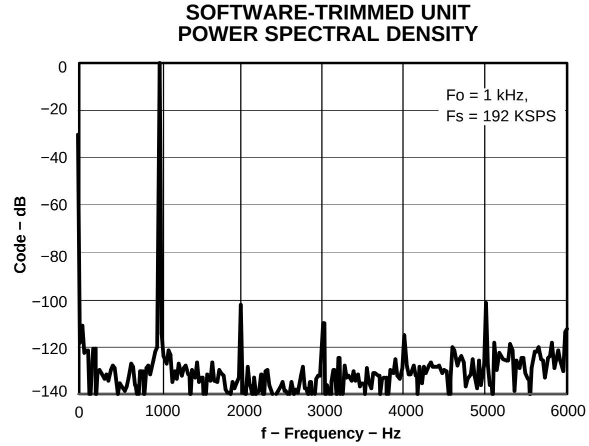


Figure 17.

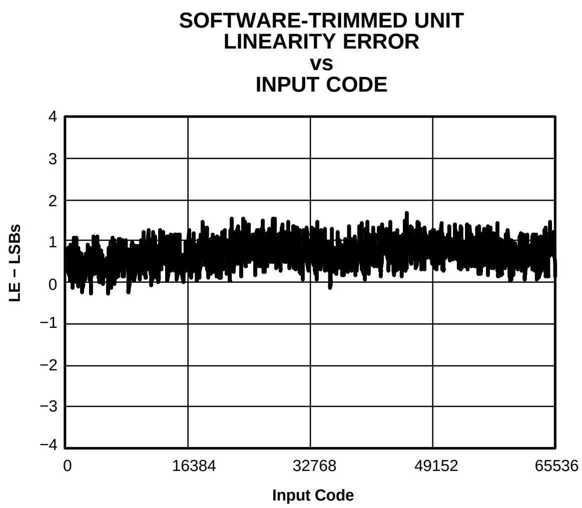


Figure 18.

THEORY OF OPERATION

DAC8581 uses proprietary, monotonic, high-speed resistor string architecture. The 16-bit input data is coded in twos complement, MSB-first format and transmitted using a 3-wire serial interface. The serial interface sends the input data to the DAC latch. The digital data is then decoded to select a tap voltage of the resistor string. The resistor string output is sent to a high-performance output amplifier. The output buffer has rail-to-rail (±5 V) swing capability on a 600-Ω, 200-pF load. The resistor string DAC architecture provides exceptional differential linearity and temperature stability whereas the output buffer provides fast-settling, low-glitch, and exceptionally low idle-channel noise. The DAC8581 settles within 1 µs for large input signals. Exceptionally low glitch (0.5 nV-s) is attainable for small-signal, code-to-code output changes. Resistor string architecture also provides code-independent power consumption and code-independent settling time. The DAC8581 resistor string needs an external reference voltage to set the output voltage range of the DAC. To aid fast settling, VREF input is internally buffered.

Supply Pins

DAC8581 uses ±5-V analog power supplies (AV_{DD}, AV_{SS}) and a 1.8 V–5.5 V digital supply (DV_{DD}). Analog and digital ground pins (AGND and DGND) are also provided. For low-noise operation, analog and digital power and ground pins should be separated. Sufficient bypass capacitors, at least 1 µF, should be placed between AV_{DD} and AV_{SS}, AV_{SS} and DGND, and DV_{DD} and DGND pins. Series inductors are *not* recommended on the supply paths. The digital input pins should not exceed the ground potential during power up. During power up, AGND and DGND are first applied with all digital inputs and the reference input kept zero volts. Then, AV_{DD}, DV_{DD}, AV_{SS}, and V_{REF} should be applied together. Care should be taken to avoid applying V_{REF} before AV_{DD} and AV_{SS}. All digital pins must be kept at ground potential before power up.

Reference Input Voltage

The reference input pin V_{REF} is typically tied to a +3.3 V, +4.096 V, or +5.0 V external reference. A bypass capacitor 0.1 µF or less is recommended depending on the load-driving capability of the voltage reference. To reduce crosstalk and improve settling time, the V_{REF} pin is internally buffered by a high-performance amplifier. The V_{REF} pin has constant 5-kΩ impedance to AGND. The output range of the DAC8581 is equal to $\pm V_{REF}$ voltage. The V_{REF} pin should be powered at the same time, or after the supply pins. REF3133 and REF3140 are recommended to set the DAC8581 output range to ±3.3 V and ±4.096 V, respectively.

Output Voltage

The input data format is in twos-complement format as shown in Table 1. DAC8581 uses a high-performance, rail-to-rail output buffer capable of driving a 600-Ω, 200-pF load with fast 0.65-µs settling. The buffer has exceptional noise performance (20 $nV/\sqrt{Hz}$) and fast slew rate (35 V/µs). The small-signal settling time is under 300 ns, allowing update rates up to 3 MSPS. Loads of 50 Ω or 75 Ω could be driven as long as output current does not exceed ±25 mA continuously. Long cables, up to 1 nF in capacitance, can be driven without the use of external buffers. To aid stability under large capacitive loads (>1 nF), a small series resistor can be used at the output.

Table 1. Data Format

DAC OUTPUT	DIGITAL CODE	
	BINARY	HEX
+Vref	0111111111111111	7FFF
+Vref/2	0100000000000000	4FFF
0	0000000000000000	0000
–Vref/2	1011111111111111	BFFF
–Vref	1000000000000000	8000

Glitch area is low at 0.5 nV-s, with peak glitch amplitude under 10 mV, and the glitch duration under 100 ns. Low glitch is obtained for code-to-code (small signal) changes across the entire transfer function of the device. For large signals, settling characteristics of the reference and output amplifiers are observed in terms of overshoot and undershoot.

Combined with ±5-V output range, and extremely good noise performance, the outstanding differential linearity performance of this device becomes significant. That is, each DAC step can be clearly observed at the DAC output, without being corrupted by wideband noise.

SERIAL INTERFACE

The DAC8581 serial interface consists of the serial data input pin SDIN, bit clock pin SCLK, and chip-select pin $\overline{CS}$. The serial interface is designed to support the industry standard SPI interface up to 50 MHz. The serial inputs are 1.8-V to 5.5-V logic compatible.

$\overline{CS}$ operates as an active-low, chip-select signal. The falling edge of $\overline{CS}$ initiates the data transfer. Each rising edge of SCLK following the falling edge of $\overline{CS}$ shifts the SDIN data into a 16-bit shift register, MSB-first. At the 16^{th} rising edge of SCLK, the shift register becomes full and the DAC data updates on the falling edge that follows the 16^{th} rising edge. After the data update, further clocking gets ignored. The sequence restarts at the next falling edge of $\overline{CS}$. If the $\overline{CS}$ is brought high before the DAC data is updated, the data is ignored. See the Figure 1 timing diagram for details.

Pin $\overline{CLR}$

Pin $\overline{CLR}$ is implemented to set the DAC output to 0 V. When the $\overline{CS}$ pin is low during the 16th SCLK cycle following the falling edge of $\overline{CS}$, the falling edge of 16^{th} SCLK sets the DAC latch to midcode, and the DAC output to 0 V. If the $\overline{CLR}$ pin is high during the 16^{th} clock, the falling edge of 16th clock updates the DAC latch with the input data. Therefore, if the $\overline{CLR}$ pin is brought back to High from Low during serial communication, the DAC output stays at 0 V until the falling edge of the next 16th clock is received. The $\overline{CLR}$ pin is active low. The $\overline{CLR}$ low does not affect the serial data transfer. The serial data input does not get interrupted or lost while the output is set at midscale.

SCLK

This digital input pin is the serial bit-clock. Data is clocked in the device at the rising edge of SCLK.

$\overline{CS}$

This digital input pin is the chip-select signal. When $\overline{CS}$ is low, the serial port is enabled and data can be transferred into the device. When $\overline{CS}$ is high, all SCLK and SDIN signals are ignored.

SDIN

This digital input is the serial data input. Serial data is shifted on the rising edge of the SCLK when $\overline{CS}$ is low.

APPLICATION INFORMATION

IMPROVING DAC8581 LINEARITY USING EXTERNAL CALIBRATION

At output frequencies up to 50 kHz, DAC8581 linearity error and total harmonic distortion are dominated by resistor mismatches in the string. These resistor mismatches are fairly insensitive to temperature and aging effects and also to reference voltage changes. Therefore, it is possible to use a piece-wise linear (PWL) approximation to cancel linearity errors, and the calibration will remain effective for different supply and Vref voltages, etc. The cancellation of linearity errors also improves the total harmonic distortion (THD) performance. It is possible to improve the integral linearity errors from ±25 LSB to ±1 LSB and the THD from –70 dB to almost –98 dB (see Figure 17 and Figure 18). The improvements are at the expense of ~2X DNL deterioration, which is not critical for the generation of large-signal waveforms.

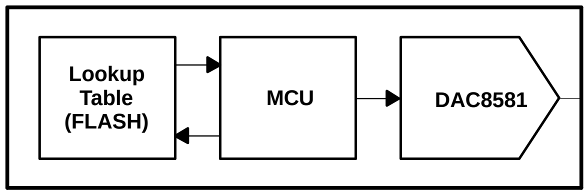


Figure 19. A Simple Printed-Circuit Board Scheme for Calibrated Use of DAC8581

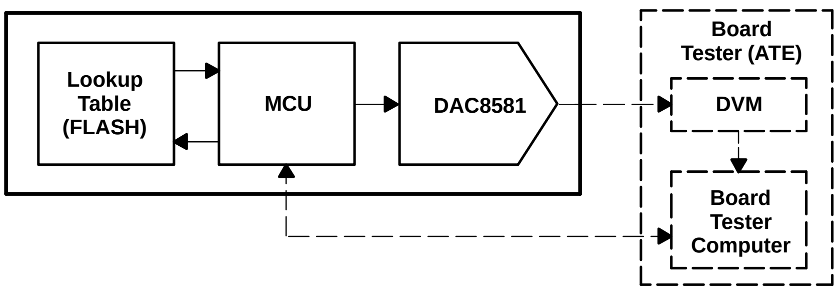


Figure 20. Production Test Setup for a DAC8581 Board With Calibration

The PWL calibration scheme uses a DAC8581 and a microcontroller unit (MCU) with flash memory, on a printed-circuit board as seen in Figure 19. Calibration is done during board test, and the calibration coefficients are stored permanently in flash memory as seen in Figure 20. An automated board tester is assumed to have a precision digital voltmeter (DVM) and a tester computer. The test flow for a 1024-segment, piece-wise linear calibration is as follows:

1. Use the tester computer to load software into the MCU to ramp the DAC8581 and
   - take a reading at each step after a short wait time
   - store 65,536 readings in tester computer's volatile memory
2. Use the tester computer to
   - search the 65,536-point capture data and find the actual DAC8581 codes which would generate ideal DAC outputs for DAC input codes 0, 64, 128, 192, … .
   - store these actual codes in the onboard microcontroller's flash memory in a 1025-point array called COEFF[].
3. Use the tester computer to program the MCU such that, when the end-user provides new 16-bit input data D0 to the MCU
   - The 10 MSBs of D0 directly index the array COEFF[].
   - The content of indexed memory of COEFF and the content of the next higher memory location are placed in variables I1 and I2.
   - The 6 LSBs of the user data D0 with two variables I1 and I2 are used for computing Equation 1 (See Figure 21).
   - Instead of D0, I0 is loaded to DAC8581

APPLICATION INFORMATION (continued)

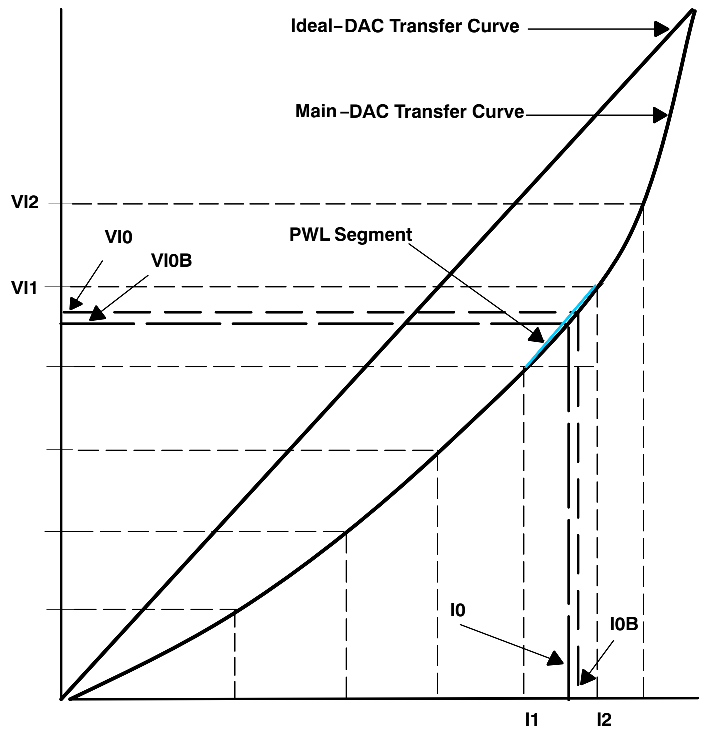


Figure 21. The Geometry Behind the PWL Calibration

$$I0 = \frac{I1 + (I2 - I1)(D0 - VI1)}{VI2 - VI1} \tag{1}$$

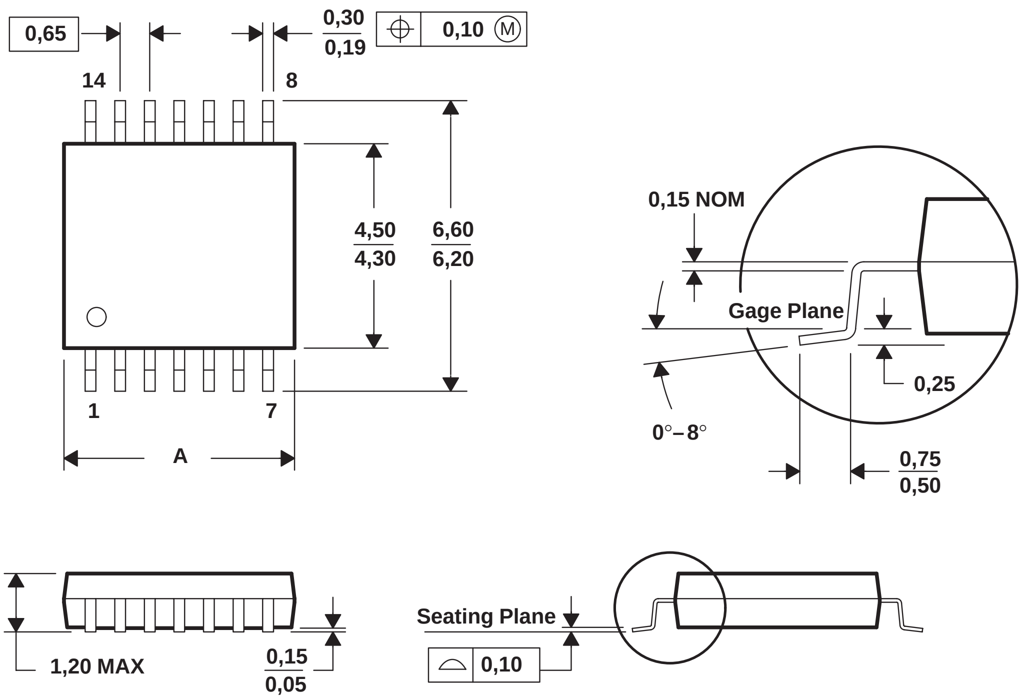
Where both x-axis and y-axis are normalized from 0 to 65535, and,

- VI0: Desired ideal DAC voltage corresponding to input code D0.
- VI0B: DAC8581 output voltage, which approximates VI0 after PWL calibration. This is the actual DAC8581 output for input code D0 after PWL calibration.
- I0: DAC8581 code generating VI0B, an approximation to the desired voltage VI0. This is actual code loaded into DAC latch for input code D0, after PWL calibration.
- I0B: DAC8581 code, which generates output VI0. This code is approximated by the N-segment PWL calibration.
- I1: Contents of memory COEFF, addressed by the 10 MSBs of user input code D0.
- I2: Contents of the next memory location in COEFF.
- VI1: DAC8581 output voltage corresponding to code I1. Notice that (D0–VI1) is nothing but the 6 LSBs of the input code D0, given that the y-axis is normalized from 0 to 65,536.
- VI2: DAC8581 output voltage corresponding to code I2. Notice that (VI2–VI1) is always equal to number 64, given that the y-axis is normalized from 0 to 65,536. Division becomes a 6-bit arithmetic right shift.

Other similar PWL calibration implementations exist. This particular algorithm does not need digital division, and it does not accumulate measurement errors at each segment.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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