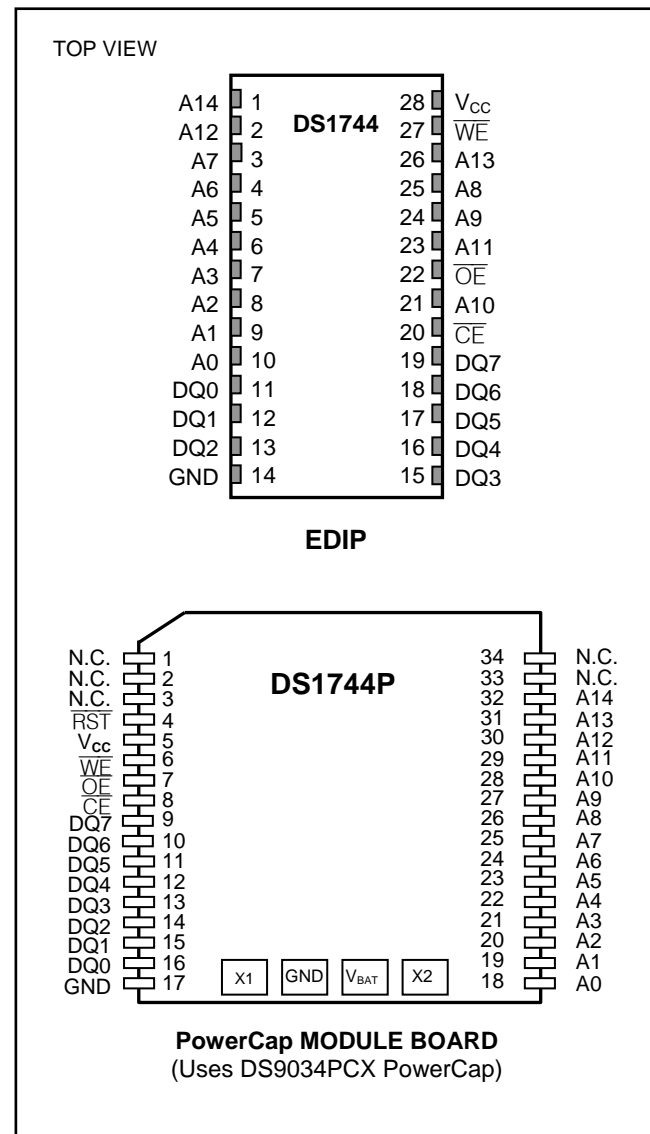


## FEATURES

- Integrated NV SRAM, Real-Time Clock, Crystal, Power-Fail Control Circuit, and Lithium Energy Source
- Clock Registers are Accessed Identically to the Static RAM. These Registers are Resident in the Eight Top RAM Locations.
- Century Byte Register (i.e., Y2K Compliant)
- Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power
- BCD-Coded Century, Year, Month, Date, Day, Hours, Minutes, and Seconds with Automatic Leap-Year Compensation Valid Up to the Year 2100
- Battery Voltage-Level Indicator Flag
- Power-Fail Write Protection Allows for  $\pm 10\%$   $V_{CC}$  Power-Supply Tolerance
- Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time
- DIP Module Only  
Standard JEDEC Byte-Wide 32k x 8 Static RAM Pinout
- PowerCap<sup>®</sup> Module Board Only  
Surface-Mountable Package for Direct Connection to PowerCap Containing Battery and Crystal  
Replaceable Battery (PowerCap)  
Power-On Reset Output  
Pin-for-Pin Compatible with Other Densities of DS174xP Timekeeping RAM
- Also Available in Industrial Temperature Range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- UL Recognized

## PIN CONFIGURATIONS



PowerCap is a registered trademark of Maxim Integrated Products, Inc.

**PIN DESCRIPTION**

PIN		NAME	FUNCTION
EDIP	PowerCap		
1	32	A14	Address Input
2	30	A12	
3	25	A7	
4	24	A6	
5	23	A5	
6	22	A4	
7	21	A3	
8	20	A2	
9	19	A1	
10	18	A0	
21	28	A10	
23	29	A11	
24	27	A9	
25	26	A8	
26	31	A13	
11	16	DQ0	Data Input/Output
12	15	DQ1	
13	14	DQ2	
15	13	DQ3	
16	12	DQ4	
17	11	DQ5	
18	10	DQ6	
19	9	DQ7	
14	17	GND	Ground
20	8	$\overline{\text{CE}}$	Active-Low Chip-Enable Input
22	7	$\overline{\text{OE}}$	Active-Low Output-Enable Input
27	6	$\overline{\text{WE}}$	Active-Low Write-Enable Input
28	5	V <sub>CC</sub>	Power-Supply Input
—	4	$\overline{\text{RST}}$	Active-Low Reset Output, Open Drain. Requires a pullup resistor for proper operation.
—	1, 2, 3, 33, 34	N.C.	No Connection
—		X1, X2, V <sub>BAT</sub>	Crystal Connections, V <sub>BAT</sub> Battery Connection

**ORDERING INFORMATION**

<b>PART</b>	<b>VOLTAGE (V)</b>	<b>TEMP RANGE</b>	<b>PIN-PACKAGE</b>	<b>TOP MARK**</b>
<b>DS1744-70</b>	5.0	0°C to +70°C	28 EDIP	DS1744-70
DS1744-70+	5.0	0°C to +70°C	28 EDIP	DS1744+70
DS1744-70IND	5.0	-40°C to +85°C	28 EDIP	DS1744-70IND
DS1744-100+	5.0	0°C to +70°C	28 EDIP	DS1744+100
DS1744W-120	3.3	0°C to +70°C	28 EDIP	DS1744W-120
DS1744W-120+	3.3	0°C to +70°C	28 EDIP	DS1744W+120
DS1744W-120IND	3.3	-40°C to +85°C	28 EDIP	DS1744W-120IND
<b>DS1744P-70</b>	5.0	0°C to +70°C	34 PowerCap*	DS1744P-70
DS1744P-70+	5.0	0°C to +70°C	34 PowerCap*	DS1744P+70
DS1744P-70IND	5.0	-40°C to +85°C	34 PowerCap*	DS1744P-70IND
DS1744P-100+	5.0	0°C to +70°C	34 PowerCap*	DS1744P+100
DS1744WP-120	3.3	0°C to +70°C	34 PowerCap*	DS1744WP-120
DS1744WP-120+	3.3	0°C to +70°C	34 PowerCap*	DS1744WP+120
DS1744WP-120IND	3.3	-40°C to +85°C	34 PowerCap*	DS1744WP-120IND

+ Denotes a lead-free/RoHS-compliant device.

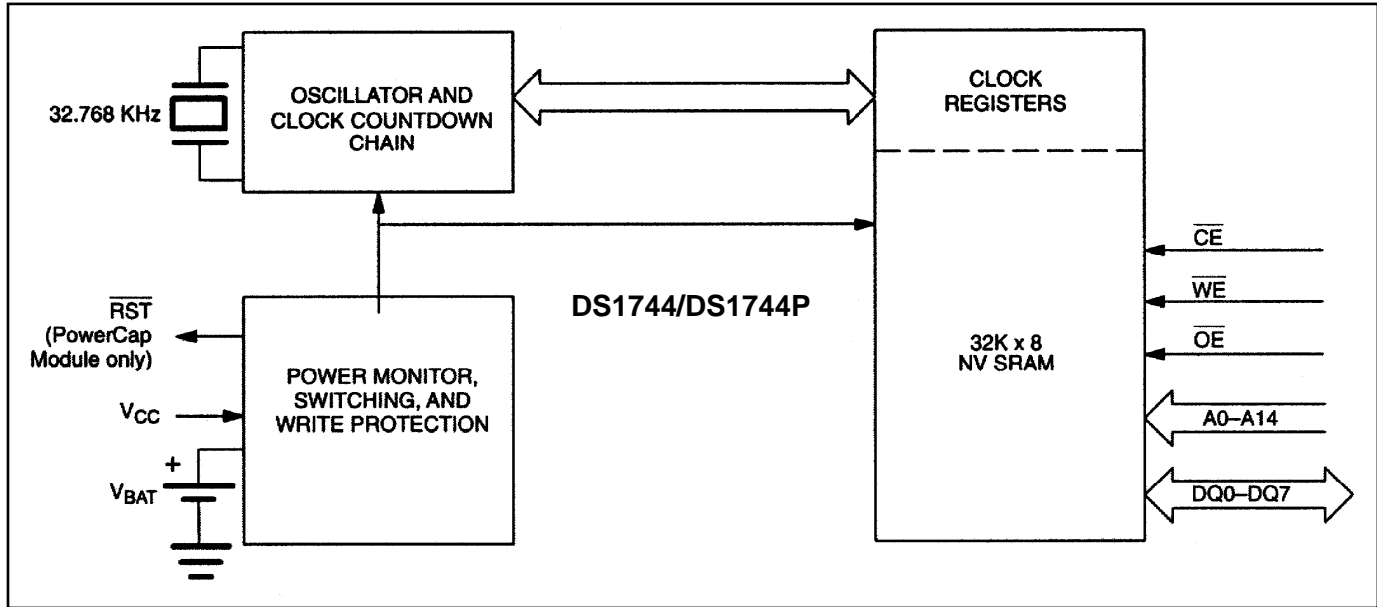
\*DS9034-PCX, DS9034I-PCX, DS9034-PCX+ required (must be ordered separately).

\*\* A "+" anywhere in the top mark denotes a lead-free device. An "IND" denotes an industrial temperature grade device.

**DESCRIPTION**

The DS1744 is a full-function, year-2000-compliant (Y2KC), real-time clock/calendar (RTC) and 32k x 8 NV SRAM. User access to all registers within the DS1744 is accomplished with a byte-wide interface as shown in Figure 1. The RTC information and control bits reside in the eight uppermost RAM locations. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the date of each month and leap year are made automatically. The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1744 also contains its own power-fail circuitry that deselected the device when the V<sub>CC</sub> supply is in an out-of-tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V<sub>CC</sub> as errant access and update cycles are avoided.

Figure 1. DS1744/DS1744P Block Diagram



## PACKAGES

The DS1744 is available in two packages (28-pin encapsulated DIP and 34-pin PowerCap module). The 28-pin EDIP module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap module board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1744P after the completion of the surface-mount process. Mounting the PowerCap after the surface-mount process prevents damage to the crystal and battery due to the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap module board and PowerCap are ordered separately and shipped in separate containers. The part number for the PowerCap is DS9034PCX.

## CLOCK OPERATIONS—READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1744 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, bit 6 of the century register (Table 2). As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is, day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that the clock accuracy is not affected by the access of data. All the DS1744 registers are updated simultaneously after the internal clock-register updating process has been re-enabled. Updating is within a second after the read bit is written to 0. The READ bit must be a 0 for a minimal of 500 $\mu$ s to ensure the external registers are updated.

**Table 1. Truth Table**

$V_{CC}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
$V_{CC} > V_{PF}$	$V_{IH}$	X	X	Deselect	High-Z	Standby
	$V_{IL}$	X	$V_{IL}$	Write	Data In	Active
	$V_{IL}$	$V_{IL}$	$V_{IH}$	Read	Data Out	Active
	$V_{IL}$	$V_{IH}$	$V_{IH}$	Read	High-Z	Active
$V_{SO} < V_{CC} < V_{PF}$	X	X	X	Deselect	High-Z	CMOS Standby
$V_{CC} < V_{SO} < V_{PF}$	X	X	X	Deselect	High-Z	Data-Retention Mode

## SETTING THE CLOCK

As shown in Table 2, bit 7 of the century register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1744 registers. The user can then load them with the correct day, date, and time data in 24-hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume.

## STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator can be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The  $\overline{OSC}$  bit is the MSB (bit 7) of the seconds registers (Table 2). Setting it to a 1 stops the oscillator.

## FREQUENCY TEST BIT

As shown in Table 2, bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the seconds register toggles at 512Hz. When the seconds register is being read, the DQ0 line toggles at the 512Hz frequency as long as conditions for access remain valid (i.e.,  $\overline{CE}$  low,  $\overline{OE}$  low,  $\overline{WE}$  high, and address for seconds register remain valid and stable).

## CLOCK ACCURACY (DIP MODULE)

The DS1744 is guaranteed to keep time accuracy to within  $\pm 1$  minute per month at  $+25^{\circ}\text{C}$ . The RTC is calibrated at the factory by Dallas Semiconductor using nonvolatile tuning elements, and does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary. Clock accuracy is also affected by the electrical environment; caution should be taken to place the RTC in the lowest-level EMI section of the PC board layout. For additional information, refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*.

## CLOCK ACCURACY (PowerCap MODULE)

The DS1744 and DS9034PCX are individually tested for accuracy. Once mounted together, the module typically keeps time accuracy to within  $\pm 1.53$  minutes per month (35ppm) at  $+25^{\circ}\text{C}$ . Clock accuracy is also affected by the electrical environment and caution should be taken to place the RTC in the lowest-level EMI section of the PC board layout. For additional information, refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*.

**Table 2. Register Map**

ADDRESS	DATA								FUNCTION	RANGE
	B7	B6	B5	B4	B3	B2	B1	B0		
7FFF	10 Year				Year				Year	00-99
7FFE	X	X	X	10 Month	Month				Month	01-12
7FFD	X	X	10 Date		Date				Date	01-31
7FFC	BF	FT	X	X	X	Day			Day	01-07
7FFB	X	X	10 Hour		Hour				Hour	00-23
7FFA	X	10 Minutes			Minutes				Minutes	00-59
7FF9	OSC	10 Seconds			Seconds				Seconds	00-59
7FF8	W	R	10 Century		Century				Century	00-39

 $\overline{\text{OSC}}$  = Stop Bit

R = Read Bit

FT = Frequency Test

W = Write Bit

X = See Note

BF = Battery Flag

**Note:** All indicated “X” bits are not used but must be set to a “0” during write cycle to ensure proper clock operation.

## RETRIEVING DATA FROM RAM OR CLOCK

The DS1744 is in the read mode whenever  $\overline{\text{OE}}$  (output enable) is low,  $\overline{\text{WE}}$  (write enable) is high, and  $\overline{\text{CE}}$  (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data is available at the DQ pins within  $t_{AA}$  after the last address input is stable, providing that the  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  access times and states are satisfied. If  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  access times and states are not met, valid data is available at the latter of chip-enable access ( $t_{CEA}$ ) or at output-enable access time ( $t_{OEA}$ ). The state of the DQ pins is controlled by  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$ . If the outputs are activated before  $t_{AA}$ , the data lines are driven to an intermediate state until  $t_{AA}$ . If the address inputs are changed while  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  remain valid, output data remains valid for output-data hold time ( $t_{OH}$ ) but then goes indeterminate until the next address access.

## WRITING DATA TO RAM OR CLOCK

The DS1744 is in the write mode whenever  $\overline{\text{WE}}$  and  $\overline{\text{CE}}$  are in their active state. The start of a write is referenced to the latter occurring transition of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$ . The addresses must be held valid throughout the cycle.  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  must return inactive for a minimum of  $t_{WR}$  prior to the initiation of another read or write cycle. Data in must be valid  $t_{DS}$  prior to the end of write and remain valid for  $t_{DH}$  afterward. In a typical application, the  $\overline{\text{OE}}$  signal is high during a write cycle. However,  $\overline{\text{OE}}$  can be active provided that care is taken with the data bus to avoid bus contention. If  $\overline{\text{OE}}$  is low prior to  $\overline{\text{WE}}$  transitioning low, the data bus can become active with read data defined by the address inputs. A low transition on  $\overline{\text{WE}}$  then disables the output  $t_{WEZ}$  after  $\overline{\text{WE}}$  goes active.

## DATA-RETENTION MODE

The 5V device is fully accessible and data can be written or read only when  $V_{CC}$  is greater than  $V_{PF}$ . However, when  $V_{CC}$  is below the power-fail point,  $V_{PF}$  (point at which write protection occurs), the internal clock registers and SRAM are blocked from any access. At this time the power-fail reset-output signal ( $\overline{RST}$ ) is driven active and remains active until  $V_{CC}$  returns to nominal levels. When  $V_{CC}$  falls below the battery switch point  $V_{SO}$  (battery supply level), device power is switched from the  $V_{CC}$  pin to the backup battery. RTC operation and SRAM data are maintained from the battery until  $V_{CC}$  is returned to nominal levels. The 3.3V device is fully accessible, and data can be written or read only when  $V_{CC}$  is greater than  $V_{PF}$ . When  $V_{CC}$  falls below  $V_{PF}$  access to the device is inhibited. At this time the power-fail reset-output signal ( $\overline{RST}$ ) is driven active and remains active until  $V_{CC}$  returns to nominal levels. If  $V_{PF}$  is less than  $V_{SO}$ , the device power is switched from  $V_{CC}$  to the backup supply ( $V_{BAT}$ ) when  $V_{CC}$  drops below  $V_{PF}$ . If  $V_{PF}$  is greater than  $V_{SO}$ , the device power is switched from  $V_{CC}$  to the backup supply ( $V_{BAT}$ ) when  $V_{CC}$  drops below  $V_{SO}$ . RTC operation and SRAM data are maintained from the battery until  $V_{CC}$  is returned to nominal levels. The  $\overline{RST}$  signal is an open-drain output and requires a pullup. Except for the  $\overline{RST}$ , all control, data, and address signals must be powered down when  $V_{CC}$  is powered down.

## BATTERY LONGEVITY

The DS1744 has a lithium power source that is designed to provide energy for clock activity and clock and RAM data retention when the  $V_{CC}$  supply is not present. The capability of this internal power supply is sufficient to power the DS1744 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at +25°C with the internal clock oscillator running in the absence of  $V_{CC}$  power. Each DS1744 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{CC}$  is first applied at a level greater than  $V_{PF}$ , the lithium energy source is enabled for battery-backup operation. Actual life expectancy of the DS1744 is much longer than 10 years since no lithium battery energy is consumed when  $V_{CC}$  is present.

## BATTERY MONITOR

The DS1744 constantly monitors the battery voltage of the internal battery. The battery flag bit (bit 7) of the day register is used to indicate the voltage-level range of the battery. This bit is not writable and should always be a 1 when read. If a 0 is ever present, an exhausted lithium energy source is indicated, and both the contents of the RTC and RAM are questionable.

**ABSOLUTE MAXIMUM RATINGS**

Voltage Range on Any Pin Relative to

Ground.....-0.3V to +6.0V

Operating Temperature Range.....-40°C to +85°C

(noncondensing)

Storage Temperature Range.....-40°C to +85°C

(noncondensing)

Soldering Temperature.....See IPC/JEDEC J-STD-020 Specification

(EDIP, Note 7)

*This is a stress rating only and functional operation of the device at these or any other condition beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.*

**OPERATING RANGE**

RANGE	TEMP RANGE	V <sub>CC</sub>
Commercial	0°C to +70°C, Noncondensing	3.3V ±10% or 5V±10%
Industrial	-40°C to +85°C, Noncondensing	3.3V ±10% or 5V±10%

**RECOMMENDED DC OPERATING CONDITIONS**(T<sub>A</sub> = Over the operating range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage (All Inputs) V <sub>CC</sub> = 5V ±10% V <sub>CC</sub> = 3.3V ±10%	V <sub>IH</sub>	2.2		V <sub>CC</sub> + 0.3V	V	1
	V <sub>IH</sub>	2.0		V <sub>CC</sub> + 0.3V	V	
Logic 0 Voltage (All Inputs) V <sub>CC</sub> = 5V ±10% V <sub>CC</sub> = 3.3V ±10%	V <sub>IL</sub>	-0.3		0.8	V	
	V <sub>IL</sub>	0.3		0.6	V	1

**DC ELECTRICAL CHARACTERISTICS**(V<sub>CC</sub> = 5.0V ±10%, T<sub>A</sub> = Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I <sub>CC</sub>			75	mA	2, 3
TTL Standby Current ( $\overline{CE} = V_{IH}$ )	I <sub>CC1</sub>			6	mA	2, 3
CMOS Standby Current ( $\overline{CE} \geq V_{CC} - 0.2V$ )	I <sub>CC2</sub>			4	mA	2, 3
Input Leakage Current (Any Input)	I <sub>IL</sub>	-1		+1	μA	
Output Leakage Current (Any Output)	I <sub>OL</sub>	-1		+1	μA	
Output Logic 1 Voltage (I <sub>OUT</sub> = -1.0mA)	V <sub>OH</sub>	2.4				1
Output Logic 0 Voltage (I <sub>OUT</sub> = +2.1mA)	V <sub>OL</sub>			0.4		1



Write Protection Voltage	$V_{PF}$	4.25	4.50	V	1
Battery Switchover Voltage	$V_{SO}$	$V_{BAT}$			1, 4

**DC ELECTRICAL CHARACTERISTICS**(V<sub>CC</sub> = 3.3V ±10%, T<sub>A</sub> = Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I <sub>CC</sub>			30	mA	2, 3
TTL Standby Current ( $\overline{CE} = V_{IH}$ )	I <sub>CC1</sub>			2	mA	2, 3
CMOS Standby Current ( $\overline{CE} \geq V_{CC} - 0.2V$ )	I <sub>CC2</sub>			2	mA	2, 3
Input Leakage Current (Any Input)	I <sub>IL</sub>	-1		+1	μA	
Output Leakage Current (Any Output)	I <sub>OL</sub>	-1		+1	μA	
Output Logic 1 Voltage (I <sub>OUT</sub> = -1.0mA)	V <sub>OH</sub>	2.4				1
Output Logic 0 Voltage (I <sub>OUT</sub> = +2.1mA)	V <sub>OL</sub>			0.4		1
Write Protection Voltage	V <sub>PF</sub>	2.80		2.97	V	1
Battery Switchover Voltage	V <sub>SO</sub>		V <sub>BAT</sub> or V <sub>PF</sub>		V	1, 4

**AC CHARACTERISTICS—READ CYCLE (5V)**(V<sub>CC</sub> = 5.0V ±10%, T<sub>A</sub> = Over the operating range.)

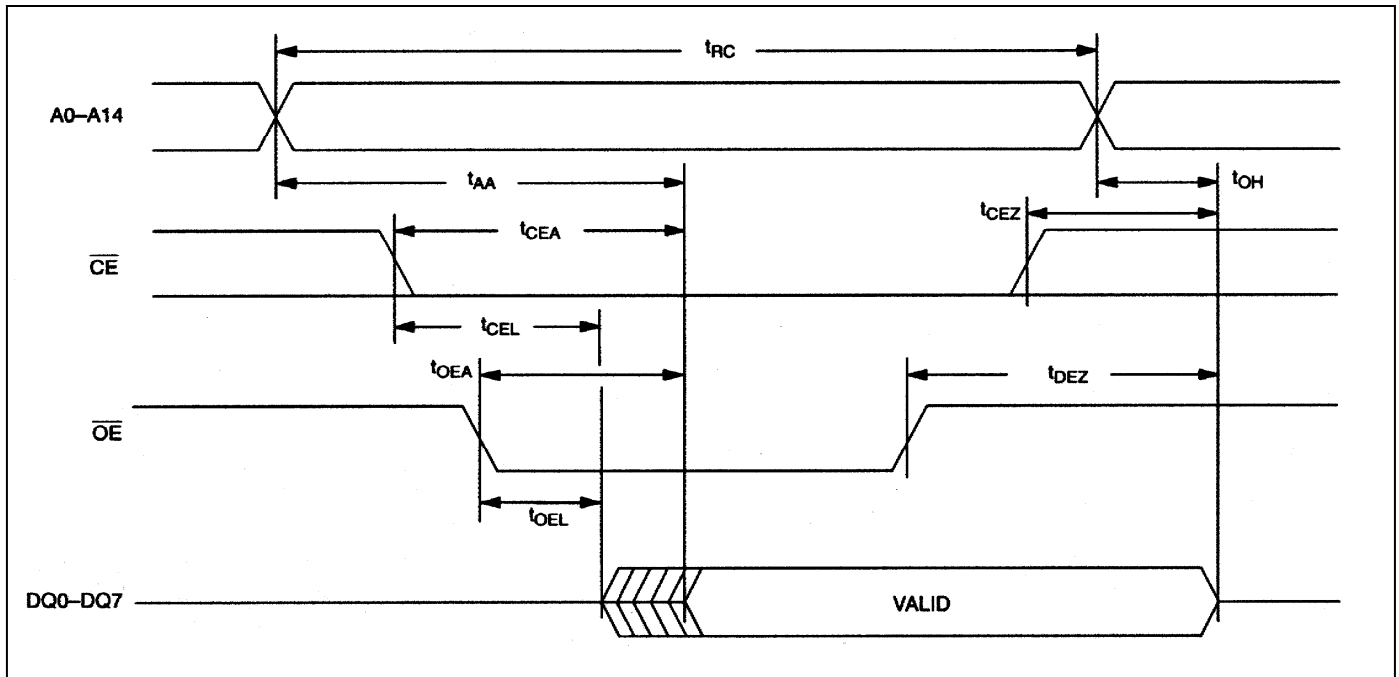
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	70			ns	
Address Access Time	t <sub>AA</sub>			70	ns	
$\overline{CE}$ to DQ Low-Z	t <sub>CEL</sub>	5			ns	
$\overline{CE}$ Access Time	t <sub>CEA</sub>			70	ns	
$\overline{CE}$ Data Off Time	t <sub>CEZ</sub>			25	ns	
$\overline{OE}$ to DQ Low-Z	t <sub>OEL</sub>	5			ns	
$\overline{OE}$ Access Time	t <sub>OEA</sub>			35	ns	
$\overline{OE}$ Data Off Time	t <sub>OEZ</sub>			25	ns	
Output Hold from Address	t <sub>OH</sub>	5			ns	

### AC CHARACTERISTICS—READ CYCLE (3.3V)

( $V_{CC} = 3.3V \pm 10\%$ ,  $T_A =$  Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	$t_{RC}$	120			ns	
Address Access Time	$t_{AA}$			120	ns	
$\overline{CE}$ to DQ Low-Z	$t_{CEL}$	5			ns	
$\overline{CE}$ Access Time	$t_{CEA}$			120	ns	
$\overline{CE}$ Data Off Time	$t_{CEZ}$			40	ns	
$\overline{OE}$ to DQ Low-Z	$t_{OEL}$	5			ns	
$\overline{OE}$ Access Time	$t_{OEA}$			100	ns	
$\overline{OE}$ Data Off Time	$t_{OEZ}$			35	ns	
Output Hold from Address	$t_{OH}$	5			ns	

### READ CYCLE TIMING DIAGRAM



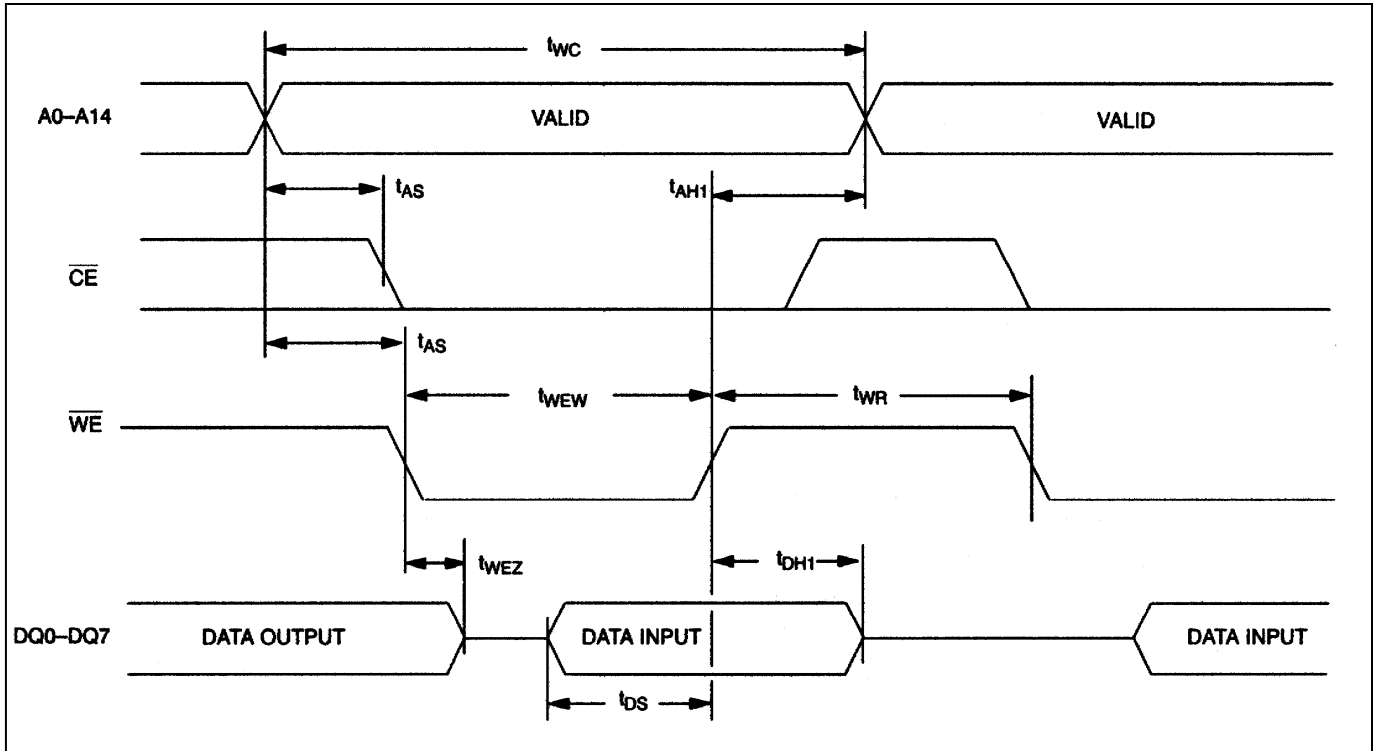
**AC CHARACTERISTICS—WRITE CYCLE (5V)**(V<sub>CC</sub> = 5.0V ±10%, T<sub>A</sub> = Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t <sub>WC</sub>	70			ns	
Address Setup Time	t <sub>AS</sub>	0			ns	
$\overline{\text{WE}}$ Pulse Width	t <sub>WEW</sub>	50			ns	
$\overline{\text{CE}}$ Pulse Width	t <sub>CEW</sub>	60			ns	
Data Setup Time	t <sub>DS</sub>	30			ns	
Data Hold Time	t <sub>DH1</sub>	0			ns	8
Data Hold Time	t <sub>DH2</sub>	0			ns	9
Address Hold Time	t <sub>AH1</sub>	5			ns	8
Address Hold Time	t <sub>AH2</sub>	5			ns	9
$\overline{\text{WE}}$ Data Off Time	t <sub>WEZ</sub>			25	ns	
Write Recovery Time	t <sub>WR</sub>	5			ns	

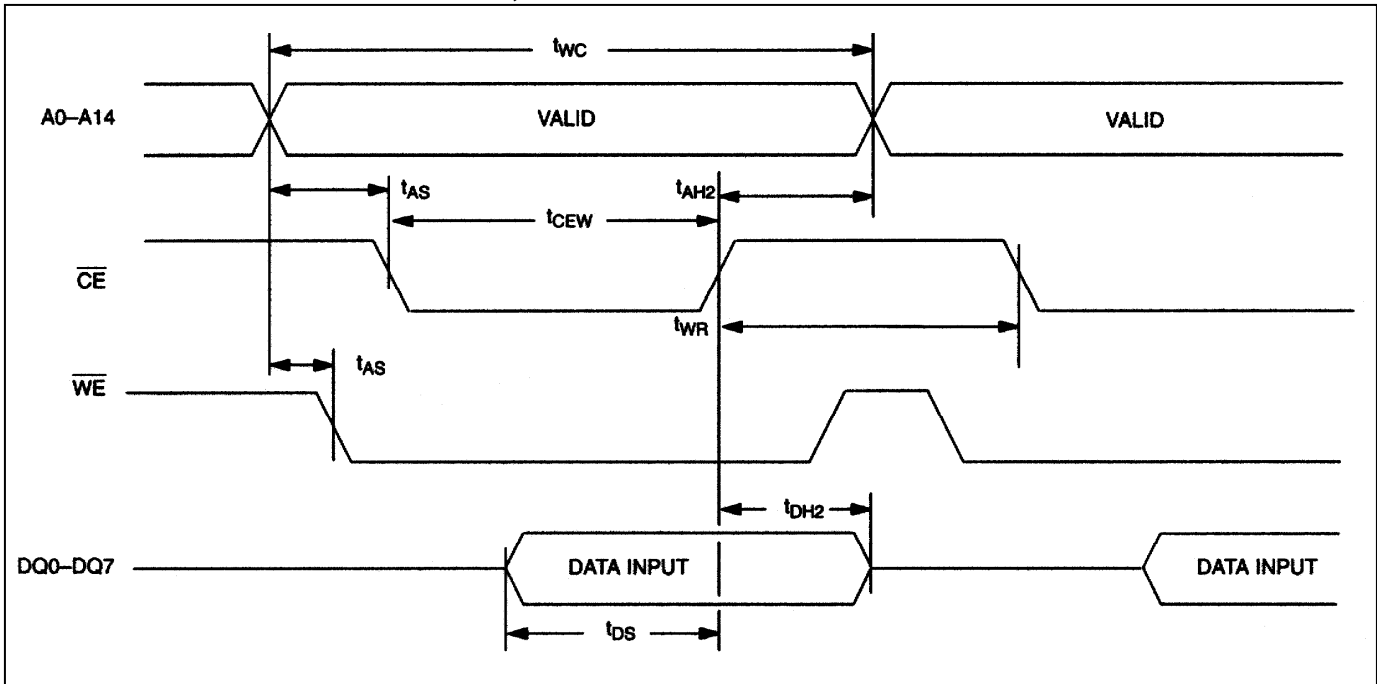
**AC CHARACTERISTICS—WRITE CYCLE (3.3V)**(V<sub>CC</sub> = 3.3V ±10%, T<sub>A</sub> = Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t <sub>WC</sub>	120			ns	
Address Setup Time	t <sub>AS</sub>	0		120	ns	
$\overline{\text{WE}}$ Pulse Width	t <sub>WEW</sub>	100			ns	
$\overline{\text{CE}}$ Pulse Width	t <sub>CEW</sub>	110			ns	
$\overline{\text{CE}}$ and CE2 Pulse Width	t <sub>CEW</sub>	110			ns	
Data Setup Time	t <sub>DS</sub>	80			ns	
Data Hold Time	t <sub>DH1</sub>	0			ns	8
Data Hold Time	t <sub>DH2</sub>	0			ns	9
Address Hold Time	t <sub>AH1</sub>	0			ns	8
Address Hold Time	t <sub>AH2</sub>	10			ns	9
$\overline{\text{WE}}$ Data Off Time	t <sub>WEZ</sub>			40	ns	
Write Recovery Time	t <sub>WR</sub>	10			ns	

**WRITE CYCLE TIMING DIAGRAM, WRITE-ENABLE CONTROLLED**



**WRITE CYCLE TIMING DIAGRAM, CHIP-ENABLE CONTROLLED**

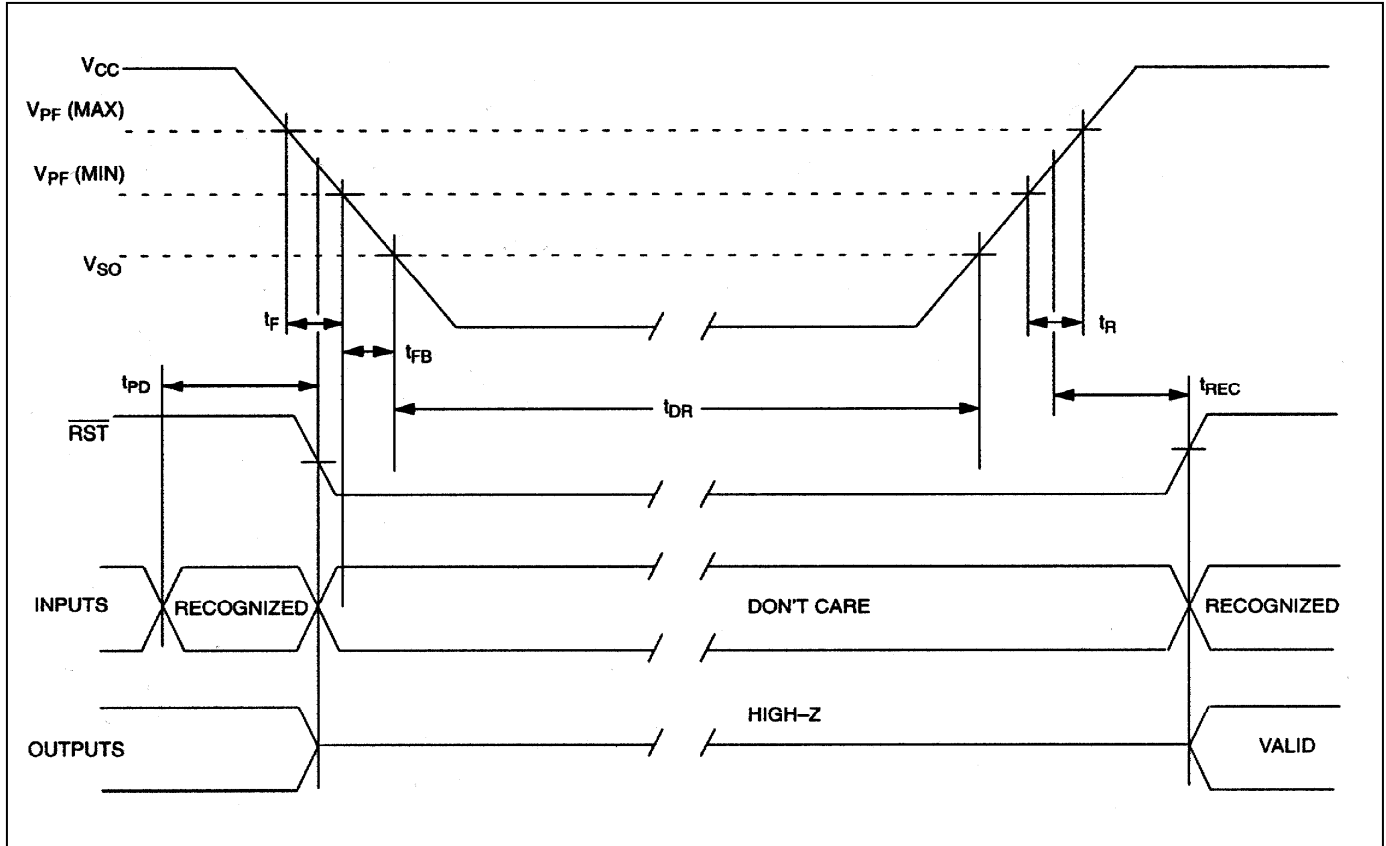


### POWER-UP/DOWN AC CHARACTERISTICS (5V)

( $V_{CC} = 5.0V \pm 10\%$ ,  $T_A =$  Over the operating range.)

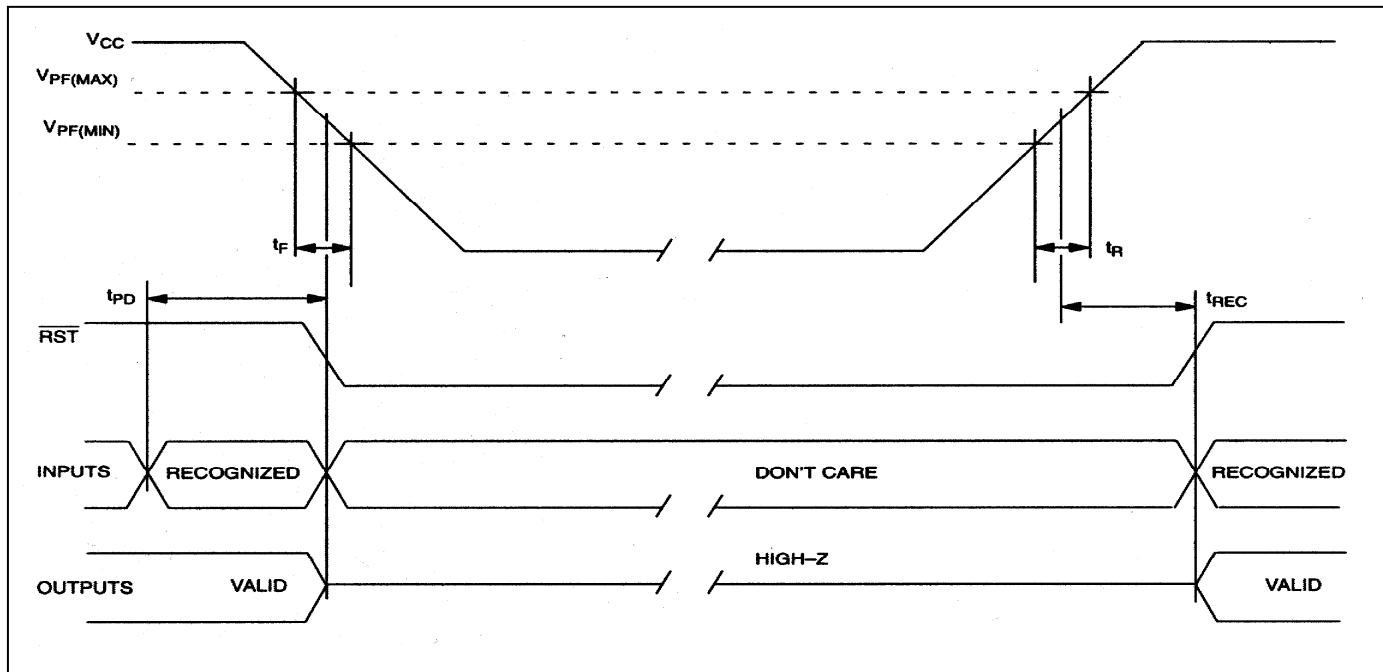
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at $V_{IH}$ Before Power-Down	$t_{PD}$	0			$\mu s$	
$V_{CC}$ Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	$t_F$	300			$\mu s$	
$V_{CC}$ Fall Time: $V_{PF(MIN)}$ to $V_{SO}$	$t_{FB}$	10			$\mu s$	
$V_{CC}$ Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	$t_R$	0			$\mu s$	
Power-Up Recover Time	$t_{REC}$			35	ms	
Expected Data-Retention Time (Oscillator ON)	$t_{DR}$	10			years	5, 6

### POWER-UP/DOWN TIMING (5V DEVICE)



**POWER-UP/DOWN CHARACTERISTICS (3.3V)** $(V_{CC} = 3.3V \pm 10\%, T_A = \text{Over the operating range.})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at $V_{IH}$ , Before Power-Down	$t_{PD}$	0			$\mu\text{s}$	
$V_{CC}$ Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	$t_F$	300			$\mu\text{s}$	
$V_{CC}$ Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	$t_R$	0			$\mu\text{s}$	
$V_{PF}$ to $\overline{RST}$ High	$t_{REC}$			35	ms	
Expected Data-Retention Time (Oscillator ON)	$t_{DR}$	10			years	5, 6

**POWER-UP/DOWN WAVEFORM TIMING (3.3V DEVICE)****CAPACITANCE** $(T_A = +25^\circ\text{C})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance On All Input Pins	$C_{IN}$			14	pF	
Capacitance On All Output Pins	$C_O$			10	pF	

## AC TEST CONDITIONS

Output Load: 50pF + 1TTL Gate

Input Pulse Levels: 0 to 3.0V

Timing Measurement Reference Levels:

Input: 1.5V

Output: 1.5V

Input Pulse Rise and Fall Times: 5ns

## NOTES:

- 1) Voltages are referenced to ground.
- 2) Typical values are at +25°C and nominal supplies.
- 3) Outputs are open.
- 4) Battery switchover occurs at the lower of either the battery terminal voltage or  $V_{PF}$ .
- 5) Data-retention time is at +25°C.
- 6) Each DS1744 has a built-in switch that disconnects the lithium source until the user first applies  $V_{CC}$ . The expected  $t_{DR}$  is defined for DIP modules and assembled PowerCap modules as a cumulative time in the absence of  $V_{CC}$  starting from the time power is first applied by the user.
- 7) RTC modules (DIP) can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used.

In addition, for the PowerCap:

- a.) Dallas Semiconductor recommends that PowerCap module bases experience one pass through solder reflow oriented with the label side up (“live-bug”).
  - b.) Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad, and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflows, and use a solder wick to remove solder.
- 8)  $t_{AH1}$ ,  $t_{DH1}$  are measured from  $\overline{WE}$  going high.
  - 9)  $t_{AH2}$ ,  $t_{DH2}$  are measured from  $\overline{CE}$  going high.

## PACKAGE INFORMATION

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 EDIP	MDF28+3	<a href="#">21-0245</a>
34 PWRCP	PC2+2	<a href="#">21-0246</a>