# LOW INPUT CURRENT HIGH GAIN SPLIT DARLINGTON OPTOCOUPLERS

| | | |
|---|---|---|
| **SINGLE CHANNEL:** | **HCPL-0700** | **HCPL-0701** |
| **DUAL CHANNEL:** | **HCPL-0730** | **HCPL-0731** |

## DESCRIPTION

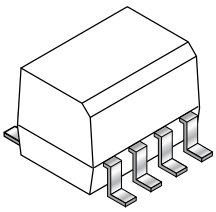
The HCPL-0700, HCPL-0701, HCPL-0730 and HCPL-0731 optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector housed in a compact 8-pin small outline package. The HCPL-0730 and HCPL-0731 devices have two channels per package for optimum mounting density.

The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler.

The combination of a very low input current of 0.5 mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements.

## FEATURES

- Low input current – 0.5 mA
- Superior CTR – 2000%
- Superior CMR – 10 kV/µs
- CTR guaranteed 0-70°C
- U.L. Recognized (file# E90700)
- VDE 0884 recognized (file# 136616)
  – approval pending for HCPL-0730/0731
- BSI recognized (file# 8661, 8662)
  – HCPL-0700/0701 only



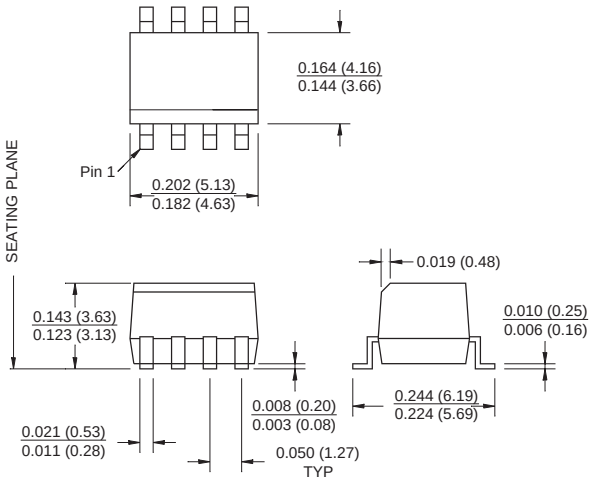
## APPLICATIONS

- Digital logic ground isolation
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- µP bus isolation
- Current loop receiver

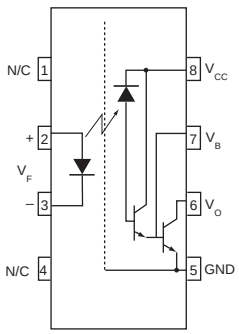
## TRUTH TABLE

| LED | $V_O$ |
|---|---|
| ON | LOW |
| OFF | HIGH |

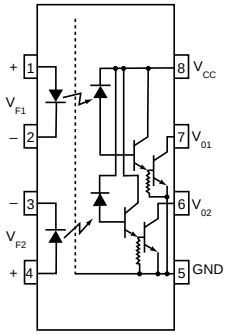
## PACKAGE DIMENSIONS




**NOTE**
All dimensions are in inches (millimeters)




HCPL0700 / HCPL0701




HCPL0730 / HCPL0731

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## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise specified)

| Parameter | | Symbol | Value | Units |
|---|---|---|---|---|
| Storage Temperature | | $T_{STG}$ | -40 to +125 | °C |
| Operating Temperature | | $T_{OPR}$ | -40 to +85 | °C |
| Reflow Temperature Profile (Refer to fig. 11) | | | | |
| **EMITTER** | | | | |
| DC/Average Forward Input Current | | $I_F$ (avg) | 20 | mA |
| Peak Forward Input Current (50% duty cycle, 1 ms P.W.) | | $I_F$ (pk) | 40 | mA |
| Peak Transient Input Current - (≤1 µs P.W., 300 pps) | | $I_F$ (trans) | 1.0 | A |
| Reverse Input Voltage | | $V_R$ | 5 | V |
| Input Power Dissipation | | $P_D$ | 35 | mW |
| **DETECTOR** | | | | |
| Average Output Current (Pin 6) | | $I_O$ (avg) | 60 | mA |
| Emitter-Base Reverse Voltage | HCPL-0700/HCPL-0701 | $V_{EBR}$ | 0.5 | V |
| Supply Voltage, Output Voltage | HCPL-0700/HCPL-0730 | $V_{CC}$, $V_O$ | -0.5 to 7 | V |
| | HCPL-0701/HCPL-0731 | | -0.5 to 18 | |
| Output power dissipation | | $P_D$ | 100 | mW |

## ELECTRICAL CHARACTERISTICS ($T_A$ = 0 to 70°C Unless otherwise specified)

### INDIVIDUAL COMPONENT CHARACTERISTICS

| Parameter | Test Conditions | | Symbol | Device | Min | Typ** | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| **EMITTER** Input Forward Voltage | $I_F$ = 1.6mA | $T_A$ = 25°C | $V_F$ | HCLP-0700/01 | 1.0 | 1.25 | 1.7 | V |
| | | | | HCLP-0730/31 | | 1.35 | | |
| | | | | All | | | 1.75 | |
| Input Reverse Breakdown Voltage | ($T_A$ =25°C, $I_R$ = 10 µA) | | $BV_R$ | All | 5.0 | | | |
| **DETECTOR** Logic high output current | ($I_F$ = 0 mA, $V_O$ = $V_{CC}$ = 18 V) | | $I_{OH}$ | HCPL-0701/31 | | 0.01 | 100 | µA |
| | ($I_F$ = 0 mA, $V_O$ = $V_{CC}$ = 7 V) | | | HCPL-0700/30 | | 0.01 | 250 | |
| Logic Low Supply Current | $I_F$ = 1.6 mA, $V_O$ = Open, $V_{CC}$ = 18V | | $I_{CCL}$ | HCPL-0700/01 | | 0.4 | 1.5 | mA |
| | $I_{F1}$ = $I_{F2}$ = 1.6mA | $V_{CC}$ = 7V | | HCPL-0730 | | 0.8 | 3 | |
| | $V_{O1}$ = $V_{O2}$ = Open | $V_{CC}$ = 18 V | | HCPL-0731 | | 1 | | |
| Logic High Supply Current | $I_F$ = 0 mA, $V_O$ = Open, $V_{CC}$ = 18V | | $I_{CCH}$ | HCPL-0700/01 | | | 10 | µA |
| | $I_{F1}$ = $I_{F2}$ = 0, | $V_{CC}$ = 7V | | HCPL-0730 | | 0.001 | 20 | |
| | $V_{O1}$ = $V_{O2}$ = Open, | $V_{CC}$ = 18 V | | HCPL-0731 | | 0.01 | | |

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**TRANSFER CHARACTERISTICS** ($T_A$ = 0 to 70°C Unless otherwise specified)

| Parameter | Test Conditions | Symbol | Device | Min | Typ** | Max | Unit |
|---|---|---|---|---|---|---|---|
| **COUPLED** | ($I_F$ = 0.5 mA, $V_O$ = 0.4 V, $V_{CC}$ = 4.5V) | CTR | HCPL-0701/31 | 400 | | 5000 | % |
| Current transfer ratio (Notes 1,2) | $I_F$ = 1.6 mA, $V_O$ = 0.4 V, $V_{CC}$ = 4.5V | | HCPL-0700 | 300 | | 2600 | |
| | | | HCPL-0701 | 500 | | 2600 | |
| | | | HCPL-0730 | 300 | | 5000 | |
| | | | HCPL-0731 | 500 | | 5000 | |
| Logic low output voltage output voltage | ($I_F$ = 0.5 mA, $I_O$ = 2 mA, $V_{CC}$ = 4.5V) | $V_{OL}$ | HCPL-0701 HCPL-0731 | | | 0.4 | V |
| | ($I_F$ = 1.6 mA, $I_O$ = 8 mA, $V_{CC}$ = 4.5V) | | | | | 0.4 | |
| | ($I_F$ = 5 mA, $I_O$ = 15 mA, $V_{CC}$ = 4.5V) | | | | | 0.4 | |
| | ($I_F$ = 12 mA, $I_O$ = 24 mA, $V_{CC}$ = 4.5V) | | | | | 0.4 | |
| | ($I_F$ = 1.6 mA, $I_O$ = 4.8 mA, $V_{CC}$ = 4.5V) | | HCPL-0700/0730 | | | 0.4 | |

**ISOLATION CHARACTERISTICS** ($T_A$ = 0 to 70°C Unless otherwise specified)

| Characteristics | Test Conditions | Symbol | Min | Typ** | Max | Unit |
|---|---|---|---|---|---|---|
| Input-output insulation leakage current | (Relative humidity = 45%) ($T_A$ = 25°C, t = 5 s) ($V_{I-O}$ = 3000 VDC) (Note 4) | $I_{I-O}$ | | | 1.0 | µA |
| Withstand insulation test voltage | ($R_H \leq$ 50%, $T_A$ = 25°C) (Note 4, 5) ( t = 1 min.) | $V_{ISO}$ | 2500 | | | $V_{RMS}$ |
| Resistance (input to output) | (Note 4) ($V_{I-O}$ = 500 VDC) | $R_{I-O}$ | | $10^{12}$ | | Ω |

** All typicals at $T_A$ = 25°C

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**SWITCHING CHARACTERISTICS** ($T_A$ = 0 to 70°C unless otherwise specified., $V_{CC}$ = 5 V)

| Parameter | Test Conditions | Symbol | Device | Min | Typ** | Max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay time to logic low (Note 2) (Fig. 14) | ($R_L$ = 4.7 kΩ, $I_F$ = 0.5 mA) | $T_{PHL}$ | HCPL-0701 | | | 30 | µs |
| | | | HCPL-0731 | | | 120 | |
| | $T_A$ = 25°C | | HCPL-0701 | | 3 | 25 | |
| | | | HCPL-0731 | | 5 | 100 | |
| | ($R_L$ = 270 Ω, $I_F$ = 12 mA) | | HCPL-0701 | | | 2 | |
| | | | HCPL-0731 | | | 3 | |
| | $T_A$ = 25°C | | HCPL-0701 | | 0.3 | 1 | |
| | | | HCPL-0731 | | 0.4 | 2 | |
| | ($R_L$ = 2.2 kΩ, $I_F$ = 1.6 mA) | | HCPL-0700 | | | 15 | |
| | | | HCPL-0730/0731 | | | 25 | |
| | $T_A$ = 25°C | | HCPL-0700 | | 1 | 10 | |
| | | | HCPL-0730/0731 | | 2 | 20 | |
| Propagation delay time to logic high (Note 2) (Fig. 14) | ($R_L$ = 4.7 kΩ, $I_F$ = 0.5 mA) | $T_{PLH}$ | HCPL-0701/31 | | | 90 | µs |
| | $T_A$ = 25°C | | HCPL-0701/31 | | 12 | 60 | |
| | ($R_L$ = 270 Ω, $I_F$ = 12 mA) | | HCPL-0701 | | | 10 | |
| | | | HCPL-0731 | | | 15 | |
| | $T_A$ = 25°C | | HCPL-0701 | | 1.6 | 7 | |
| | | | HCPL-0731 | | 1.6 | 10 | |
| | ($R_L$ = 2.2 kΩ, $I_F$ = 1.6 mA) | | HCPL-0700/30/31 | | | 50 | |
| | $T_A$ = 25°C | | HCPL-0700/30/31 | | 7 | 35 | |
| Common mode transient immunity at logic high | ($I_F$ = 0 mA, $\|V_{CM}\|$ = 10 $V_{P-P}$) $T_A$ = 25°C ($R_L$ = 2.2 kΩ) (Note 3) (Fig. 15) | $\|CM_H\|$ | ALL | 1,000 | 10,000 | | V/µs |
| Common mode transient immunity at logic low | ($I_F$ = 1.6 mA, $\|V_{CM}\|$ = 10 $V_{P-P}$, $R_L$ = 2.2 kΩ) $T_A$ = 25°C (Note 3) (Fig. 15) | $\|CM_L\|$ | ALL | 1,000 | 10,000 | | V/µs |

**NOTES**

1. Current Transfer Ratio is defined as a ratio of output collector current, $I_O$, to the forward LED input current, $I_F$, times 100%.
2. Pin 7 open. Use of a resistor between pins 5 and 7 will decrease gain and delay time.
3. Common mode transient immunity in logic high level is the maximum tolerable (positive) $dV_{CM}/dt$ on the leading edge of the common mode pulse signal, $V_{CM}$, to assure that the output will remain in a logic high state (i.e., $V_O$>2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) $dV_{CM}/dt$ on the trailing edge of the common mode pulse signal, $V_{CM}$, to assure that the output will remain in a logic low state (i.e., $V_O$<0.8 V).
4. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
5. 2500 VAC RMS for 1 minute duration is equivalent to 3000 VAC RMS for 1 second duration.

** All typicals at TA = 25°C

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## TYPICAL PERFORMANCE CURVES

**Fig. 1 Propagation Delay vs. Temperature (HCPL-0700, HCPL-0701)**

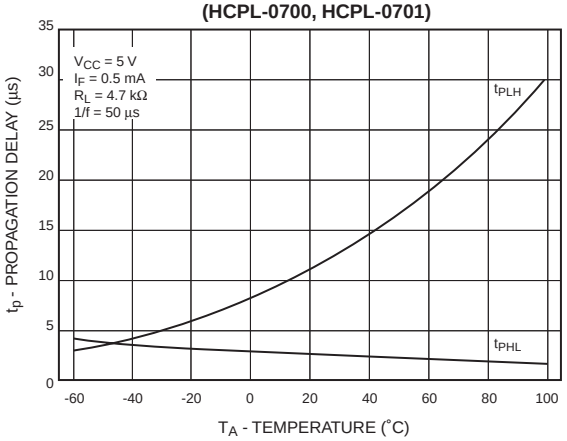



**Fig. 2 Propagation Delay vs. Temperature (HCPL-0700, HCPL-0701)**

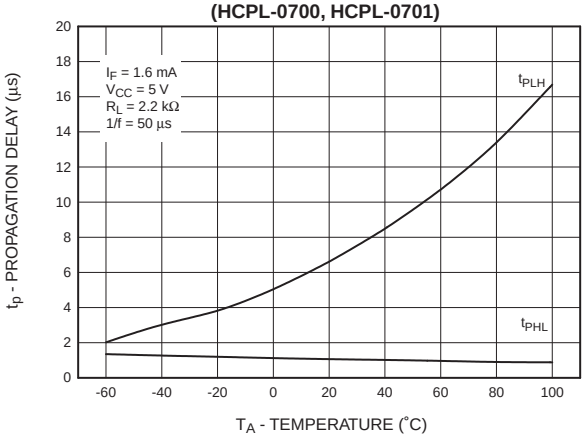



**Fig. 3 Propagation Delay vs. Temperature (HCPL-0700, HCPL-0701)**

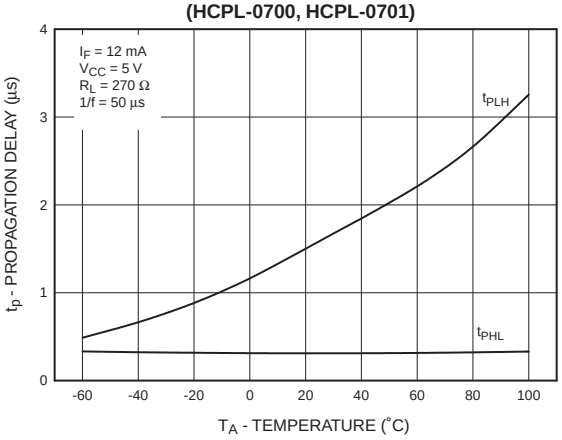



**Fig. 4 Logic High Output Current vs. Temperature (HCPL-0700, HCPL-0701)**

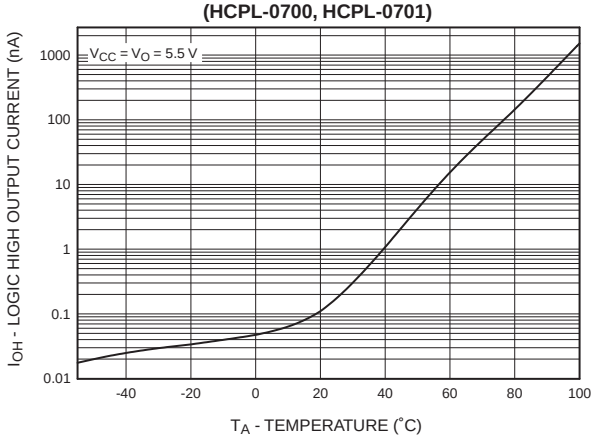



**Fig. 5 Propagation Delay vs. Input Forward Currrent (HCPL-0730, HCPL-0731)**

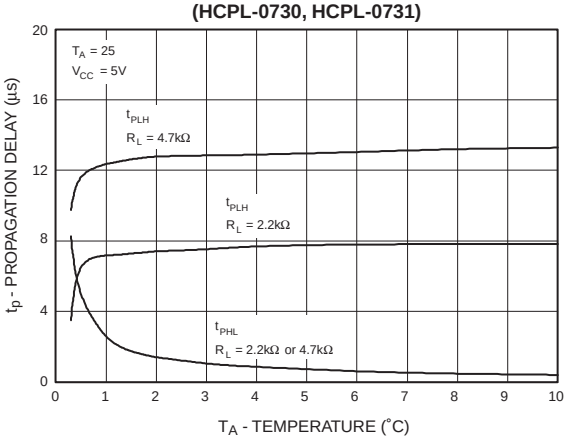
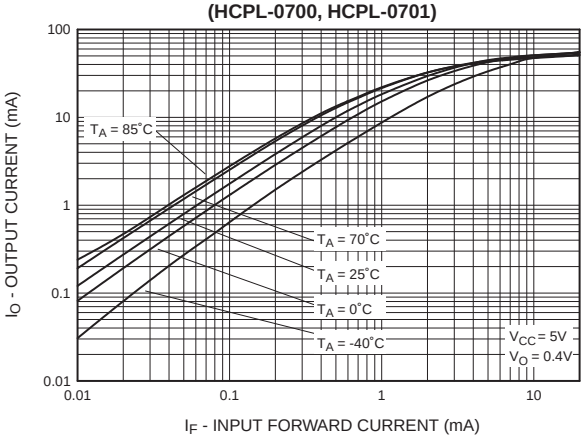



**Fig. 6 Output Current vs. Input Forward Current (HCPL-0700, HCPL-0701)**

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## TYPICAL PERFORMANCE CURVES

**Fig. 7 Input Forward Current vs. Forward Voltage (HCPL-0700, HCPL-0701)**

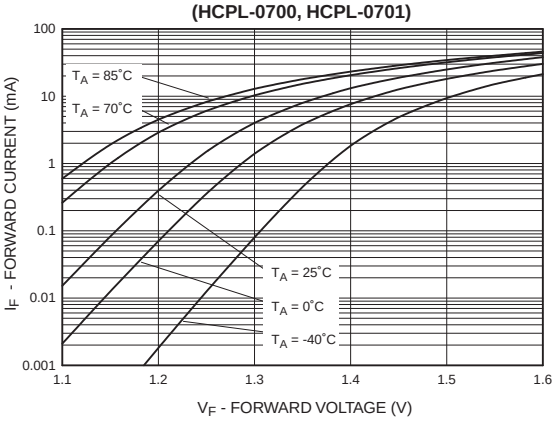



**Fig. 8 Input Forward Current vs. Forward Voltage (HCPL-0730, HCPL-0731)**

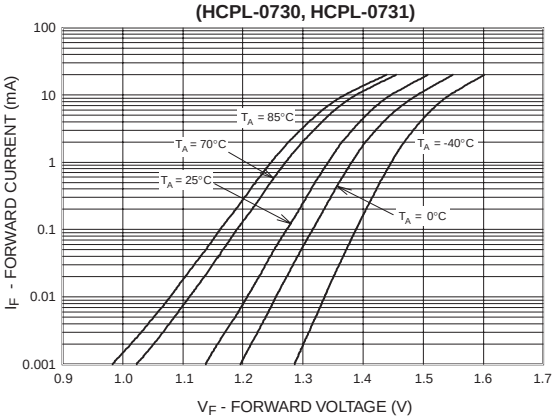



**Fig. 9 Logic Low Supply Current vs. Input Forward Current (HCPL-0700, HCPL-0701)**

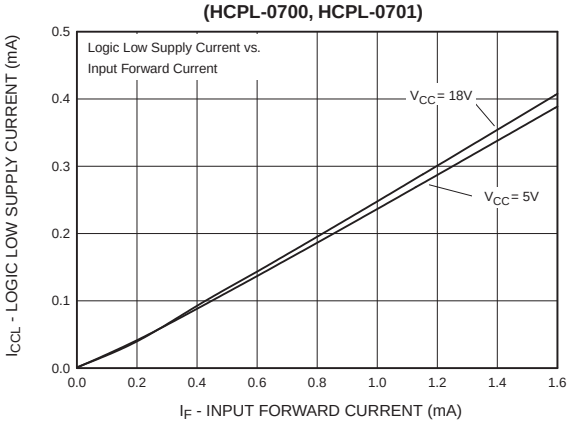



**Fig. 10 Supply Current vs. Input Forward Current (HCPL-0730, HCPL-0731)**

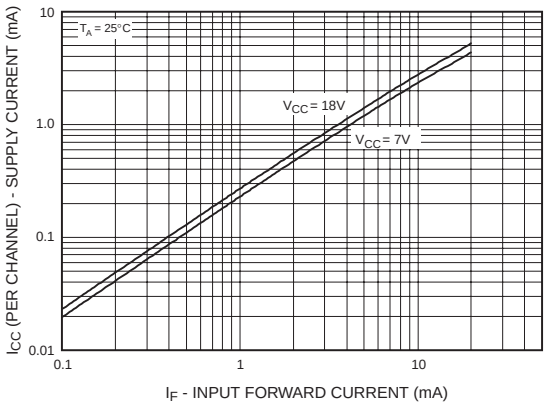



**Fig. 11 DC Transfer Characteristics (HCPL-0700, HCPL-0701)**

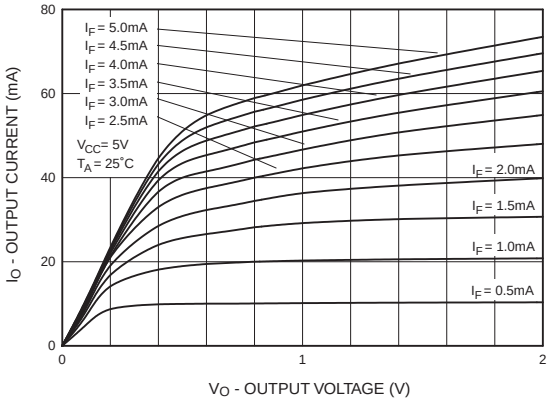
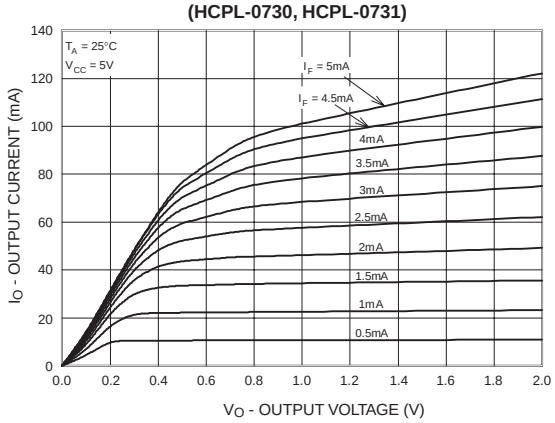
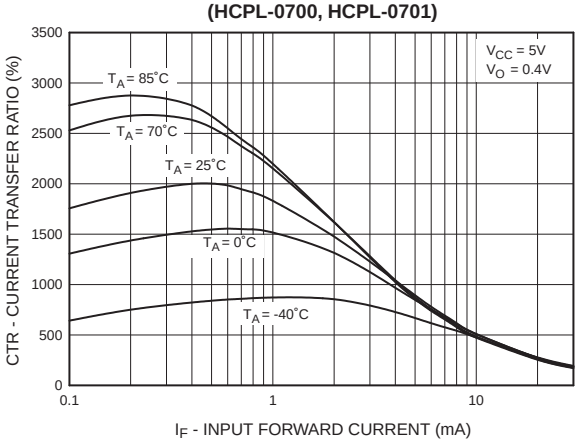


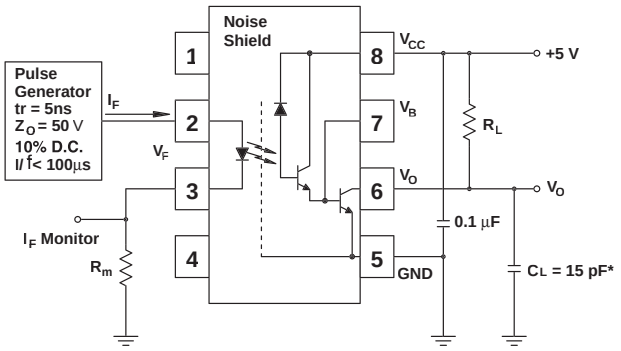

**Fig. 12 DC Transfer Characteristics (HCPL-0730, HCPL-0731)**



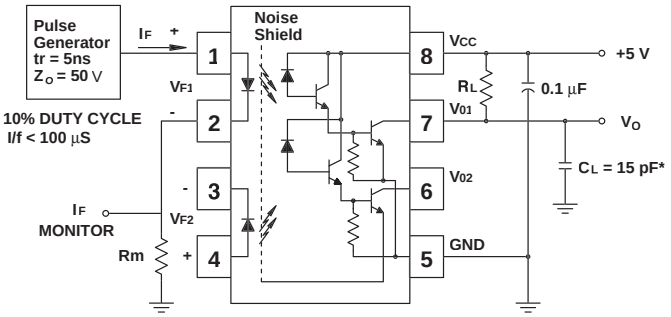
## TYPICAL PERFORMANCE CURVES

**Fig. 13 Current Transfer Ratio vs. Input Forward Current (HCPL-0700, HCPL-0701)**




Test Circuit for HCPL-0700 and HCPL-0701




Test Circuit for HCPL-0730 and HCPL-0731

*Includes probe and fixture capacitance

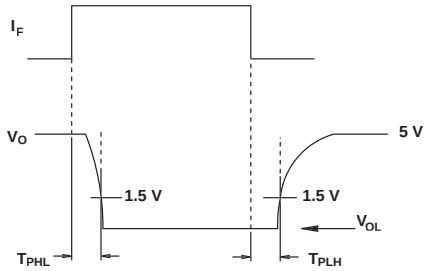
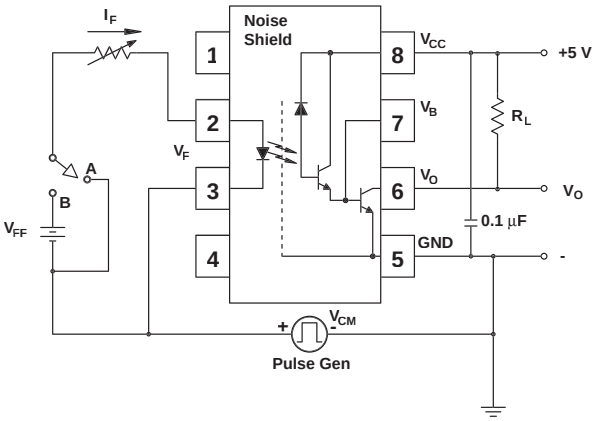
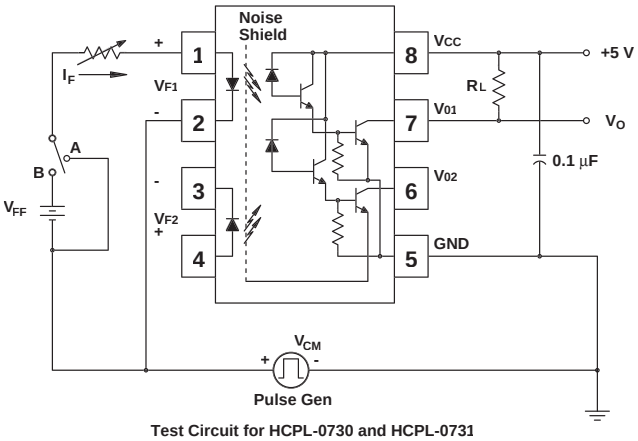



**Fig. 14 Switching Time Test Circuit**




Test Circuit for HCPL-0700 and HCPL-0701




Test Circuit for HCPL-0730 and HCPL-0731

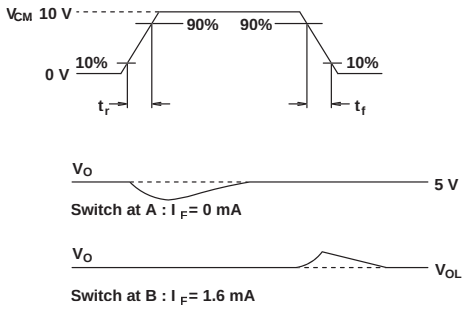
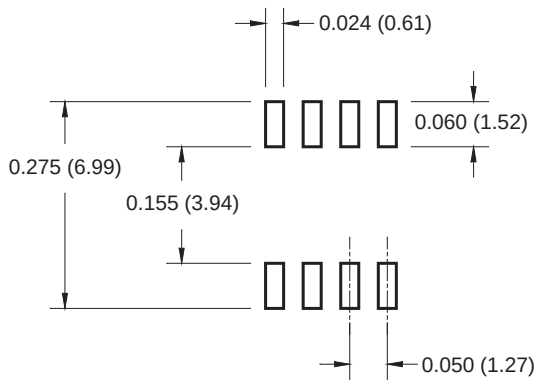



**Fig. 15 Common Mode Immunity Test Circuit**

## 8-Pin Small Outline

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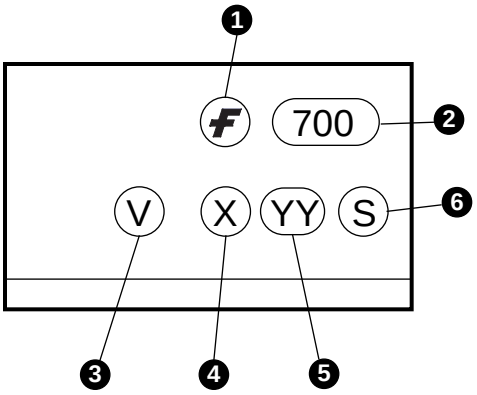
## ORDERING INFORMATION

| Option | Order Entry Identifier | Description |
|---|---|---|
| V | V | VDE 0884 |
| R1 | R1 | Tape and reel (500 units per reel) |
| R1V | R1V | VDE 0884, Tape and reel (500 units per reel) |
| R2 | R2 | Tape and reel (2500 units per reel) |
| R2V | R2V | VDE 0884, Tape and reel (2500 units per reel) |

## MARKING INFORMATION




| Definitions | |
|---|---|
| 1 | Fairchild logo |
| 2 | Device number |
| 3 | VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table) |
| 4 | One digit year code, e.g., ‘3’ |
| 5 | Two digit work week ranging from ‘01’ to ‘53’ |
| 6 | Assembly package code |

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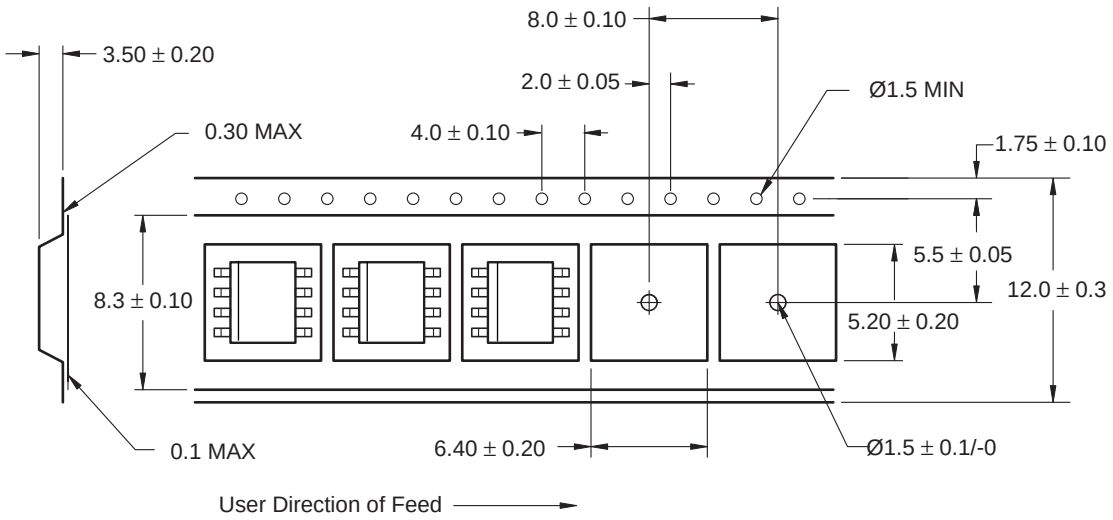
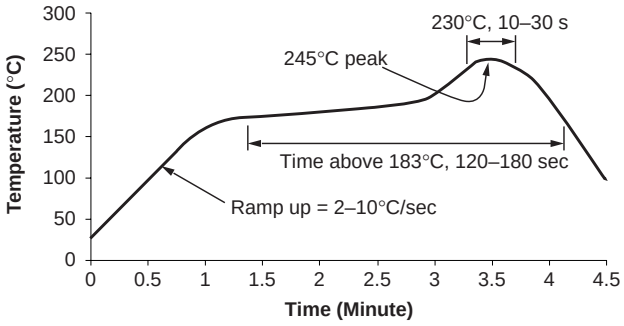
## Carrier Tape Specifications




## Reflow Profile




- Peak reflow temperature: 245°C (package surface temperature)
- Time of temperature higher than 183°C for 120–180 seconds
- One time soldering reflow is recommended

**DISCLAIMER**

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