HEF4050B

Hex non-inverting buffers

Rev. 04 — 2 July 2008 **Product data sheet**

1. General description

The HEF4050B provides six non-inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in Table 3.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input. The HEF4050B is suitable for use over the industrial (–40 °C to +85 °C) and automotive (–40 °C to +125 °C) temperature ranges.

2. Features

- Accepts input voltages in excess of the supply voltage
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the automotive temperature range –40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Applications

- LOCMOS (Local Oxidation CMOS) to DTL/TTL converter
- HIGH sink current for driving two TTL loads
- HIGH-to-LOW level logic conversion

4. Ordering information

Table 1. Ordering information

All types operate from –40 °C to +125 °C.

Type number	Package		
	Name	Description	Version
HEF4050BP	DIP16	plastic dual in-line package; 16-leads (300 mil)	SOT38-4
HEF4050BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

founded by Philips

5. Functional diagram

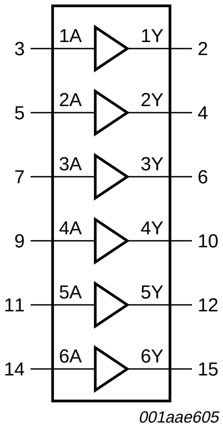


Fig 1. Logic symbol

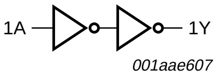


Fig 2. Logic diagram for one gate

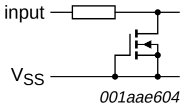


Fig 3. Input protection circuit

6. Pinning information

6.1 Pinning

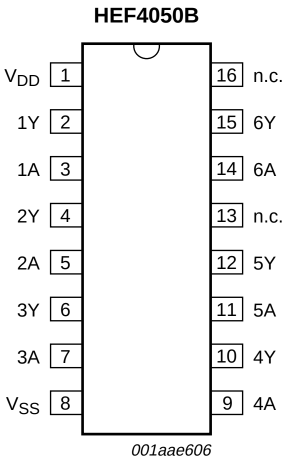


Fig 4. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{DD}	1	supply voltage
1Y to 6Y	2, 4, 6, 10, 12, 15	output

Table 2. Pin description *…continued*

Symbol	Pin	Description
1A to 6A	3, 5, 7, 9, 11, 14,	input
V_{SS}	8	ground supply voltage
n.c.	13, 16	not connected

7. Functional description

Table 3. Guaranteed fan-out

Driven element	Guaranteed fan-out
Standard TTL	2
74 LS	9
74 L	16

8. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+18	V
V_I	input voltage		–0.5	V_{DD} + 0.5	V
$I_{I/O}$	input/output current		-	10	mA
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–40	+125	°C
P_{tot}	total power dissipation	DIP16 package [1]	-	750	mW
		SO16 package [2]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	15	V
V_I	input voltage		0	V_{DD}	V
T_{amb}	ambient temperature	in free air	–40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{DD} = 5 V	-	3.75	ns/V
		V_{DD} = 10 V	-	0.5	ns/V
		V_{DD} = 15 V	-	0.08	ns/V

10. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = −40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		T_{amb} = 125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\| < 1$ μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\| < 1$ μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\| < 1$ μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\| < 1$ μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	−1.7	-	−1.4	-	−1.1	-	−1.1	-	mA
		V_O = 4.6 V	5 V	−0.64	-	−0.5	-	−0.36	-	−0.36	-	mA
		V_O = 9.5 V	10 V	−1.6	-	−1.3	-	−0.9	-	−0.9	-	mA
		V_O = 13.5 V	15 V	−4.2	-	−3.4	-	−2.4	-	−2.4	-	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	4.75 V	3.6	-	2.9	-	2.3	-	1.9	-	mA
		V_O = 0.5 V	10 V	12.5	-	10.0	-	8.0	-	6.7	-	mA
		V_O = 1.5 V	15 V	25.0	-	20.0	-	16.0	-	13.0	-	mA
I_I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I_{DD}	supply current	I_O = 0 A	5 V	-	1.0	-	1.0	-	30	-	30	μA
			10 V	-	2.0	-	2.0	-	60	-	60	μA
			15 V	-	4.0	-	4.0	-	120	-	120	μA
C_I	input capacitance			-	-	-	7.5	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; C_L = 50 pF; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nA to nY; see Figure 5	5 V	[1]	26 ns + (0.18 ns/pF)C_L	-	35	70	ns
			10 V		16 ns + (0.08 ns/pF)C_L	-	20	35	ns
			15 V		12 ns + (0.05 ns/pF)C_L	-	15	30	ns
t_{PLH}	LOW to HIGH propagation delay	nA to nY; see Figure 5	5 V	[1]	28 ns + (0.55 ns/pF)C_L	-	55	110	ns
			10 V		14 ns + (0.23 ns/pF)C_L	-	25	55	ns
			15 V		12 ns + (0.16 ns/pF)C_L	-	20	40	ns

Table 7. Dynamic characteristics *…continued*
V_{SS} = 0 V; C_L = 50 pF; $t_r = t_f \leq$ 20 ns; T_{amb} = 25 °C; unless otherwise specified.

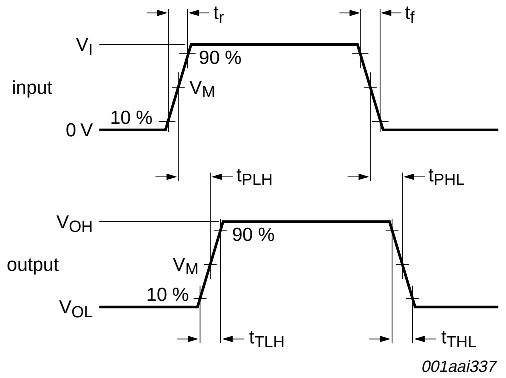
Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula	Min	Typ	Max	Unit
t_{THL}	HIGH to LOW output transition time	see Figure 5	5 V	[1]	7 ns + (0.35 ns/pF)C_L	-	25	50	ns
			10 V		3 ns + (0.14 ns/pF)C_L	-	10	20	ns
			15 V		2 ns + (0.09 ns/pF)C_L	-	7	14	ns
t_{TLH}	LOW to HIGH output transition time	see Figure 5	5 V	[1]	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V		9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V		6 ns + (0.28 ns/pF)C_L	-	20	40	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D
P_D can be calculated from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq$ 20 ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 3800 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz, f_o = output frequency in MHz, C_L = output load capacitance in pF, V_{DD} = supply voltage in V, $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 11600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 65900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

12. Waveforms



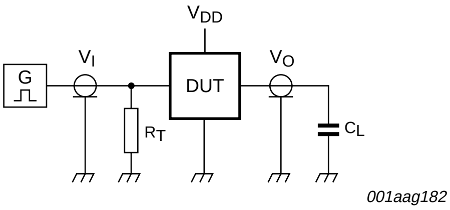
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. Input to output propagation delays

Table 9. Measurement points

Input		Output
V_M	V_I	V_M
$0.5V_{DD}$	0 V to V_{DD}	$0.5V_{DD}$



Test data is given in Table 10.

Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

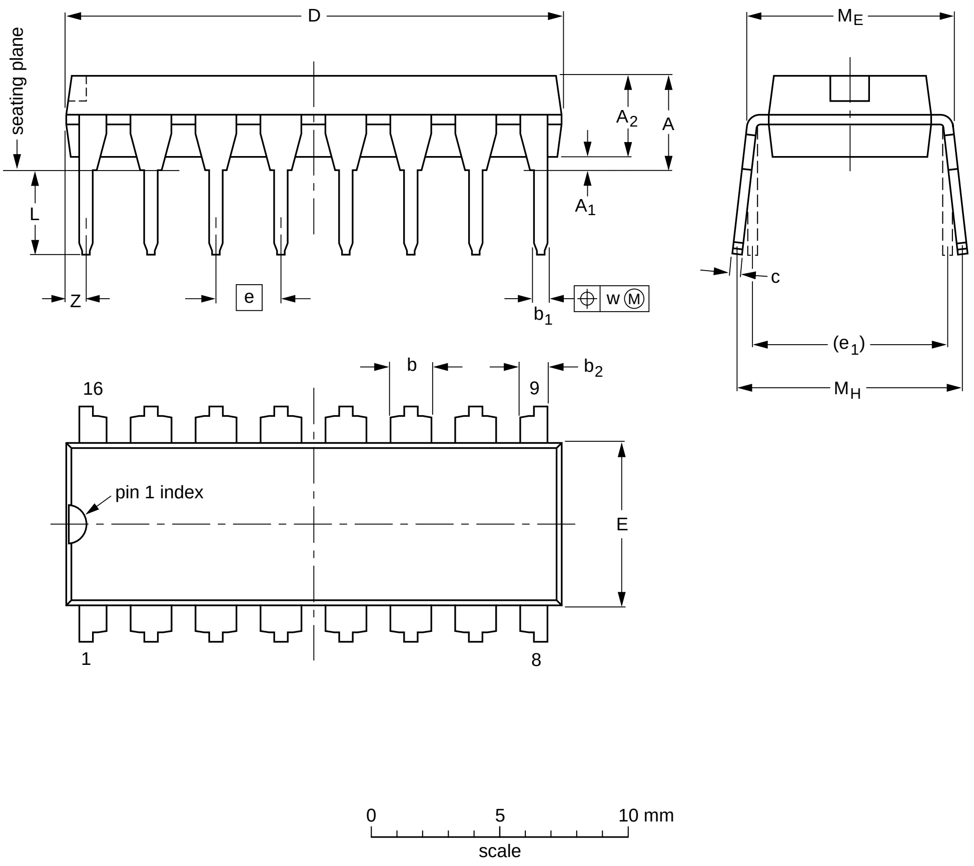
Fig 6. Load circuitry for switching times

Table 10. Test data

Supply voltage	Input			Load
	V_I	V_M	t_r, t_f	C_L
5 V to 15 V	V_{DD}	$0.5V_I$	≤ 20 ns	50 pF

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

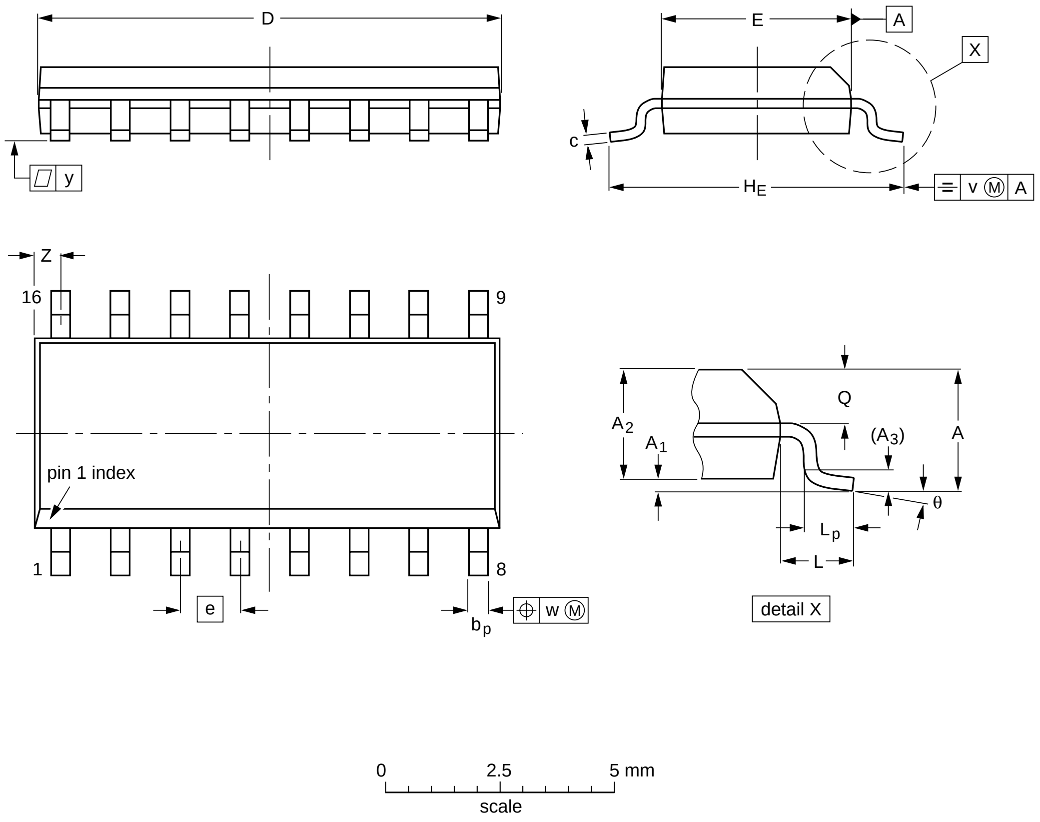
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 7. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

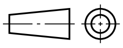
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT109-1 (SO16)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test
DTL	Diode Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
LOCMOS	Local Oxidation CMOS
MM	Machine Model
TTL	Transistor Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4050B_4	20080702	Product data sheet	-	HEF4050B_CNV_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Pins renamed throughout. • Maximum ambient temperature increased to 125 °C. • Section 2 “Features” added. • Package version SOT38-1 changed to SOT38-4 in Section 4, and Figure 7. Package SOT74 removed from Section 4. • Table 1 “Ordering information” restructured. • Section 8 “Limiting values” and Section 10 “Static characteristics” added, taken from the HE4000B Family Specifications data sheet. • Section 10 “Static characteristics” I_{OH}, I_I and I_{DD} values updated. • Section 12 “Waveforms” added. • Section 14 “Abbreviations” added.			
HEF4050B_CNV_3	19950101	Product specification	-	HEF4050B_CNV_2
HEF4050B_CNV_2	19950101	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

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18. Contents

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