

# IRFB11N50APbF

HEXFET® Power MOSFET

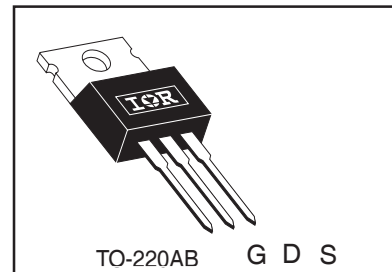
### Applications

- Switch Mode Power Supply ( SMPS )
- Uninterruptable Power Supply
- High speed power switching
- Lead-Free

$V_{DSS}$	$R_{ds(on) \max}$	$I_D$
500V	0.52Ω	11A

### Benefits

- Low Gate Charge  $Q_g$  results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic  $dv/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	11	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	7.0	
$I_{DM}$	Pulsed Drain Current ①	44	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	170	W
	Linear Derating Factor	1.3	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 30	V
$dv/dt$	Peak Diode Recovery $dv/dt$ ②	6.9	V/ns
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

### Applicable Off Line SMPS Topologies:

- Two Transistor Forward
- Half & Full Bridge
- Power Factor Correction Boost

Notes ① through ③ are on page 8

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Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

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	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	500	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.52	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6.6A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 500V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 400V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -30V

## Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	6.1	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 6.6A
Q <sub>g</sub>	Total Gate Charge	—	—	52	nC	I <sub>D</sub> = 11A V <sub>DS</sub> = 400V V <sub>GS</sub> = 10V, See Fig. 6 and 13 ④
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	13		
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	18		
t <sub>d(on)</sub>	Turn-On Delay Time	—	14	—	ns	V <sub>DD</sub> = 250V I <sub>D</sub> = 11A R <sub>G</sub> = 9.1Ω R <sub>D</sub> = 22Ω, See Fig. 10 ④
t <sub>r</sub>	Rise Time	—	35	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	32	—		
t <sub>f</sub>	Fall Time	—	28	—		
C <sub>iss</sub>	Input Capacitance	—	1423	—		
C <sub>oss</sub>	Output Capacitance	—	208	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz, See Fig. 5 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 400V, f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 400V ⑤
C <sub>riss</sub>	Reverse Transfer Capacitance	—	8.1	—		
C <sub>oss</sub>	Output Capacitance	—	2000	—		
C <sub>oss</sub>	Output Capacitance	—	55	—		
C <sub>oss eff.</sub>	Effective Output Capacitance	—	97	—		

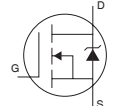
## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy②	—	275	mJ
I <sub>AR</sub>	Avalanche Current①	—	11	A
E <sub>AR</sub>	Repetitive Avalanche Energy①	—	17	mJ

## Thermal Resistance

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	0.75	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat, Greased Surface	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient	—	62	

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	11	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	44		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.5	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 11A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	510	770	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 11A
Q <sub>rr</sub>	Reverse Recovery Charge	—	3.4	5.1	μC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

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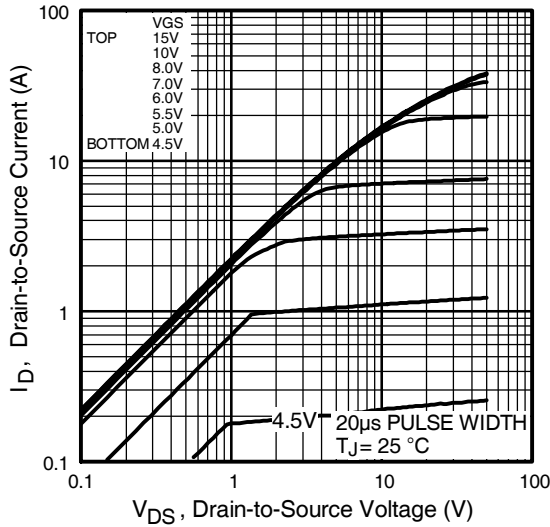


Fig 1. Typical Output Characteristics

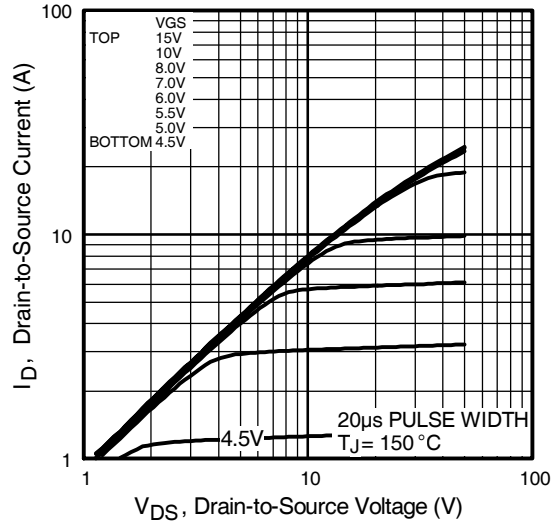


Fig 2. Typical Output Characteristics

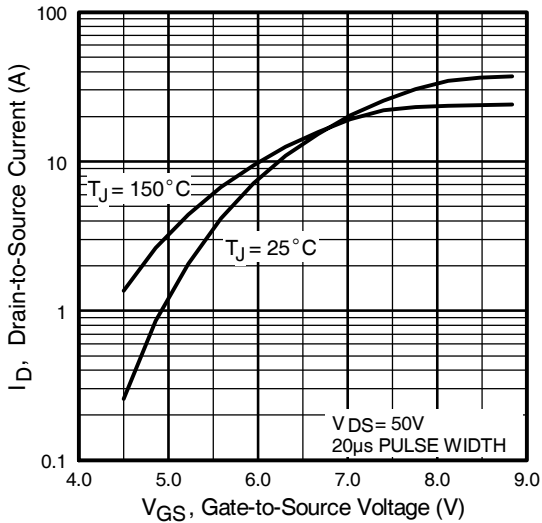


Fig 3. Typical Transfer Characteristics

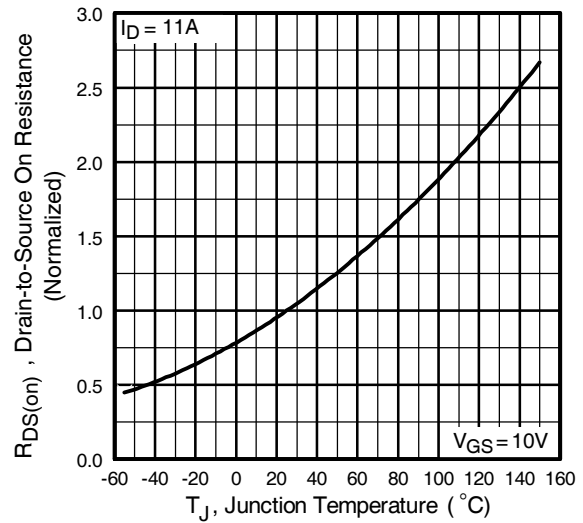
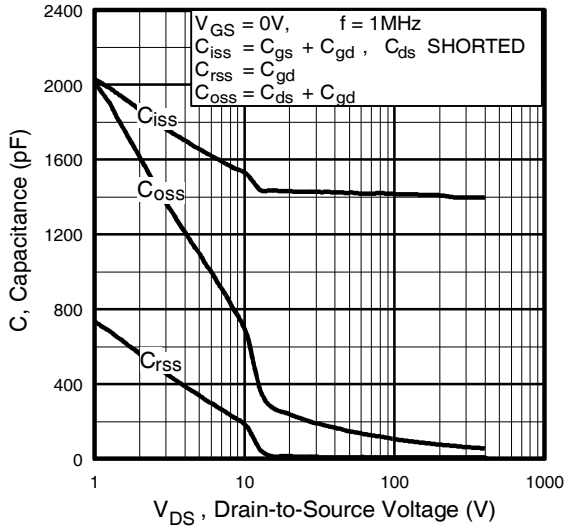
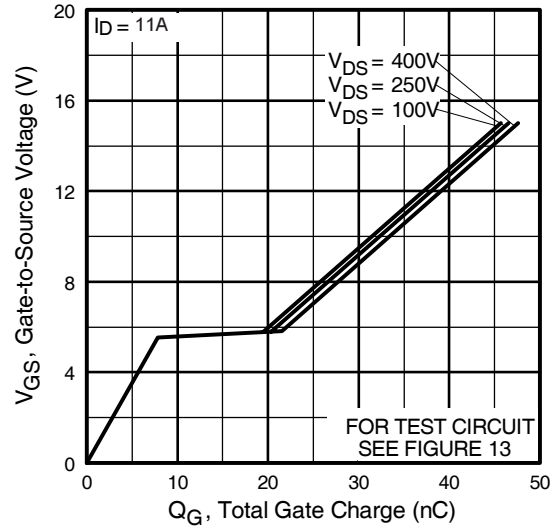


Fig 4. Normalized On-Resistance Vs. Temperature

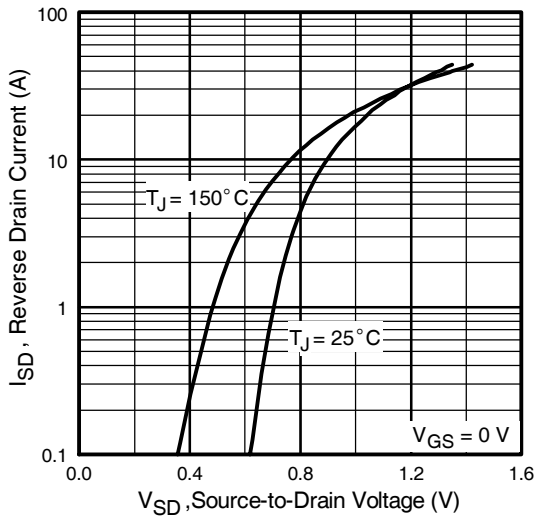
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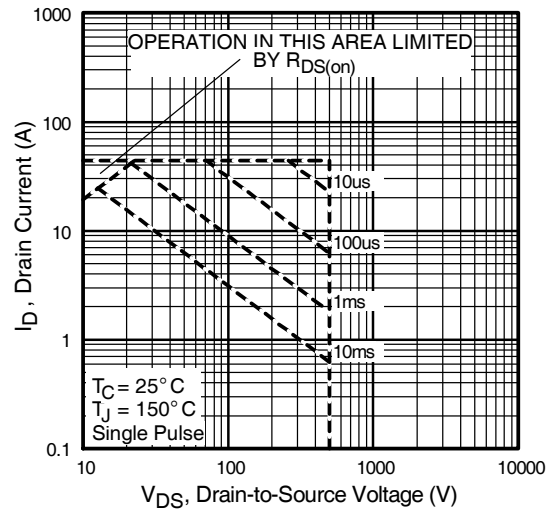
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



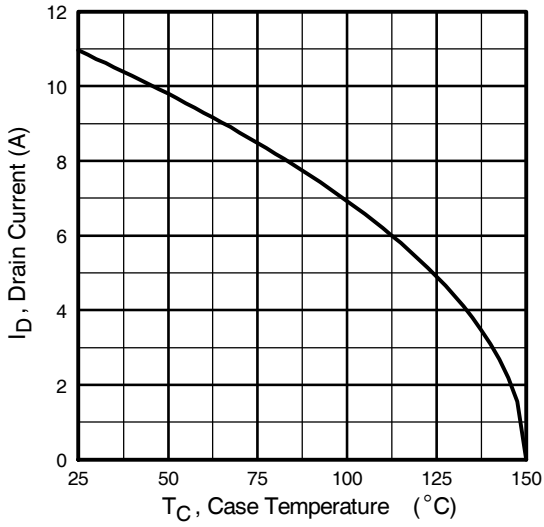
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



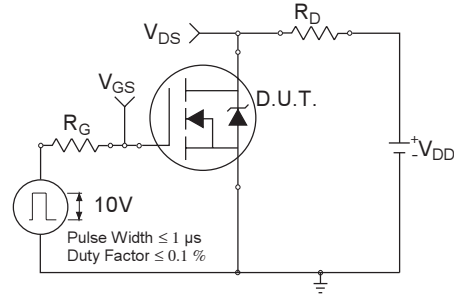
**Fig 7.** Typical Source-Drain Diode Forward Voltage



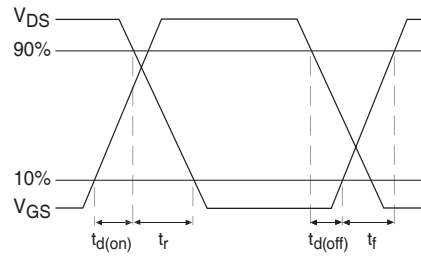
**Fig 8.** Maximum Safe Operating Area



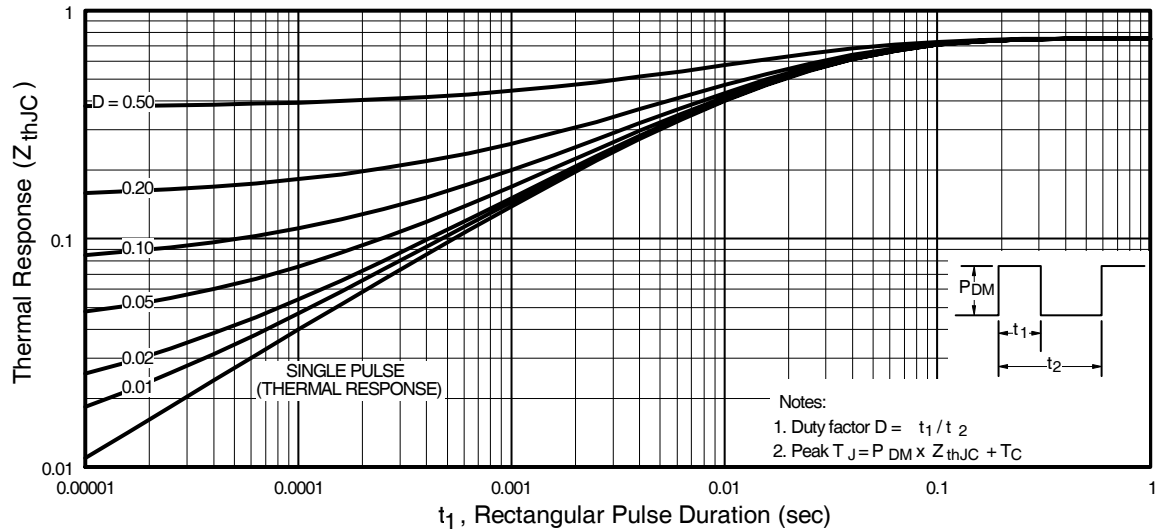
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

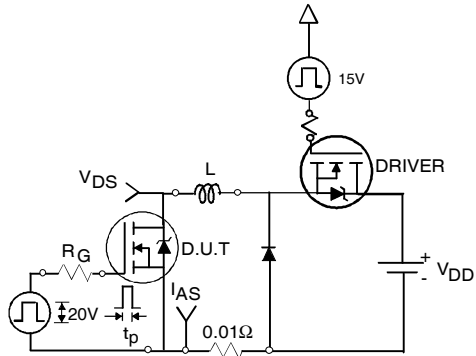


**Fig 10b.** Switching Time Waveforms

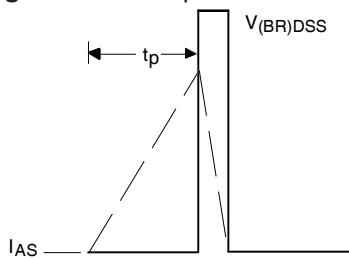


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

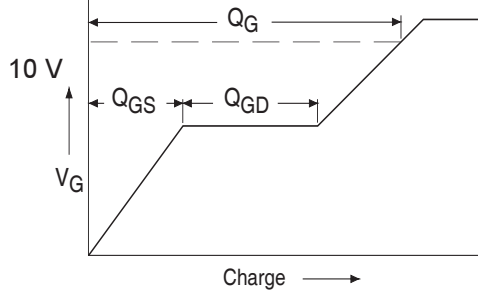
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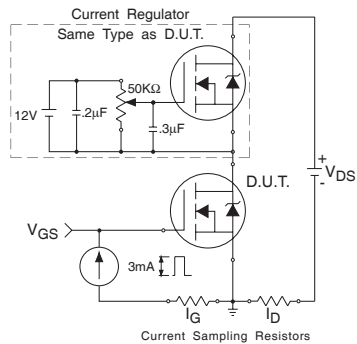
**Fig 12a.** Unclamped Inductive Test Circuit



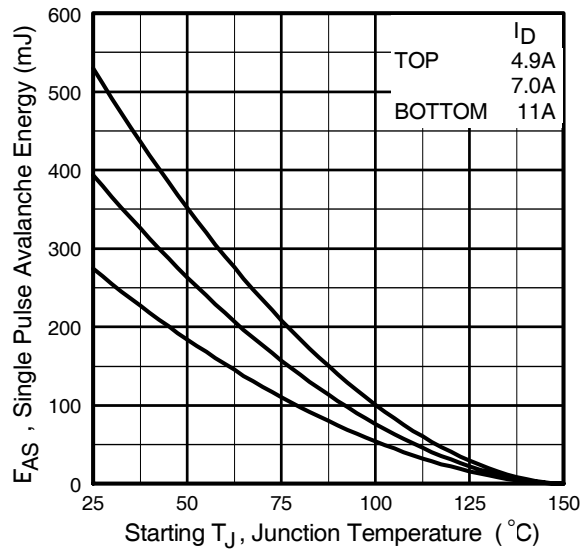
**Fig 12b.** Unclamped Inductive Waveforms



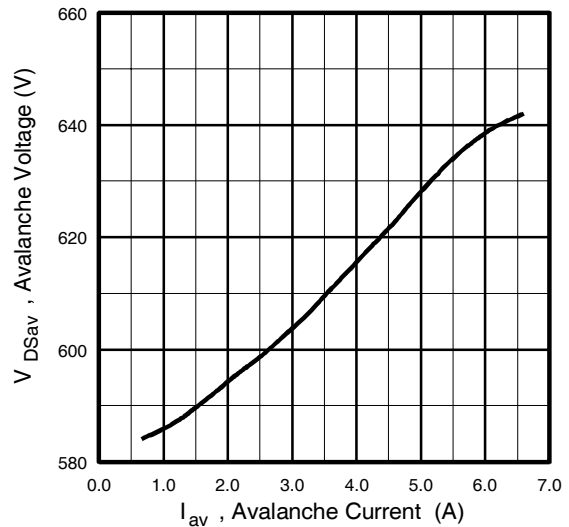
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 12d.** Typical Drain-to-Source Voltage Vs. Avalanche Current

## Peak Diode Recovery dv/dt Test Circuit



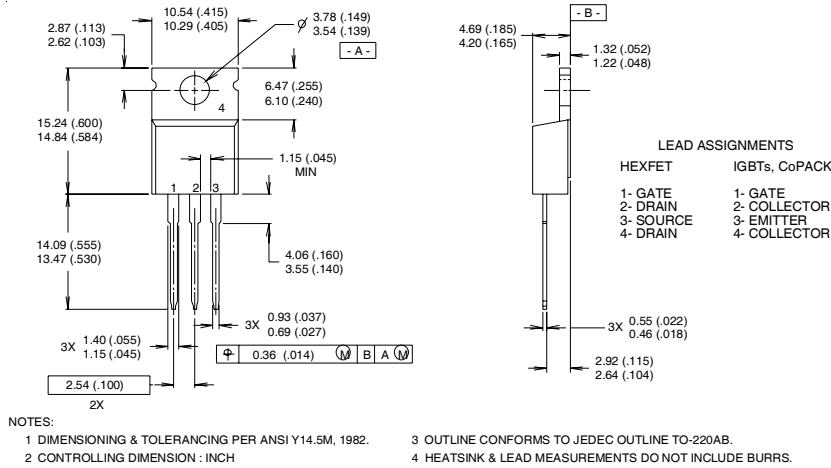
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

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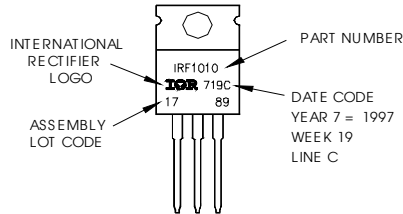
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## TO-220AB Package Outline



## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line position indicates "Lead-Free"



### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 4.5\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 11\text{A}$ . (See Figure 12)
- ③  $I_{SD} \leq 11\text{A}$ ,  $di/dt \leq 140\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$

Data and specifications subject to change without notice.

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