LM3495 Evaluation Board

National Semiconductor
Application Note 1446
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Specifications Of The Board

The Evaluation Board has been designed for testing of various circuits using the LM3495 buck regulator controller. A complete schematic for all the components is shown in Figure 3. The board is four layers, consisting of signal/power traces on top and bottom, one internal ground plane, and an internal split power plane. The top and bottom planes are 1oz. copper, internal planes are ½oz., and the board is 62mil FR4 laminate.

Example Circuit

The example circuit which comes on the evaluation board steps input voltages of 12V ±10% down to 1.2V at currents up to 10A with a switching frequency of 500 kHz. The measured efficiency of the converter is 86% at an output current of 7A.

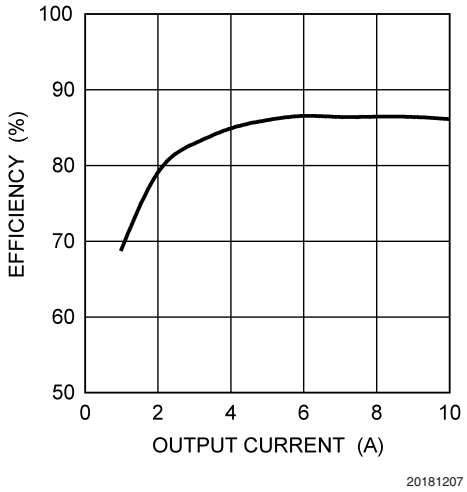


FIGURE 1. Efficiency for V_{IN} = 12V

Powering The Converter

The example circuit for the LM3495 Evaluation Board is optimized to run at inputs of 12V, however the circuit will operate with input voltages ranging from 2.9V to 18.0V connected between the 'Vin' and 'GND' terminals at the top of the board. Fixed loads, resistors, and variable electronic loads can be connected between the 'Vo' and 'GND' terminals. The Bill of Materials table lists all the components used in the example circuit.

Enabling The Converter

The SPDT switch **ON/OFF** controls the state of the converter while power is applied to the input terminals. While in the OFF position the COMP/SD* pin of the LM3495 is grounded, the output is disabled, and the IC enters a low power state. While in the ON position the output voltage is regulated and is capable of delivering current to a load connected at the output terminals.

Testing The Converter

Figure 4 shows a block diagram of connections for making measurements of efficiency. The wires used for making connections at both the input and output should be rated to at least 10A of continuous current and should be no longer than is needed for convenient testing. A series ammeter capable of measuring 10A or more should be used for both the input and the output lines. Dedicated voltmeters should be connected with their positive and negative leads right at the four power terminals at the top of the evaluation board. This measurement technique minimizes the voltage loss in the wires that connect the evaluation board to the input power supply and the electronic load.

Output voltage ripple measurements should be taken directly across the 100 nF ceramic capacitor **Cox**, placed right between the output terminals. Care must be taken to minimize the loop area between the oscilloscope probe tip and the ground lead. One method to minimize this loop is to remove the probe's spring tip and 'pigtail' ground lead and then wind bare wire around the probe shaft. The bare wire should contact the ground of the probe, and the end of the wire can then contact the ground side of **Cox**. Figure 5 shows a diagram of this method.

An oscilloscope probe modified as described above can also be used to measure the switch node voltage, LG pin voltage, and HG pin voltage (all three with respect to ground) using the 40mil diameter hole pairs labeled "+ SW −", "+ LG −", and "+ HG −", respectively.

SKIP/PWM

A second SPDT switch labeled SKIP/FPWM determines which control scheme the LM3495 uses at low output currents. When set to SKIP, the converter saves energy during light loads (approximately 100 mA or less) by using the body diode of the low side FET, as well as leaving the high side FET off if possible. When the switch is set to FPWM, the LM3495 forces both top and bottom FETs to switch during every cycle, regardless of the load current.

MOSFET Footprints

The LM3495 evaluation board has footprints for single N-MOSFETs with SO-8 packages and standard pinouts. These footprints can also accept newer MOSFET packages that are compatible with SO-8 footprints. See *Figure 2*. **Q1** is the high side FET, and **Q2** low side FET.

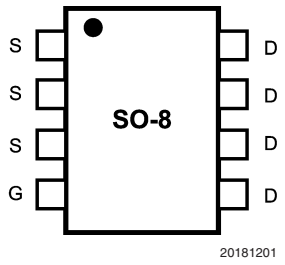


FIGURE 2. SO-8 MOSFET Pinout

Permanent Components

The following components should remain the same for any new circuits evaluated on the LM3495 evaluation board:

Name	Value
Cb	0.1 µF
Cf	1 µF
Cdd	2.2 µF

Additional Footprints

A 100 pF ceramic capacitor should be placed at position **Dsync** whenever the LM3495 runs without an external clock. When an external clock is used, **Dsync** should be removed and a 100 pF ceramic capacitor placed at **Csync**.

The 0Ω resistor **J1** connects the TRACK pin and VDD pins of the LM3495 together. It should be removed only when the tracking function is used.

The 0Ω resistor **J2** connects the VIN and VLIN5 terminals of the LM3495 together. This resistor should be used only when the input voltage is 5.5V or less, to provide maximum MOSFET gate drive.

The 0Ω resistor **J3** connects the 'Vin' terminal to the VIN pin of the LM3495. This resistor should be removed only for testing of the input current draw of the LM3495 IC.

The 0Ω resistor **Rbst** can be replaced with a higher value resistor to limit the current drawn by the BOOST pin. This slows the high-side FET gate drive rise time and may reduce ringing on the switch node. Care must be taken, as slowing the gate drive too much can cause shoot-through current.

Components **Rt1** and **Rt2** are used if the output of the converter is tracking another supply during startup. For this application the output of the external supply should be connected to the TRACK IN terminal. When the tracking feature is not used, the track pin should be connected to the VDD pin by placing a 0Ω resistor in position **J2**.

Components **Rsnb** and **Csnb** can be used to filter ringing on the switch node.

D2 provides a position for a diode to go in parallel with **Q2**. In circuits with output currents of approximately 5A or less, a Schottky diode at **D2** can improve the efficiency of the converter.

Complete Circuit Schematic

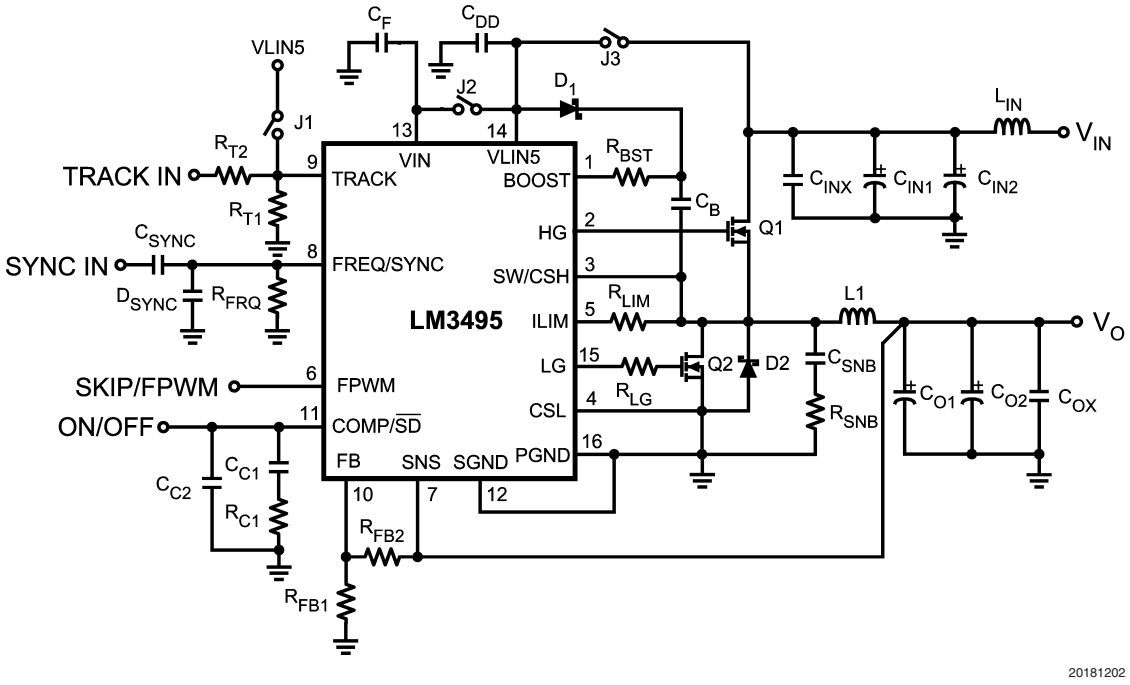


FIGURE 3. Circuit Schematic

Connection Diagrams

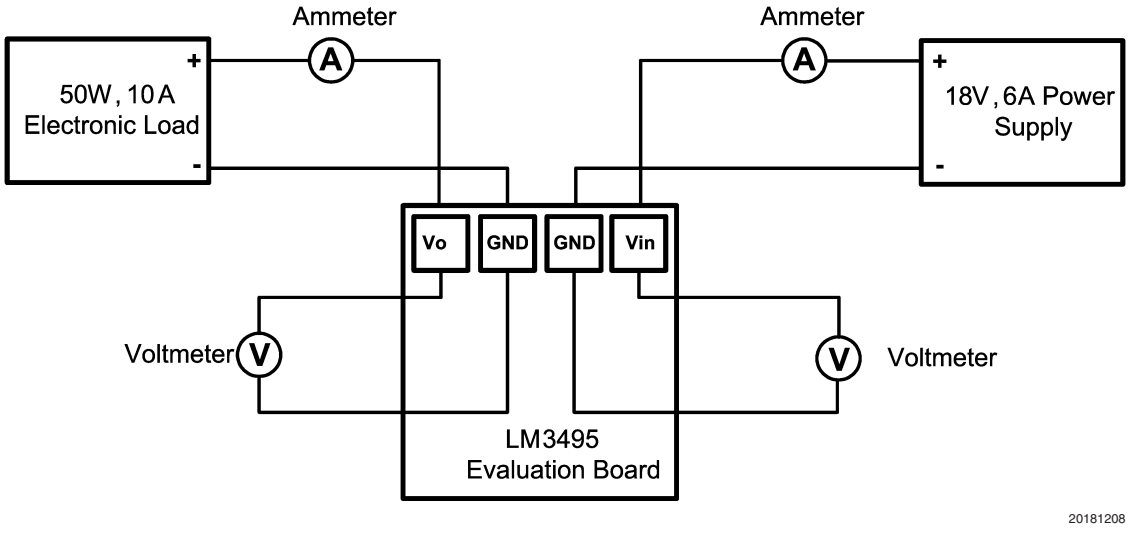


FIGURE 4. Efficiency Measurement Setup

Connection Diagrams (Continued)

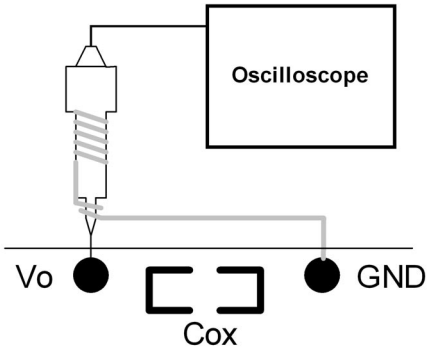


FIGURE 5. Output Voltage Ripple Measurement Setup

Typical Performance Waveforms

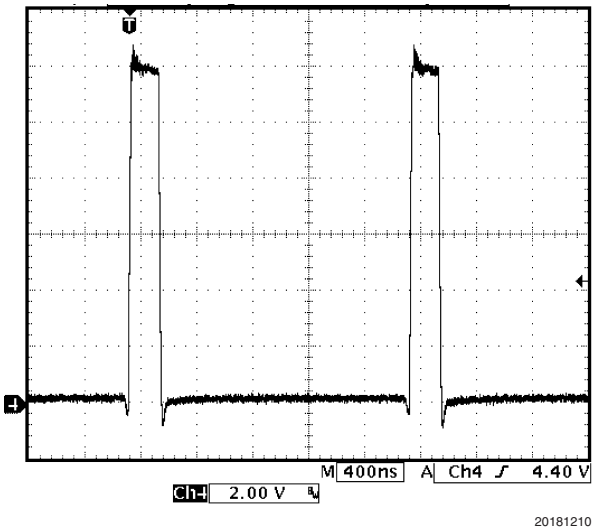


FIGURE 6. Switch Node Voltage (V_{IN} = 12V, V_O = 1.2V, I_O = 5A)

Typical Performance Waveforms (Continued)

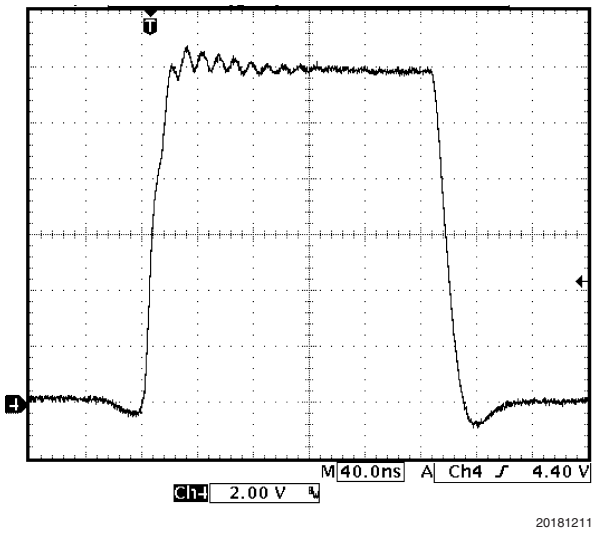


FIGURE 7. Switch Node Voltage (V_{IN} = 12V, V_O = 1.2V, I_O = 5A)

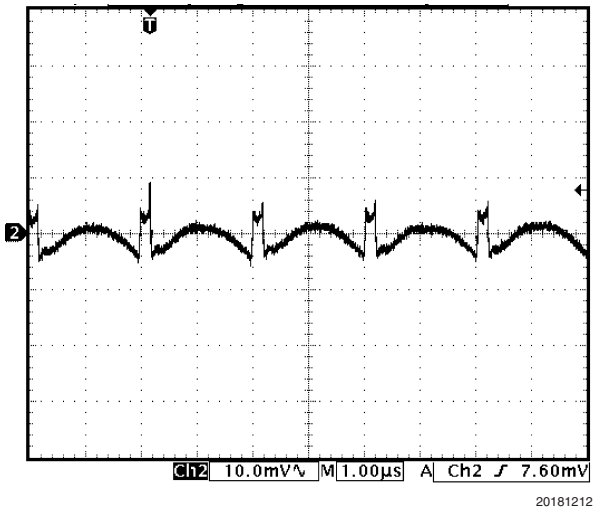


FIGURE 8. Output Voltage Ripple, AC Coupled (V_{IN} = 12V, V_O = 1.2V, I_O = 5A)

Typical Performance Waveforms (Continued)

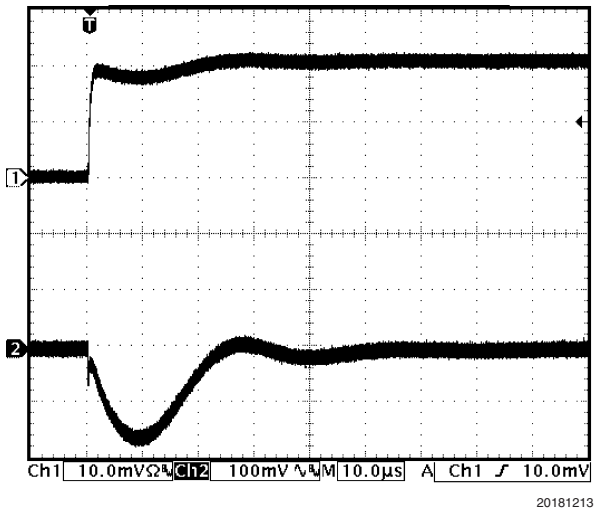


FIGURE 9. Load Transient Response (V_{IN} = 12V, V_O = 1.2V, I_O = 0A to 4A)

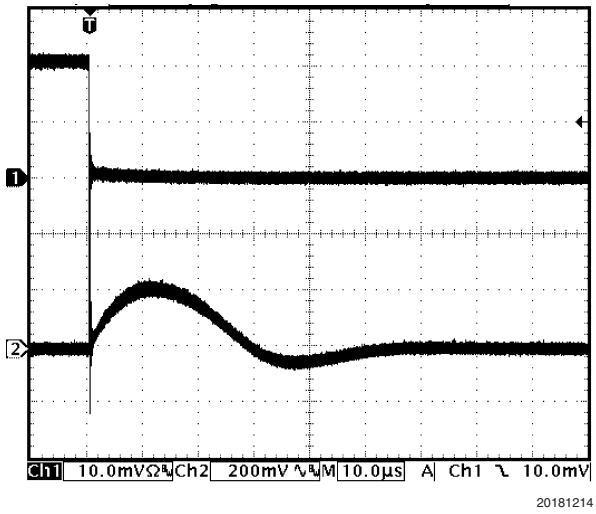
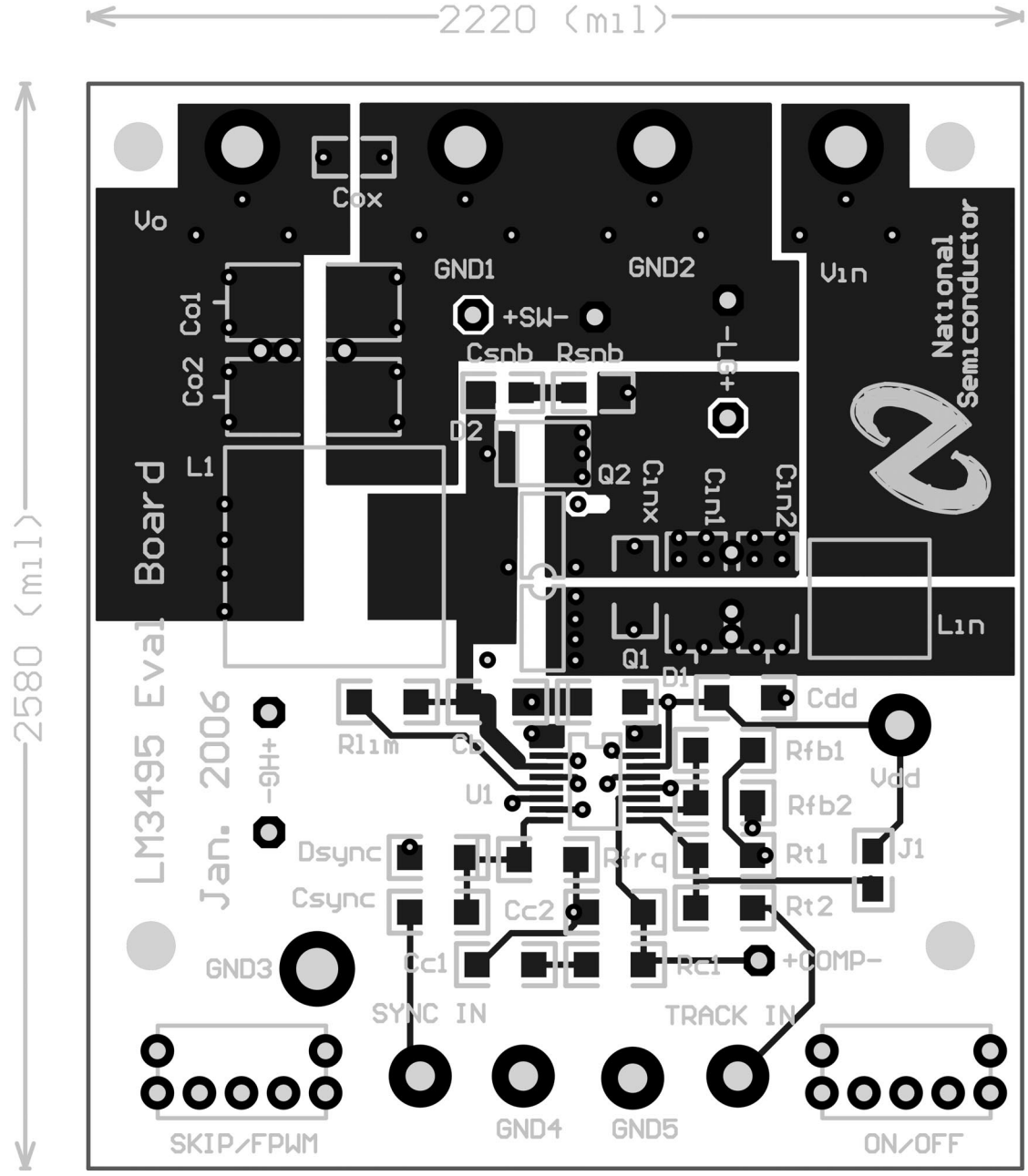


FIGURE 10. Load Transient Response (V_{IN} = 12V, V_O = 1.2V, I_O = 4A to 0A)

Bill of Materials

ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LM3495	Synchronous Controller	TSSOP-16		1	NSC
Q1	HAT2198R	N-MOSFET	SO-8	30V, 9.6mΩ 11nC	1	Renesas
Q2	HAT2165H	N-MOSFET	LFPAK	30V 3.4mΩ, 33nC	1	Renesas
D1	MBR0530	Schottky Diode	SMA	30V, 0.5A	1	Vishay
L1	RLF12560T-1R0N140	Inductor	12.5x12.8 x6.0mm	1µH 14A 3mΩ	1	TDK
Cin	C3225X5R1E226M	Capacitor	1210	22µF, 25V	1	TDK
Co1, Co2	C3225X5R0J107M	Capacitor	1210	100µF 6.3V 1mΩ	2	TDK
Cf	C3216X7R1E105M	Capacitor	1206	1µF, 25V	1	TDK
Cdd	C3216X7R1E225M	Capacitor	1206	2.2µF 25V	1	TDK
Cb, Cinx	VJ1206Y104KXXAT	Capacitor	1206	100nF 10%	2	Vishay
Cc1	VJ1206Y103KXXAT	Capacitor	1206	10nF 10%	1	Vishay
Cc2, Csync, Dsync	VJ1206A101KXXAT	Capacitor	1206	100pF 10%	3	Vishay
Cox	VJ0805Y104KXXAT	Capacitor	805	100nF 10%	1	Vishay
Rbst, J1, J3	CRCW08050R00F	Resistor	805	0Ω	3	Vishay
Lin	CRCW25120R00F	Resistor	2512	0Ω	1	Vishay
Rc1	CRCW12061501F	Resistor	1206	1.5kΩ 1%	1	Vishay
Rfb1, Rfb2	CRCW12061002F	Resistor	1206	10kΩ 1%	2	Vishay
Rfrq	CRCW12065492F	Resistor	1206	54.9kΩ 1%	1	Vishay
Rlg	CRCW12061R00F	Resistor	1206	1Ω 1%	1	Vishay
Rlim	CRCW12063321F	Resistor	1206	3.32kΩ 1%	1	Vishay
SKIP/FPWM ON/OFF	NKK A12AB	SPST			2	NKK
Vo, GND1 GND2, GND3 Vin	Newark 40F6004	Terminal Silver	0.094”		5	Cambion
SYNC IN GND4, GND5 TRACK IN	Newark 94F1478	Terminal Silver	0.062”		4	Keystone

PCB Layout



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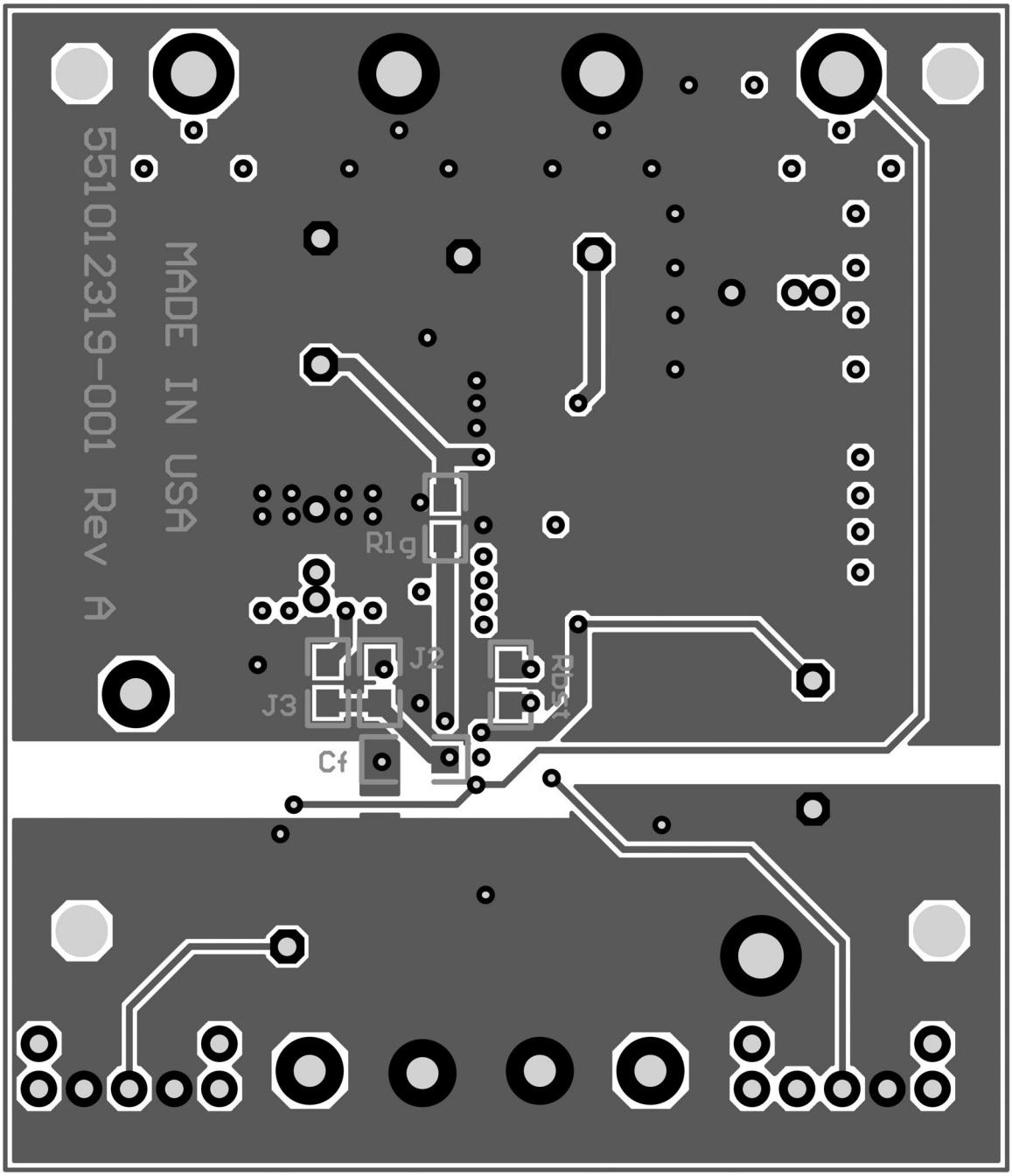
Top Layer and Top Overlay

PCB Layout (Continued)



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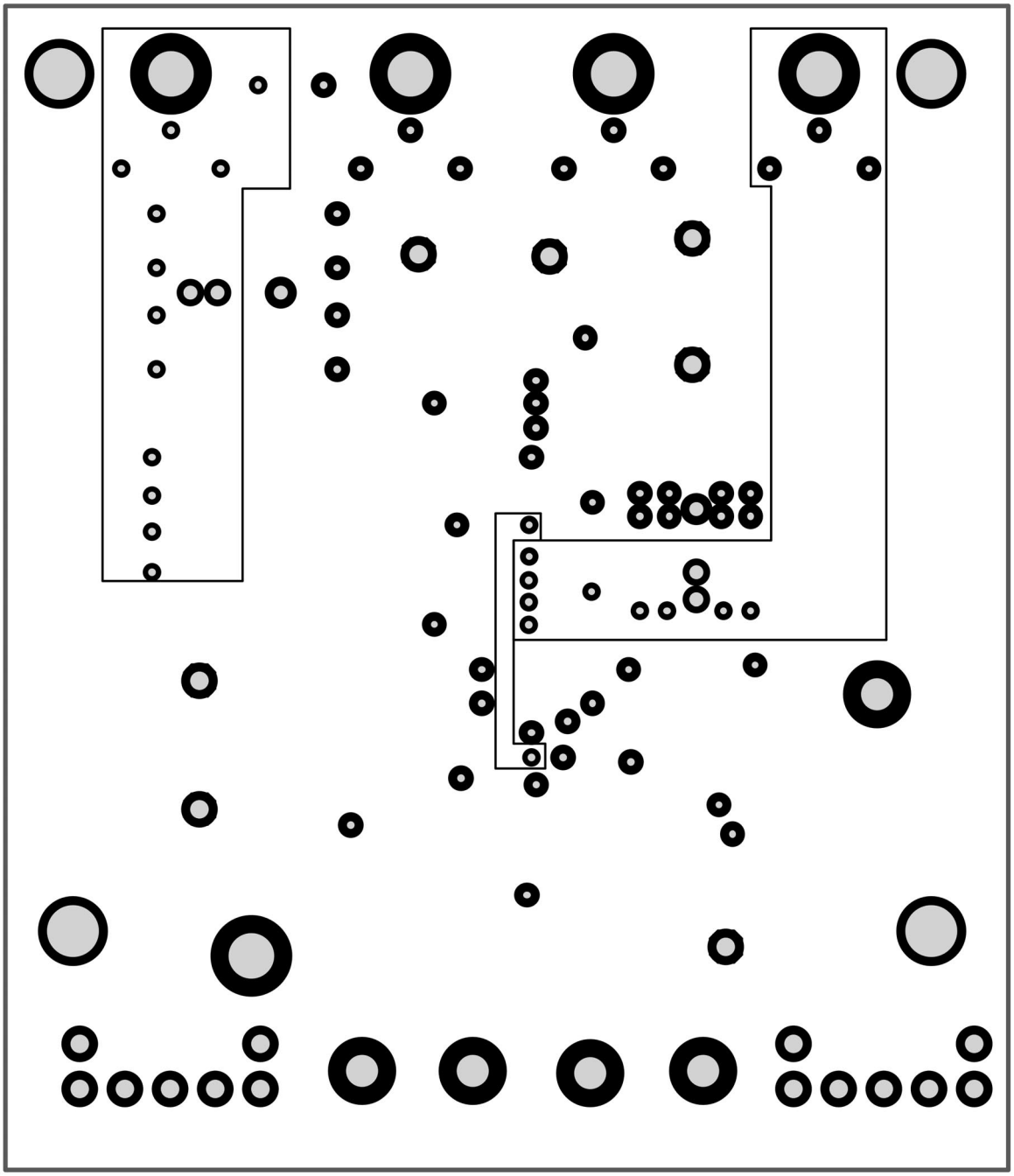
Bottom Layer

PCB Layout (Continued)



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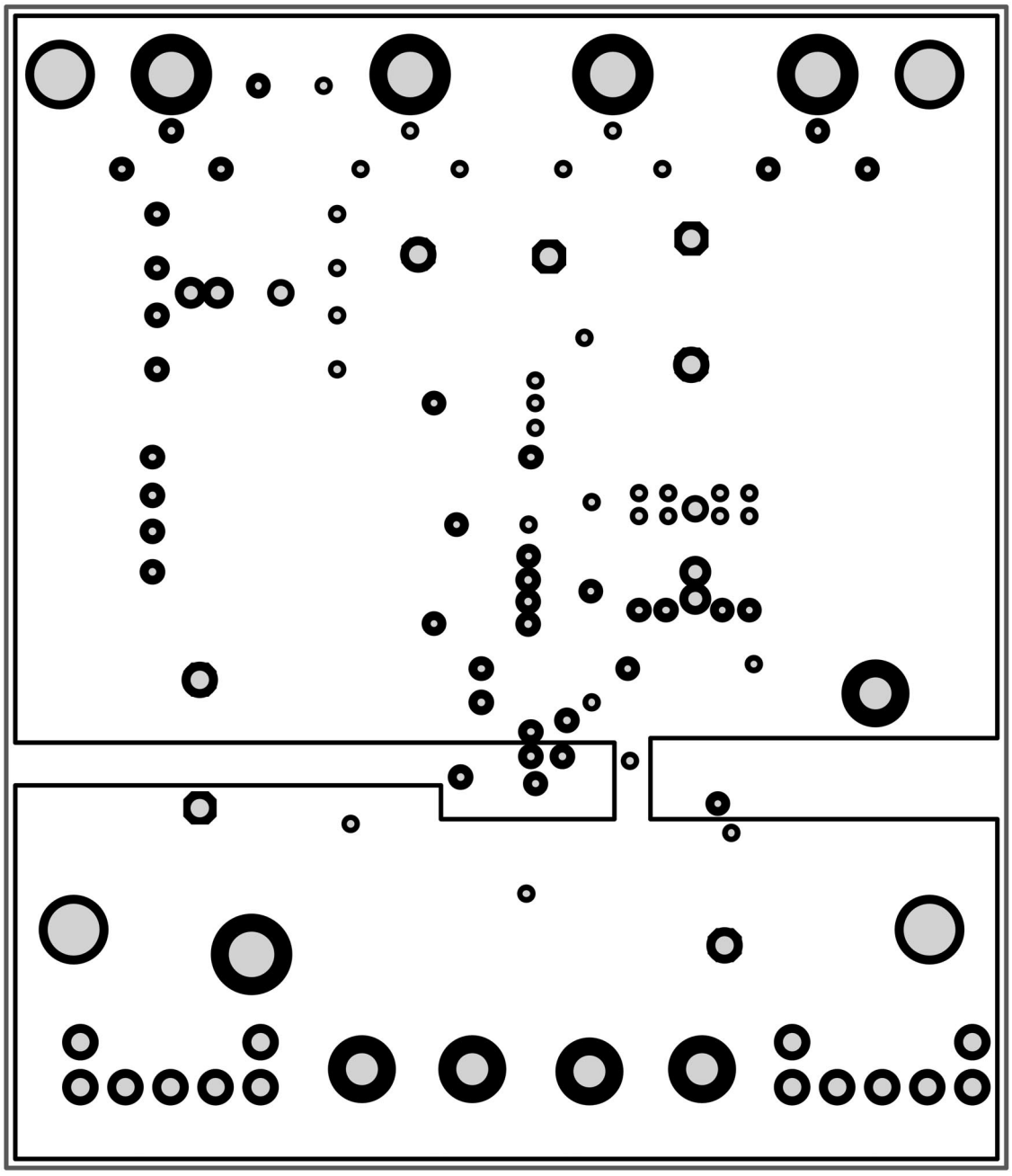
Internal Layer 1

PCB Layout (Continued)



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Internal Layer 2

Notes

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