M52352FP

NTSC/QUASI PAL TRANSCODER

DESCRIPTION

The M52352FP is a semiconductor integrated circuit that efficiently converts NTSC signals to quasi PAL signals for VCR equipment. Circuit configuration includes built-in horizontal AFC, burst gate pulse generator, adjustable gain amplifier, 4-input / 1-output analog switch, and analog for selecting 1H and 2H comb. For PAL system VCR playback, the M52352FP converts NTSC chroma signals to quasi PAL chroma signals enabling reproduction of color from NTSC system soft tape on PAL system televisions.

FEATURES

- Equipped with "through mode" for amplifying output to 6 dB when mounted with PAL soft tape.
- Burst gate pulse position and width can be set according to external constant; burst gate pulse output capability.
- Freerun adjustment mode enables adjustment of VCO freerun for horizontal AFC. (Doesn't require sync input.)
- Switching signals are produced via horizontal AFC to realize stable conversion to quasi PAL signals.

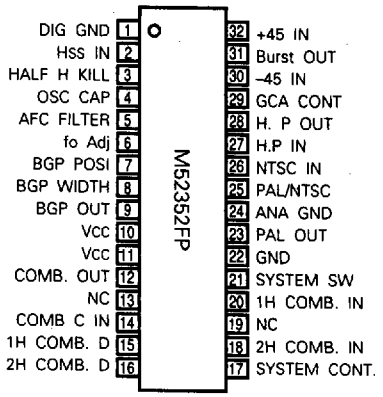
APPLICATION

VCR

RECOMMENDED OPERATING CONDITION

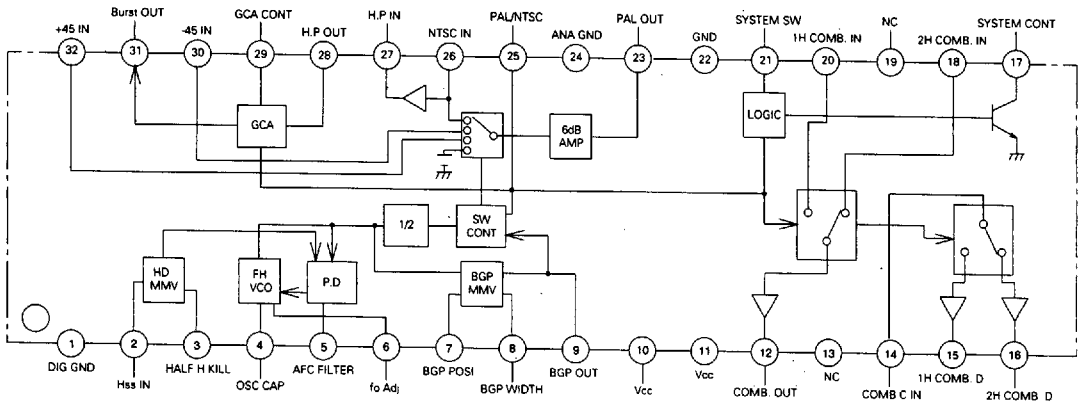
Operating Supply Voltage .....4.5~5.5V
Recommended Supply Voltage 5.0V

PIN CONFIGURATION (TOP VIEW)



Outline 32P2U-B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6	V
P_d	Power dissipation	900	mW
T_{opr}	Operating temperature	−20~75	°C
T_{stg}	Storage temperature	−40~125	°C
K_θ	Thermal derating (Ta≧25°C)	9	mW/°C
S_{urge}	Electrostatic discharge (C=200pF)	±200V or more	V

ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc=12.0V, unless otherwise noted)

Symbol	Parameter	Test conditions (S10=ON, S5=1, S27=S29=OFF, V21=5V, V25=0V unless specified otherwise.)	Limits			Unit
			Min.	Typ.	Max.	
Icc	Circuit Current	No input (S10 = OFF) Test input current of pins ⑩ and ⑪.	24	31	39	mA
G26–23	Through Mode Gain	Input SG1 into pin ㉖. (V25 = 5V) Test V_{P-P} of pin ㉓ and input the ratio. $G(26\text{-}23)=20LOG\frac{\text{Output Level}}{\text{Input Level}}$	4.5	5.5	6.5	dB
G30–23	−45° Gain	Input SG1 into pin ㉚, test V_{P-P} of pin ㉓ and take ratio with input. $G(30\text{-}23)=20LOG\frac{\text{Output Level}}{\text{Input Level}}$	4.0	5.0	6.0	dB
G32–23	+45° Gain	Input SG1 into pin ㉜, test V_{P-P} of pin ㉓ and take ratio with input. $G(32\text{-}23)=20LOG\frac{\text{Output Level}}{\text{Input Level}}$	4.0	5.0	6.0	dB
ΔG45	Gain Difference of (+45°) and (−45°)	|G(30-23)-G(32-23)|	—	0.0	0.5	dB
G26–27	H. P. Drive Gain	Input SG1 into pin ㉖, test V_{P-P} of pin ㉗ and take ratio with input. $G(26\text{-}27)=20LOG\frac{\text{Output Level}}{\text{Input Level}}$	−0.9	−0.2	0.5	dB
VCO SW	VCO Mode Switch	Input SG2 into pin ②. (S27 = ON) Gradually decrease V27 from 5V and test V27 when the frequency of the pin ⑦ waveform is the same as that of SG2.	3.2	3.7	4.0	V
G28–31 MAX	GCA Maximum Gain	Input SG1 into pin ㉘. (S29 = ON, V29 = 5V) Test V_{P-P} of pin ㉛ and take ratio with input. $20LOG\frac{\text{Output Level}}{\text{Input Level}}$	6.0	7.0	8.0	dB
G28–31 OPEN	GCA Open Gain	Input SG1 into pin ㉘. (S29 = OFF) Test V_{P-P} of pin ㉛ and take ratio with input. $20LOG\frac{\text{Output Level}}{\text{Input Level}}$	2.9	4.4	5.9	dB
G28–31 MIN	GCA Minimum Gain	Input SG1 into pin ㉘. (S29 = ON, V29 = 0V) Test V_{P-P} of pin ㉛ and take ratio with input. $20LOG\frac{\text{Output Level}}{\text{Input Level}}$	−7.0	−5.0	−3.0	dB
PAL1	Artificial PAL-1	Input SG3-1 into pin ㉖ and pin ㉚, and input SG3-2 into pin ②. Make sure output waveform of pin ㉓ is normal.	—	—	—	—
PAL2	Artificial PAL-1	Input SG3-1 into pin ㉖ and pin ㉜, and input SG3-2 into pin ②. Make sure output waveform of pin ㉓ is normal.	—	—	—	—
TH	GCA Off (During "Through")	Input SG1 into pin ㉘. (V25 = 5V) Make sure no signal is output from pin ㉛.	—	—	—	—
RT	Discharge Reset Time	Input SG2 into pin ② and test the discharge reset time of pin ③.	33	38	43	μs

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test conditions (S10=ON, S5=1, S27=S29=OFF, V21=5V, V25=0V unless specified otherwise.)	Limits			Unit
			Min.	Typ.	Max.	
HHK	Half H Killer	Input SG4 into pin ②. (S5 = 2) Gradually increase the frequency of SG4 and test the maximum frequency when the waveform frequency of pin ⑤ is the same as that of SG4. (HHK = 1/f)	33	38	43	μs
H. DP	H. D POSI	Input SG2 into pin ②. (S5 = 2) Test the time difference between rise of fH and rise of the pin ⑤ waveform.	0	0.2	0.5	μs
H. DW	H. D WIDTH	Input SG2 into pin ②. (S5 = 2) Test the pulse width of pin ⑤ waveform.	4.0	4.5	5.0	μs
HSSH	Input Sync Detector Peak Value	Input SG5 into pin ② and gradually increase the peak value of SG5. Test the peak value of SG5 when the frequency of the pin ⑦ waveform is same as that of SG5.	3.6	—	5.0	V
β	VCO β	No input. (S5 = 3, S27 = ON, V27 = 5V) Change voltage of V5 from 3V to 4V and test the frequency change of pin ⑦ output. Make β the maximum slope.	6	9	12	Hz/mV
CLW	Capture Range Amplitude	Input SG2 into pin ②. Adjust unsynchronized frequency and test the frequency when pin ⑦ waveform is locked.	2.0	2.6	—	kHz
RLW	Lock Range Amplitude	Input SG2 into pin ②. Alter frequency by increasing or decreasing and test the frequency when pin ⑦ waveform is not locked.	3.0	3.7	—	kHz
P/N–1	Artificial PAL/Normal Switching Voltage-1 (Pin 25 Threshold Voltage)	Input SG3-1 into pin ㉕, and input SG3-2 into pin ②. Gradually decrease the voltage of V25 from 5V and test the voltage when chroma of pin ㉓ output disappears for each 1 H.	2.0	2.3	2.6	V
P/N–2	Artificial PAL/Normal Switching Voltage-2 (Pin 25 Threshold Voltage, H~M)	Input SG3-1 into pin ㉕, and input SG3-2 into pin ②. Gradually increase the voltage of V21 from 0V and test the voltage when chroma of pin ㉓ output disappears for each 1 H.	3.0	3.3	3.6	V
BGPP	BGP POSI	Input SG2 into pin ②. Test the time difference between rise of fH and rise of the pin ⑨ waveform.	3.4	4.0	4.6	μs
BGPW	BGP WIDTH	Input SG2 into pin ②. Test the pulse width of pin ⑨ waveform.	5.4	6.0	6.6	μs
BGPH	BGP Output HI Voltage	Input SG2 into pin ②. Test the pulse width of pin ⑨ waveform.	3.6	4.0	—	V
BGPL	BGP Output LO Voltage	Input SG2 into pin ②. Test the pulse width of pin ⑨ waveform.	—	0	0.5	V
HSST	Input Sync Detector Rise Time	Input SG8 into pin ② and gradually increase the rise time. HSST is the rise time just before the charge/discharge waveform of pin ③ ceases.	—	—	1.5	μs
G14–15	1H COMB. D Gain	Input SG6 into pin ⑭. Test V_{P-P} of pin ⑮ and take ratio with input. $G(14\text{-}15)=20\text{LOG}\frac{\text{Output Level}}{\text{Input Level}}$	–0.9	–0.2	0.5	dB
G14–16	2H COMB. D Gain	Input SG6 into pin ⑭. (V25 = 5V) Test V_{P-P} of pin ⑯ and take ratio with input. $G(14\text{-}16)=20\text{LOG}\frac{\text{Output Level}}{\text{Input Level}}$	–0.9	–0.2	0.5	dB
ΔG14	1H COMB. D, 2H COMB. D Gain Difference	|G (14-15)-G (14-16)|	—	0.0	0.5	dB
G20–12	1H COMB. IN Gain	Input SG7 into pin ⑳. Test V_{P-P} of pin ⑫ and take ratio with input. $G(20\text{-}12)=20\text{LOG}\frac{\text{Output Level}}{\text{Input Level}}$	–0.9	–0.2	0.5	dB
G18–12	2H COMB. IN Gain	Input SG7 into pin ⑱. (V25 = 5V) Test V_{P-P} of pin ⑫ and take ratio with input. $G(18\text{-}12)=20\text{LOG}\frac{\text{Output Level}}{\text{Input Level}}$	–0.9	–0.2	0.5	dB

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test conditions (S10=ON, S5=1, S27=S29=OFF, V21=5V, V25=0V unless specified otherwise.)	Limits			Unit
			Min.	Typ.	Max.	
ΔG12	COMB. OUT Gain Difference	IG (20-12)-G (18-12)I	—	0.0	0.5	dB
S. SW	System Switch (Pin 21 Threshold Voltage, L ~ M)	Input SG1 into pin ㉘. Gradually increase V21 from 0V and test V21 voltage when voltage of pin ⑰ drops from H to L.	0.6	1.0	1.4	V
VCCR	Operating Supply Voltage Range	There must be no abnormality in standard application circuit during operation.	4.5	5.0	5.5	V

SW Conditions for Pins ㉑ and ㉕

Pin ㉓ OUT

21 \ 25	H	L
H	Through	Convert
M	Through	Through
L	Through	Through

Pin ⑰ OUT

21 \ 25	H	L
H	L	L
M	L	L
L	L	H

Convert: Artificial PAL Signal Conversion

Conditions of Pins ⑮ or ⑯ Being Output from Pin ⑭ Input

21 \ 25	H	L
H	Pin 16	Pin 15
M	Pin 16	Pin 15
L	Pin 16	Pin 15

Conditions of Pin ⑫ Being Output from Pins ⑱ and ⑳ Input

21 \ 25	H	L
H	Pin 18	Pin 20
M	Pin 18	Pin 20
L	Pin 18	Pin 20

METHOD OF ADJUSTING VR6 BEFORE TESTING

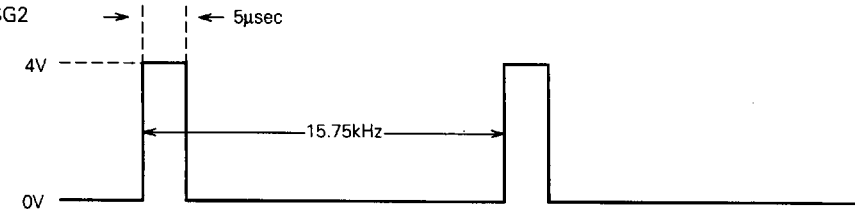
1. Freerun Frequency Adjustment
   Set S27 to ON and V27 to 5V (freerun mode) of circuit to be tested. Adjust VR6 so that the frequency of pin ⑦ waveform is 15.75kHz.
   (Adjust VR6 so that freerun during actual operation is the desired f_H.)

INPUT SIGNAL

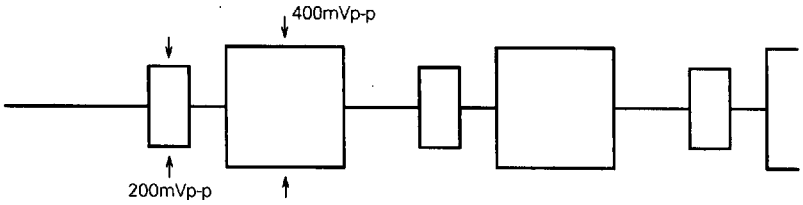
S G		Signals (50Ω termination)	
1		f=4.43MHz	0.5Vp-p CW
2		f=15.75KHz	Pulse Waveform
3	1	f=4.43MHz	Chroma Signal
	2	f=15.75KHz	Pulse
4		f=15.75KHz	Pulse Waveform (Variable Frequency)
5		f=15.75KHz	Pulse Waveform (Variable Peak Value)
6		f=4.43MHz	0.8Vp-p CW
7		f=4.43MHz	0.25Vp-p CW
8		f=15.75kHz	Pulse Waveform

INPUT SIGNAL WAVEFORM

1. SG2

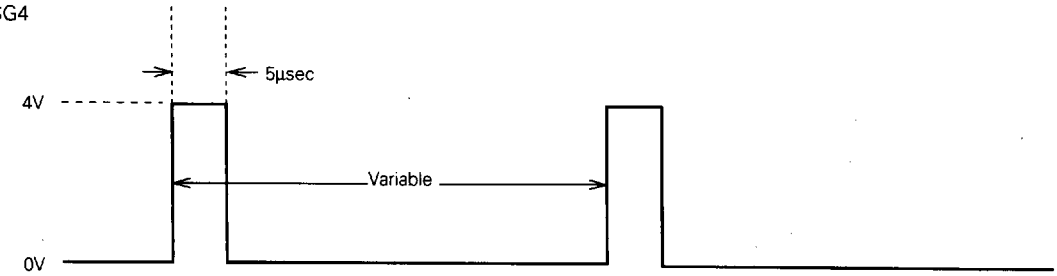


2. SG3-1

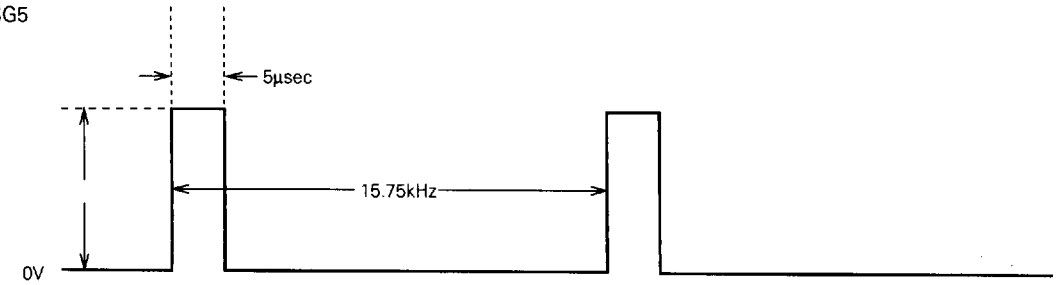


SG3-2

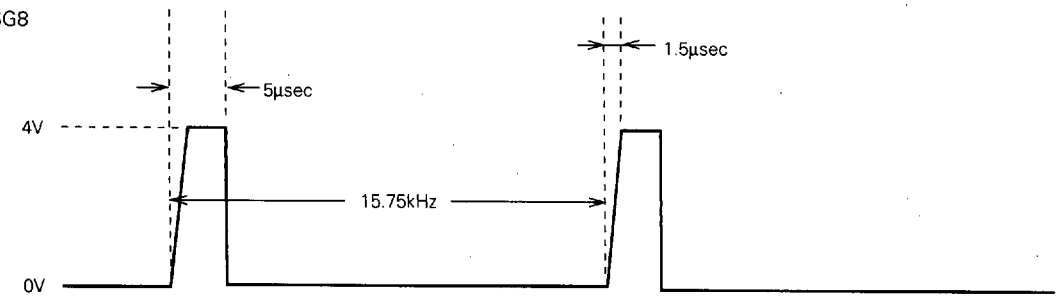
3. SG4



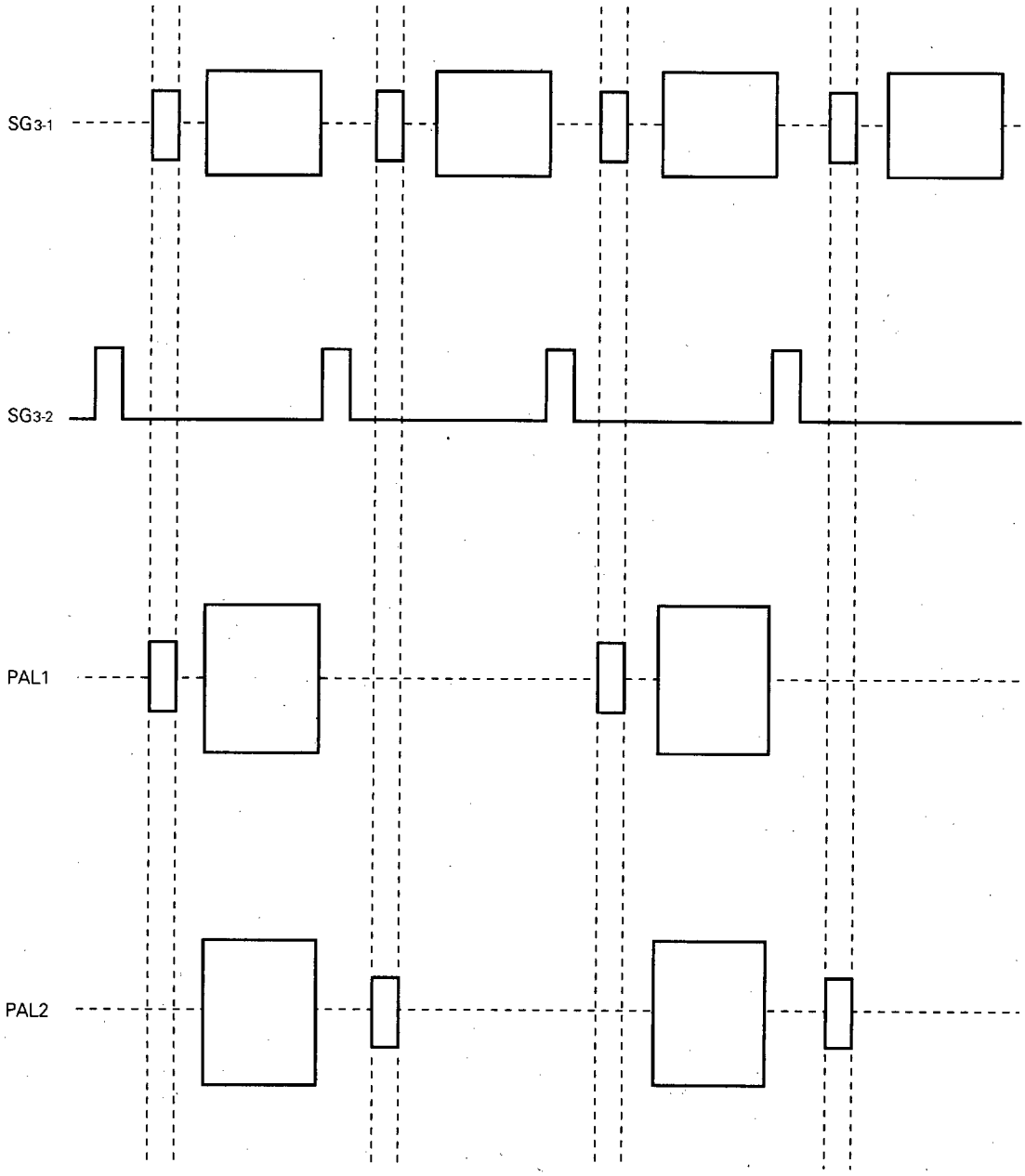
4. SG5



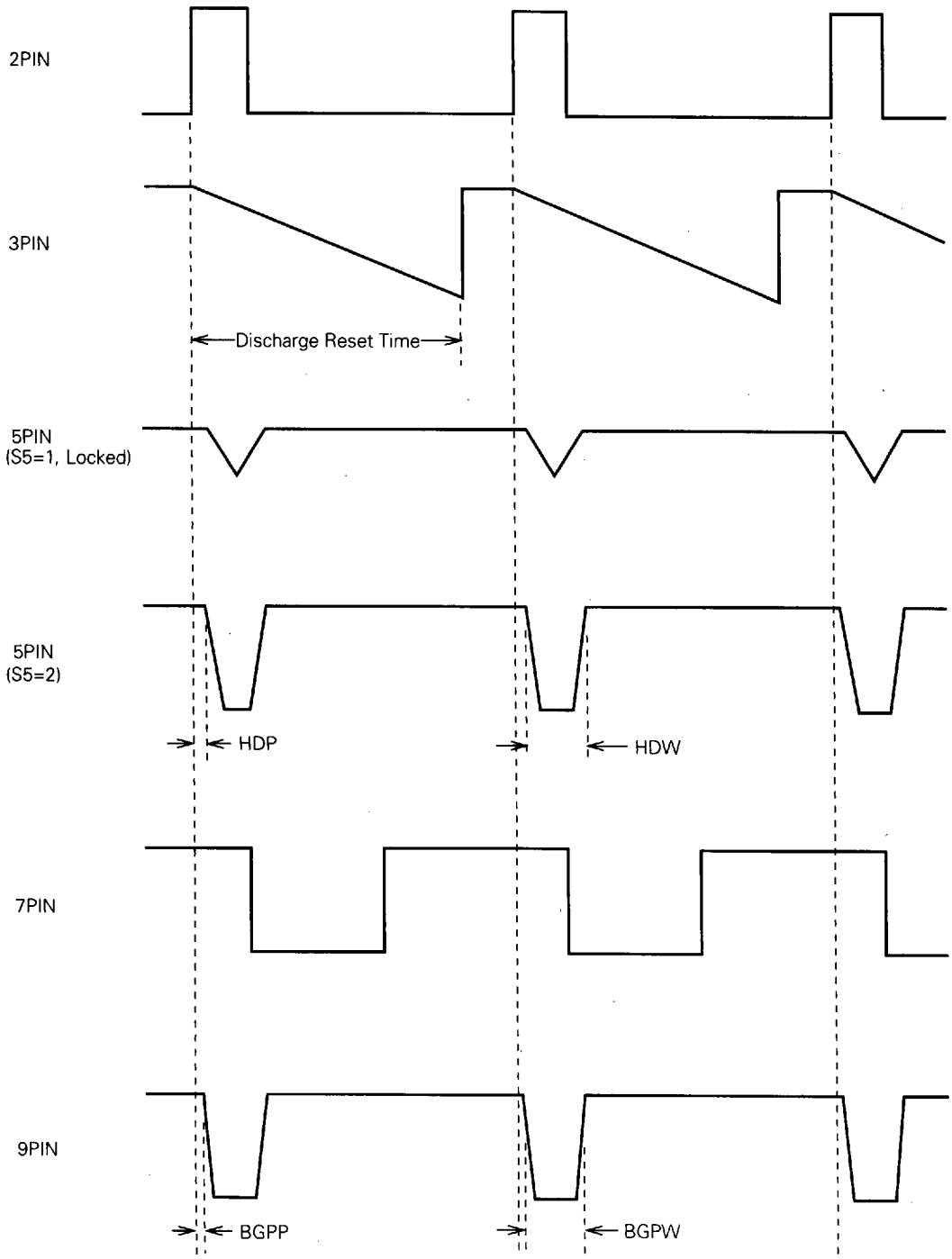
5. SG8



Note 1: Artificial PAL Operation Waveform Timing

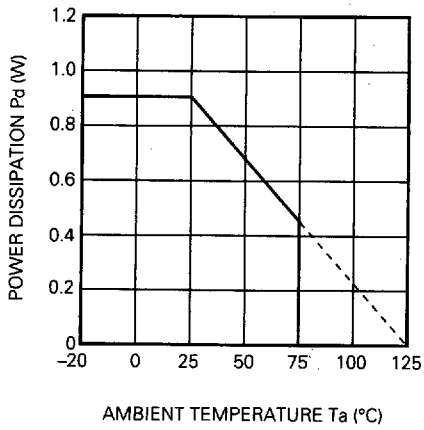


Note 2: Waveform Timing

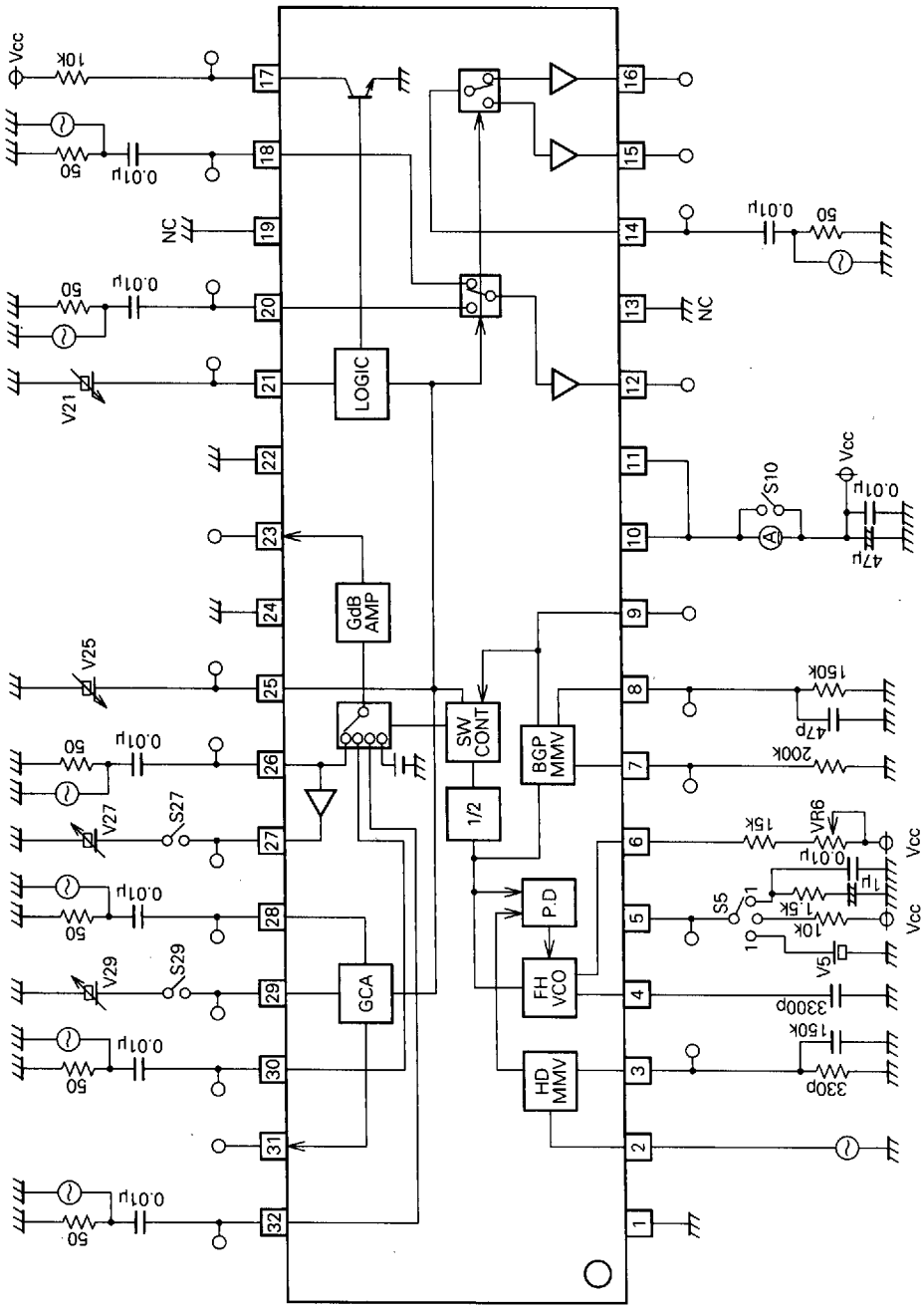


TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)

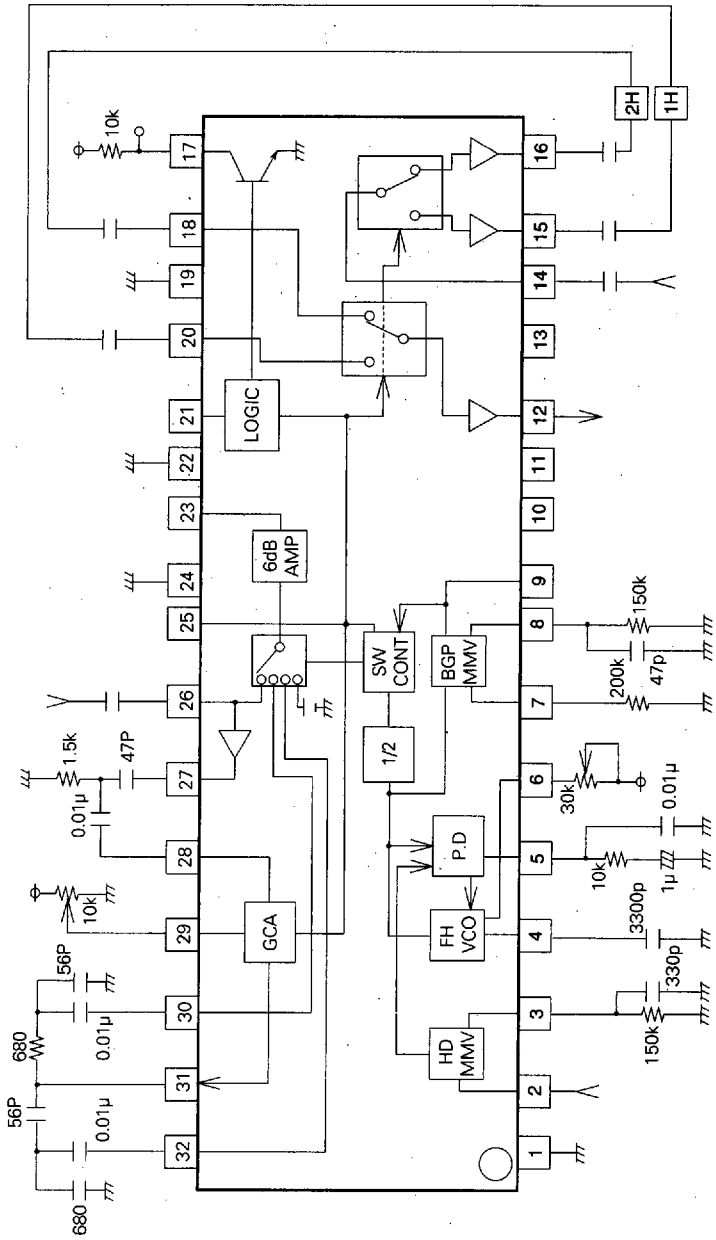


TEST CIRCUIT



Units Resistance:Ω
Capacitance:F

APPLICATION EXAMPLE



Units Resistance: Ω
Capacitance: F