



# M74HC595

## 8 BIT SHIFT REGISTER WITH OUTPUT LATCHES (3 STATE)

- HIGH SPEED:  
 $f_{MAX} = 59\text{MHz}$  (TYP.) at  $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\mu\text{A}$ (MAX.) at  $T_A=25^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 6\text{mA}$  (MIN.) FOR QA to QH  
 $|I_{OH}| = I_{OL} = 4\text{mA}$  (MIN.) FOR QH'
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:  
 $V_{CC}$  (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 595



### ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC595B1R	
SOP	M74HC595M1R	M74HC595RM13TR
TSSOP		M74HC595TTR

### DESCRIPTION

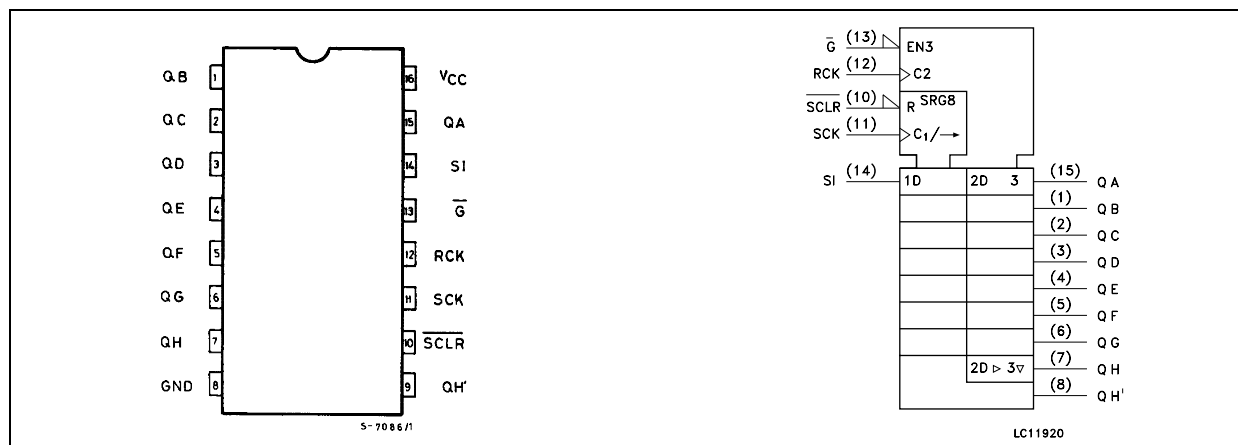
The M74HC595 is an high speed CMOS 8-BIT SHIFT REGISTERS/OUTPUT LATCHES (3-STATE) fabricated with silicon gate C<sup>2</sup>MOS technology.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register.

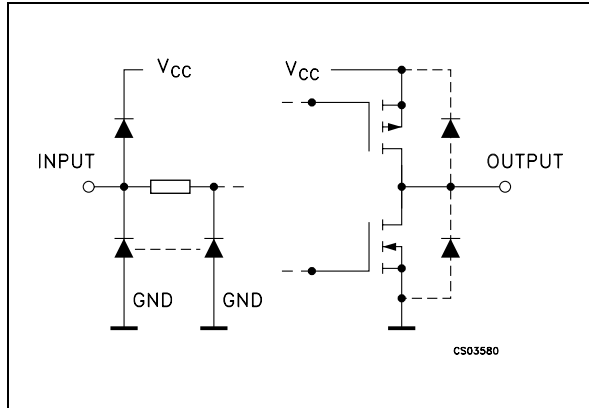
The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

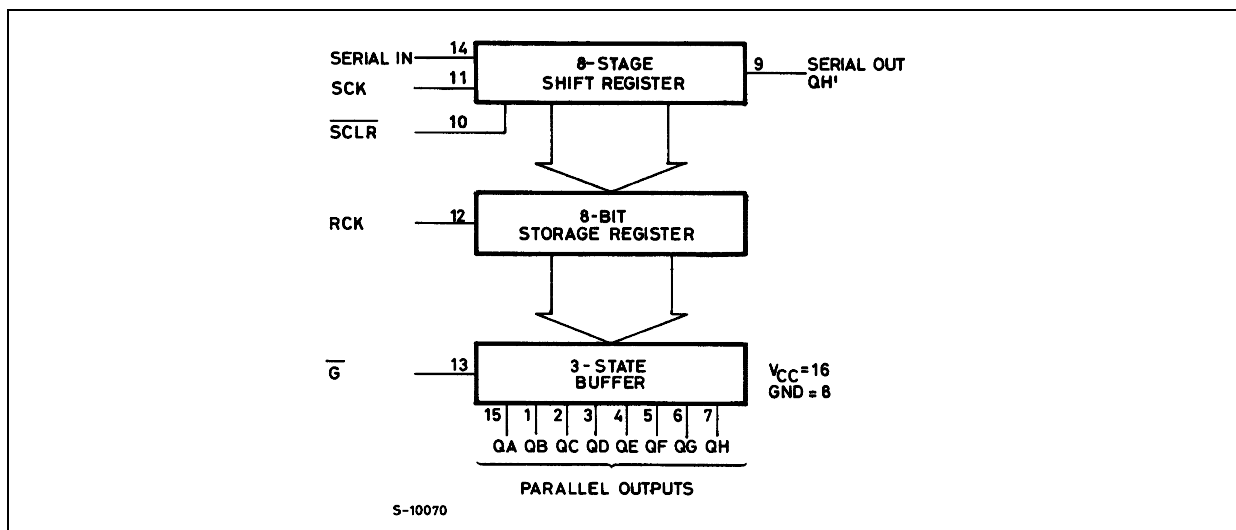
PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 15	QA to QH	Data Outputs
9	QH'	Serial Data Outputs
10	SCLR	Shift Register Clear Input
11	SCK	Shift Register Clock Input
13	$\overline{G}$	Output Enable Input
14	SI	Serial Data Input
12	RCK	Storage Register Clock Input
8	GND	Ground (0V)
16	V <sub>CC</sub>	Positive Supply Voltage

TRUTH TABLE

INPUTS					OUTPUTS
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA THRU QH OUTPUTS DISABLE
X	X	X	X	L	QA THRU QH OUTPUTS ENABLE
X	X	L	X	X	SHIFT REGISTER IS CLEARED
L		H	X	X	FIRST STAGE OF S.R. BECOMES "L" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
H		H	X	X	FIRST STAGE OF S.R. BECOMES "H" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
X		H	X	X	STATE OF S.R. IS NOT CHANGED
X	X	X		X	S.R. DATA IS STORED INTO STORAGE REGISTER
X	X	X		X	STORAGE REGISTER STATE IS NOT CHANGED

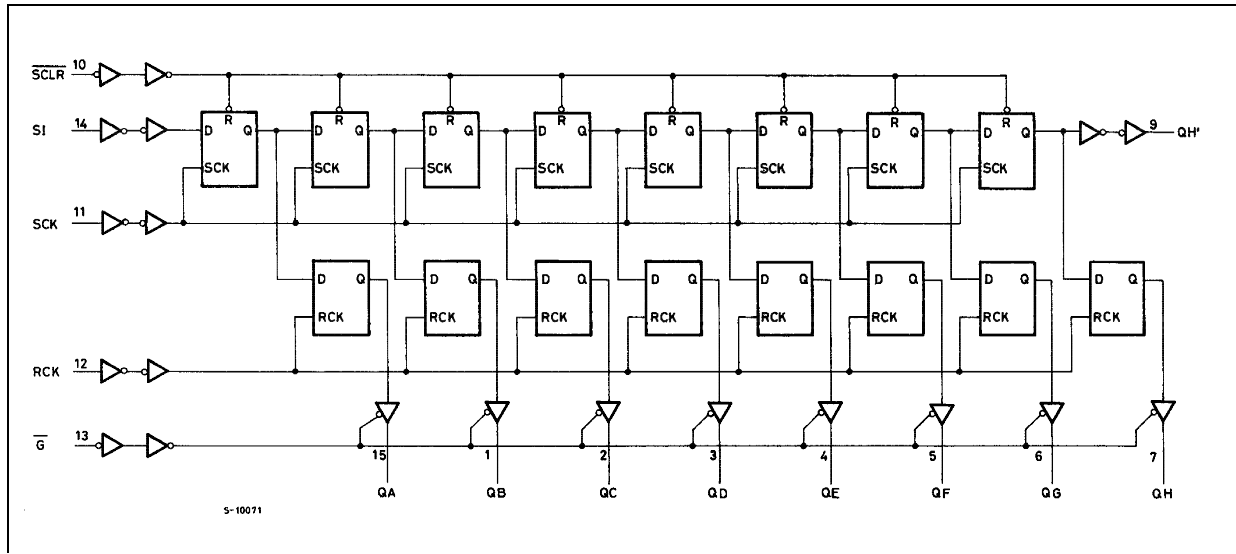
X: Don't Care

LOGIC DIAGRAM



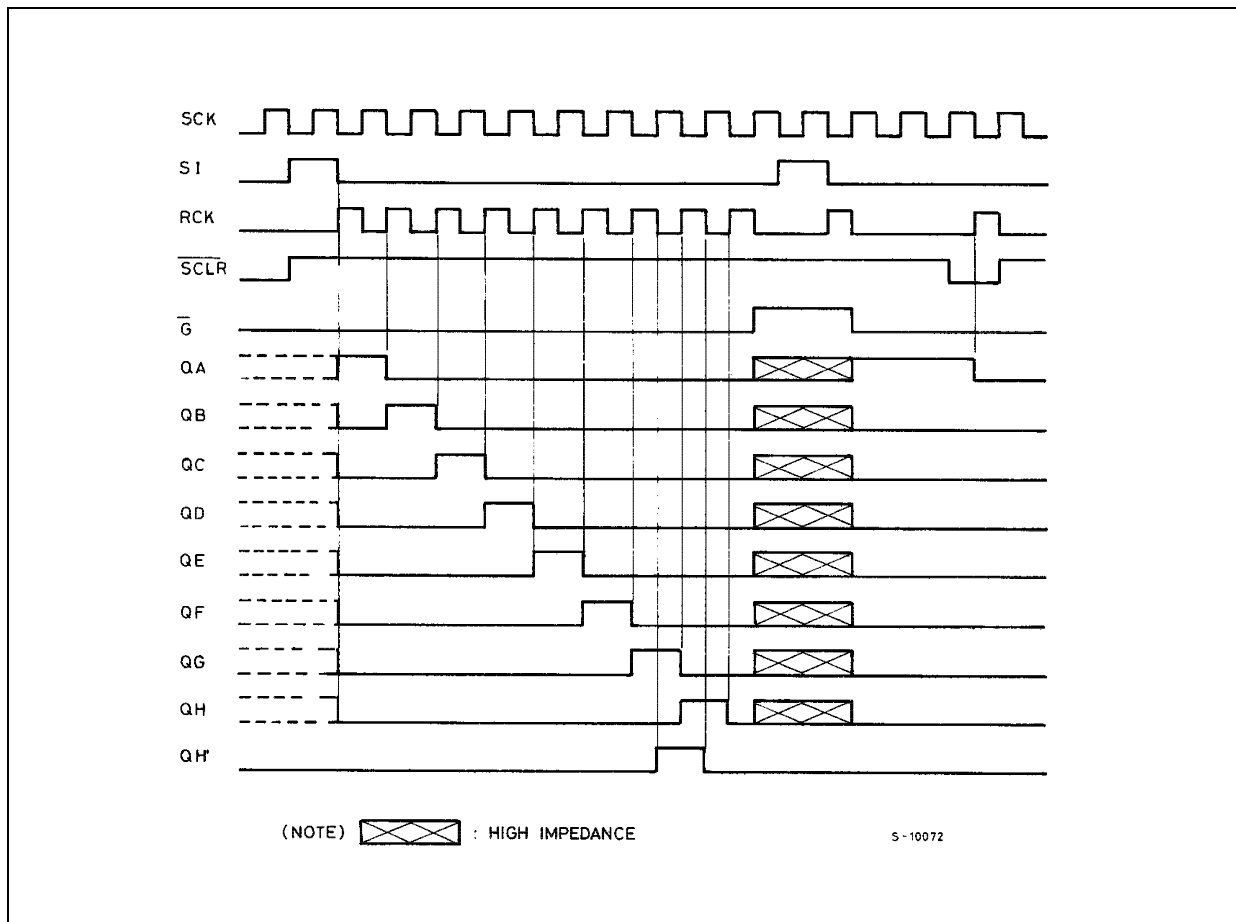
This logic diagram has not be used to estimate propagation delays

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

TIMING CHART



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 35$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 70$	mA
$P_D$	Power Dissipation	500(*)	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(\*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	2 to 6	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_{op}$	Operating Temperature	-55 to 125	°C	
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V <sub>IL</sub>	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V <sub>OH</sub>	High Level Output Voltage (for QH' outputs)	2.0	I <sub>O</sub> =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I <sub>O</sub> =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I <sub>O</sub> =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I <sub>O</sub> =-6.0 mA	4.18	4.31		4.13		4.10		
		6.0	I <sub>O</sub> =-7.8 mA	5.68	5.8		5.63		5.60		
V <sub>OH</sub>	High Level Output Voltage (for QA to QH outputs)	2.0	I <sub>O</sub> =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I <sub>O</sub> =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I <sub>O</sub> =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I <sub>O</sub> =-6.0 mA	4.18	4.31		4.13		4.10		
		6.0	I <sub>O</sub> =-7.8 mA	5.68	5.8		5.63		5.60		
V <sub>OL</sub>	Low Level Output Voltage (for QH' outputs)	2.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		6.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =6.0 mA		0.17	0.26		0.33		0.40	
		6.0	I <sub>O</sub> =7.8 mA		0.18	0.26		0.33		0.40	
V <sub>OL</sub>	Low Level Output Voltage (for QA to QH outputs)	2.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		6.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =6.0 mA		0.17	0.26		0.33		0.40	
		6.0	I <sub>O</sub> =7.8 mA		0.18	0.26		0.33		0.40	
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			± 0.1		± 1		± 1	μA
I <sub>OZ</sub>	High Impedance Output Leakage Current	6.0	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND			± 0.5		± 5		± 10	μA
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		80	μA

**M74HC595**

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6\text{ns}$ )

Symbol	Parameter	Test Condition			Value						Unit	
		$V_{CC}$ (V)	$C_L$ (pF)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{TLH}$ $t_{THL}$	Output Transition Time (Qn)	2.0	50			25	60		75		90	ns
		4.5			7	12		15		18		
		6.0			6	10		13		15		
$t_{TLH}$ $t_{THL}$	Output Transition Time (QH')	2.0	50			30	75		95		115	ns
		4.5			8	15		19		23		
		6.0			7	13		16		20		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (SCK - QH')	2.0	50			45	125		155		190	ns
		4.5			15	25		31		38		
		6.0			13	21		26		32		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (SCLR - QH')	2.0	50			60	175		220		265	ns
		4.5			18	35		44		53		
		6.0			15	30		37		45		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (RCK - Qn)	2.0	50			60	150		190		225	ns
		4.5			20	30		38		45		
		6.0			17	26		32		38		
		2.0	150			75	190		240		285	ns
		4.5			25	38		48		57		
		6.0			22	32		41		48		
$t_{PZL}$ $t_{PZH}$	High Impedance Output Enable Time	2.0	50	$R_L = 1 \text{ K}\Omega$		45	135		170		205	ns
		4.5				15	27		34		41	
		6.0				13	23		29		35	
		2.0	150	$R_L = 1 \text{ K}\Omega$		60	175		220		265	ns
		4.5				20	35		44		53	
		6.0				17	30		37		45	
$t_{PLZ}$ $t_{PHZ}$	High Impedance Output Disable Time	2.0	50	$R_L = 1 \text{ K}\Omega$		30	150		190		225	ns
		4.5				15	30		38		45	
		6.0				14	26		32		38	
$f_{MAX}$	Maximum Clock Frequency	2.0	50		6.0	17		4.8		4		MHz
		4.5			30	50		24		20		
		6.0			35	59		28		24		
		2.0	150		5.2	14		4.2		3.4		MHz
		4.5			26	40		21		17		
		6.0			31	45		25		20		
$t_{W(H)}$	Minimum Pulse Width (SCK, RCK)	2.0	50			17	75		95		110	ns
		4.5			6	15		19		22		
		6.0			6	13		16		19		
$t_{W(L)}$	Minimum Pulse Width (SCLR)	2.0	50			20	75		95		110	ns
		4.5			6	15		19		22		
		6.0			6	13		16		19		
$t_s$	Minimum Set-up Time (SI - CCK)	2.0	50			25	50		65		75	ns
		4.5			5	10		13		15		
		6.0			4	9		11		13		
$t_s$	Minimum Set-up Time (SCK - RCK)	2.0	50			35	75		95		110	ns
		4.5			8	15		19		22		
		6.0			6	13		16		19		

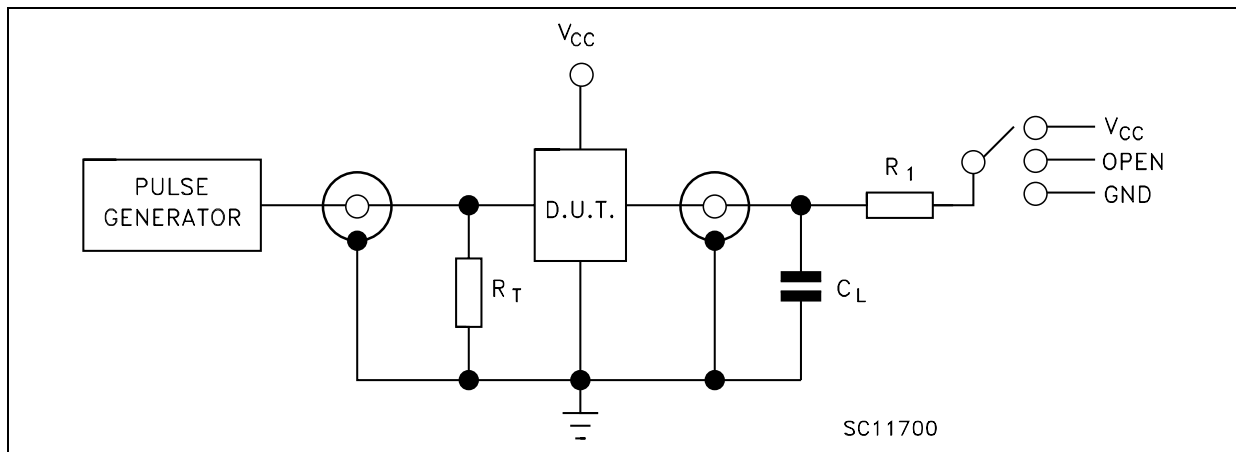
Symbol	Parameter	Test Condition			Value						Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>s</sub>	Minimum Set-up Time (SCRL - RCK)	2.0	50			40	100		125		145	ns
		4.5				10	20		25		29	
		6.0				7	17		21		25	
t <sub>h</sub>	Minimum Hold Time	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
t <sub>REM</sub>	Minimum Clear Removal Time	2.0	50			15	50		65		75	ns
		4.5				3	10		13		15	
		6.0				3	9		11		13	

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Condition			Value						Unit	
		V <sub>CC</sub> (V)			T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance					5	10		10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)					184						pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I<sub>CC(opr)</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC</sub>

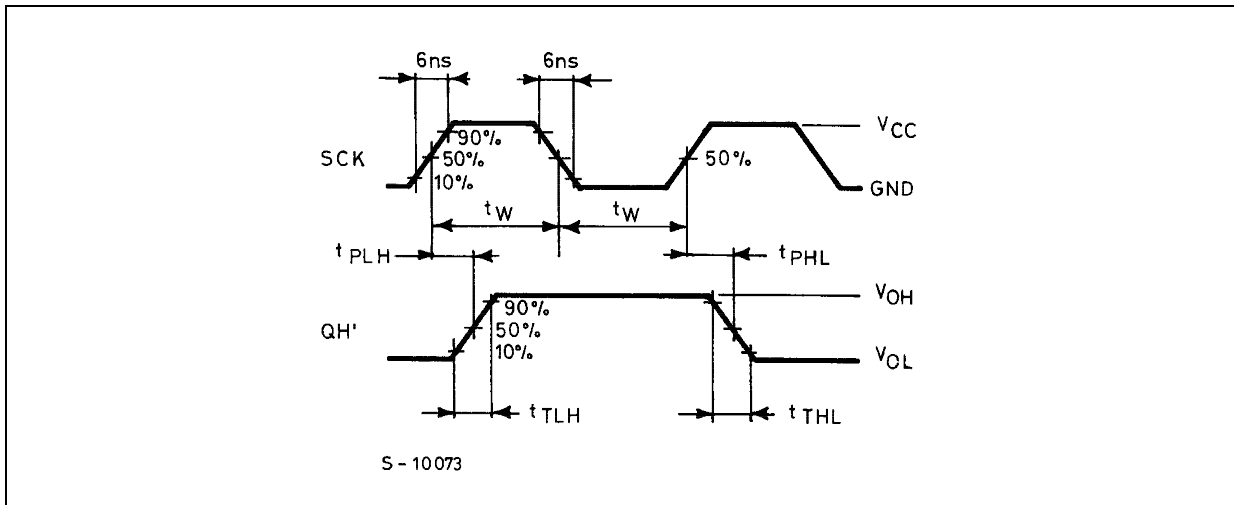
**TEST CIRCUIT**



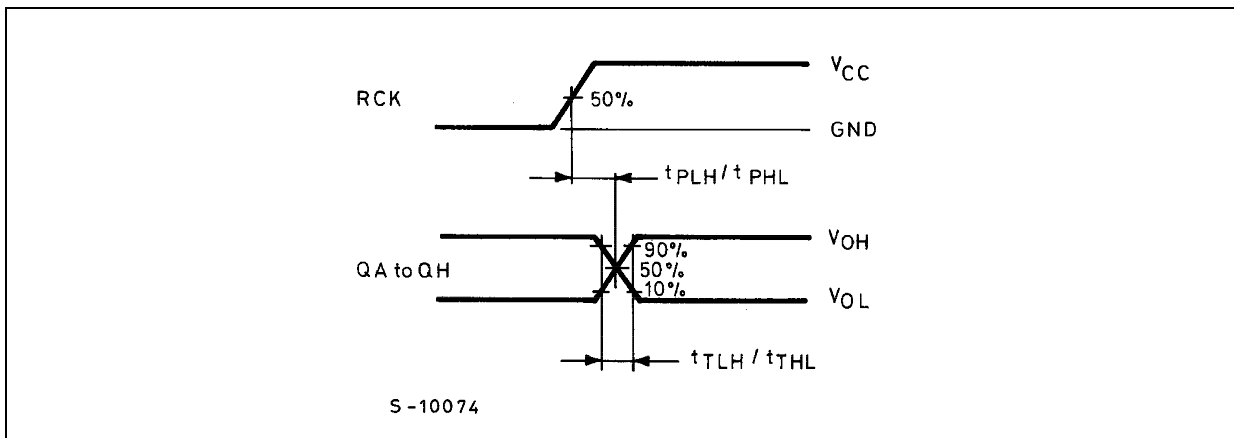
TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
t <sub>PZL</sub> , t <sub>PLZ</sub>	V <sub>CC</sub>
t <sub>PZH</sub> , t <sub>PHZ</sub>	GND

C<sub>L</sub> = 50pF/150pF or equivalent (includes jig and probe capacitance)  
R<sub>1</sub> = 1KΩ or equivalent  
R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

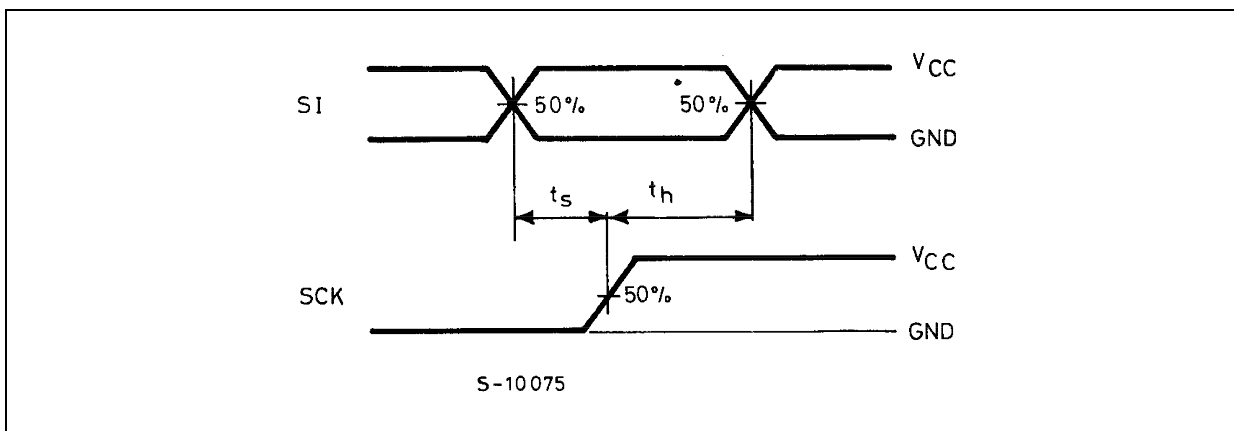
**WAVEFORM 1 : SCK TO QH' PROPAGATION DELAY TIMES, SCK MINIMUM PULSE WIDTH**  
 (f=1MHz; 50% duty cycle)



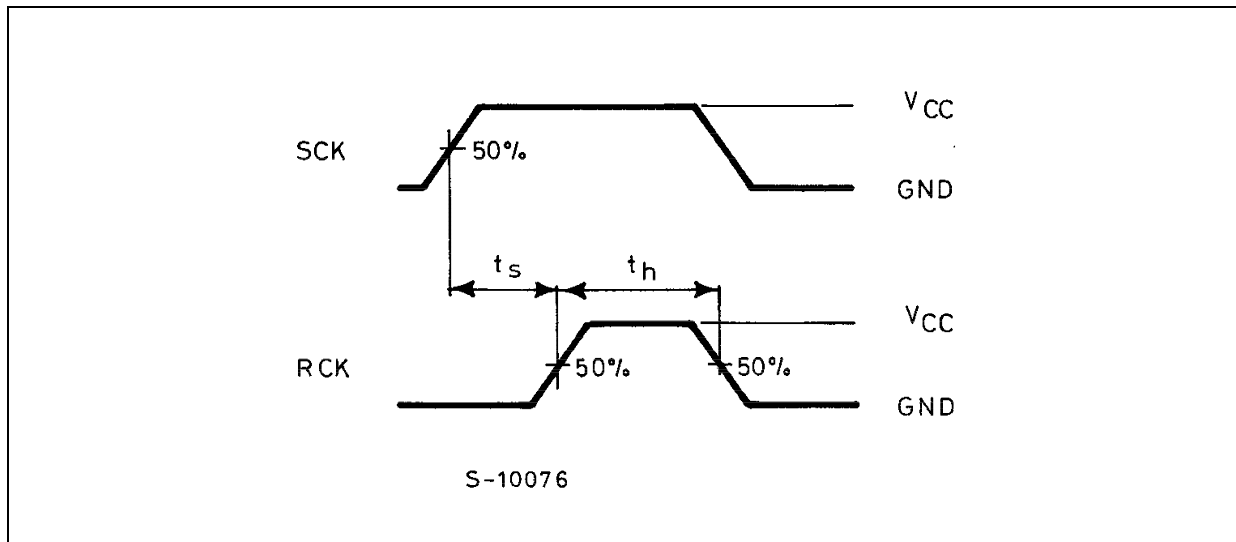
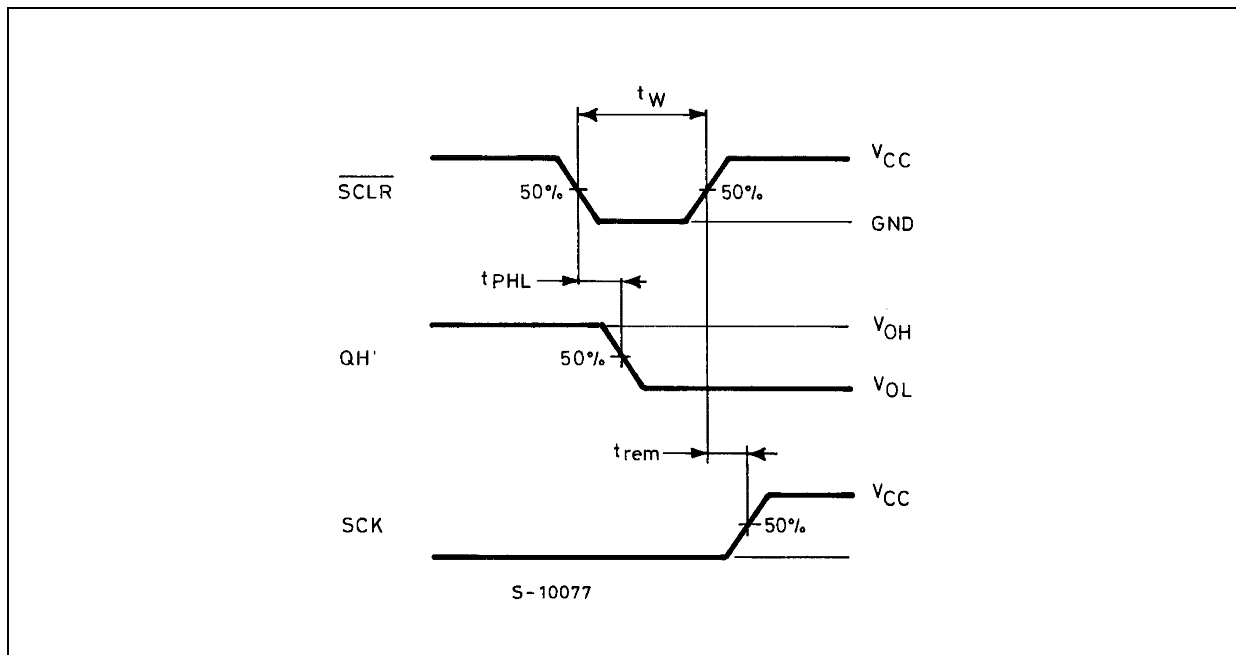
**WAVEFORM 2 : RCK TO Qn PROPAGATION DELAY TIMES** (f=1MHz; 50% duty cycle)



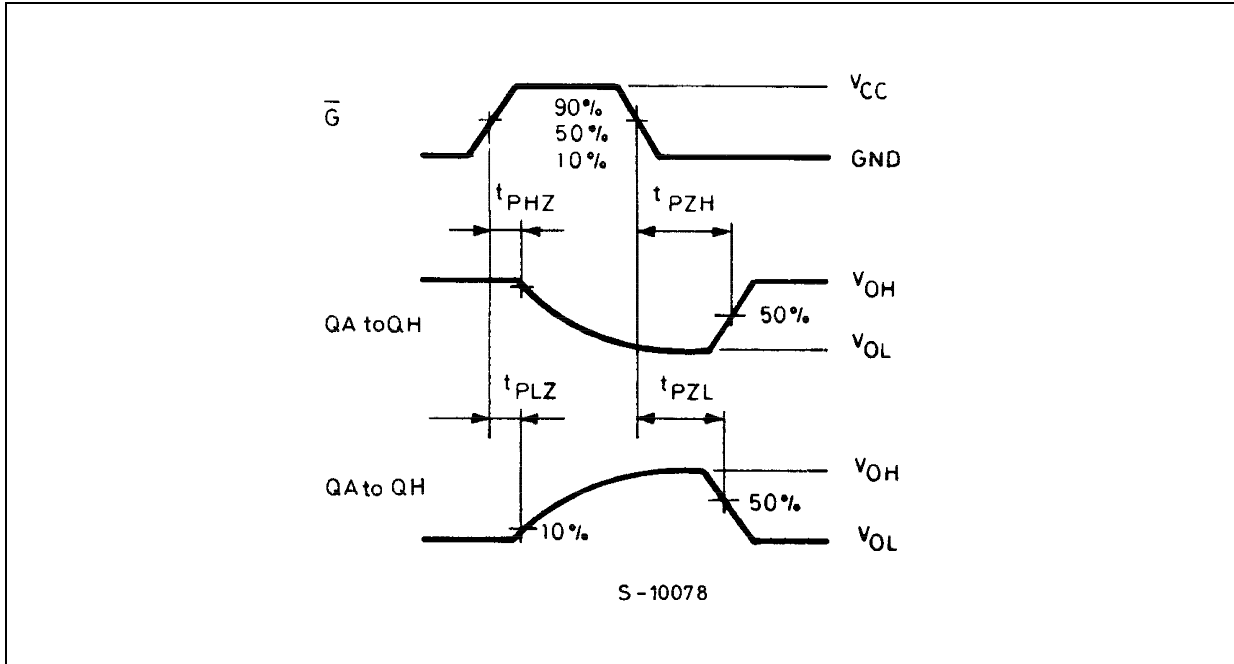
**WAVEFORM 3 : SI TO SCK SETUP AND HOLD TIMES** (f=1MHz; 50% duty cycle)



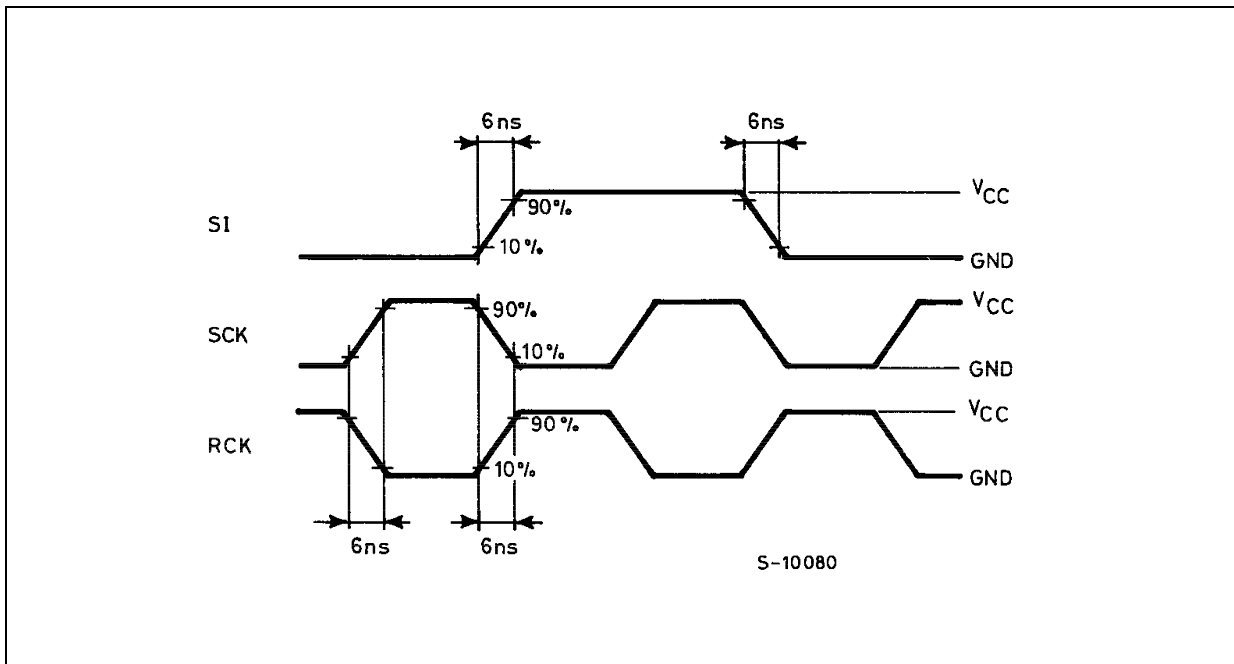


**WAVEFORM 4 : SCK TO RCK SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)****WAVEFORM 5 :  $\overline{\text{SCLR}}$  MINIMUM PULSE WIDTH, MINIMUM REMOVAL TIME (f=1MHz; 50% duty cycle)**

WAVEFORM 6 : OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)

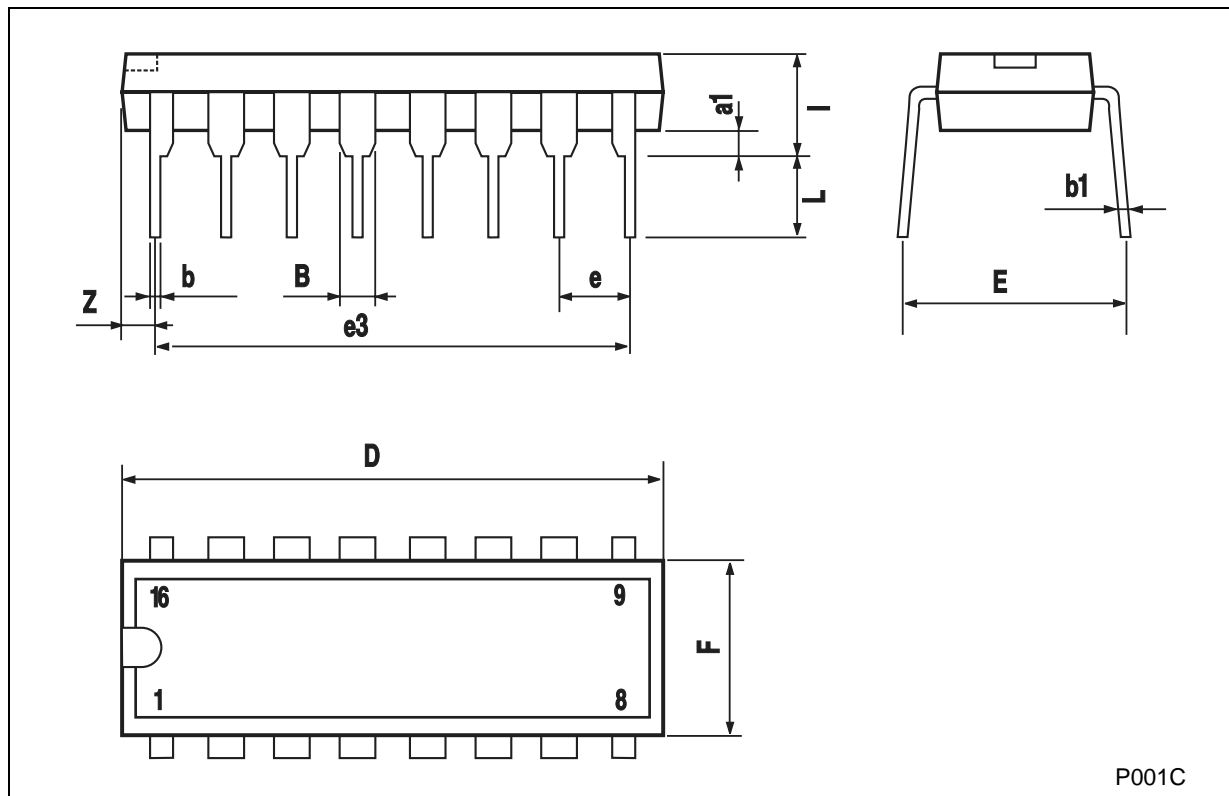


WAVEFORM 7 : INPUT WAVEFORM (f=1MHz; 50% duty cycle)



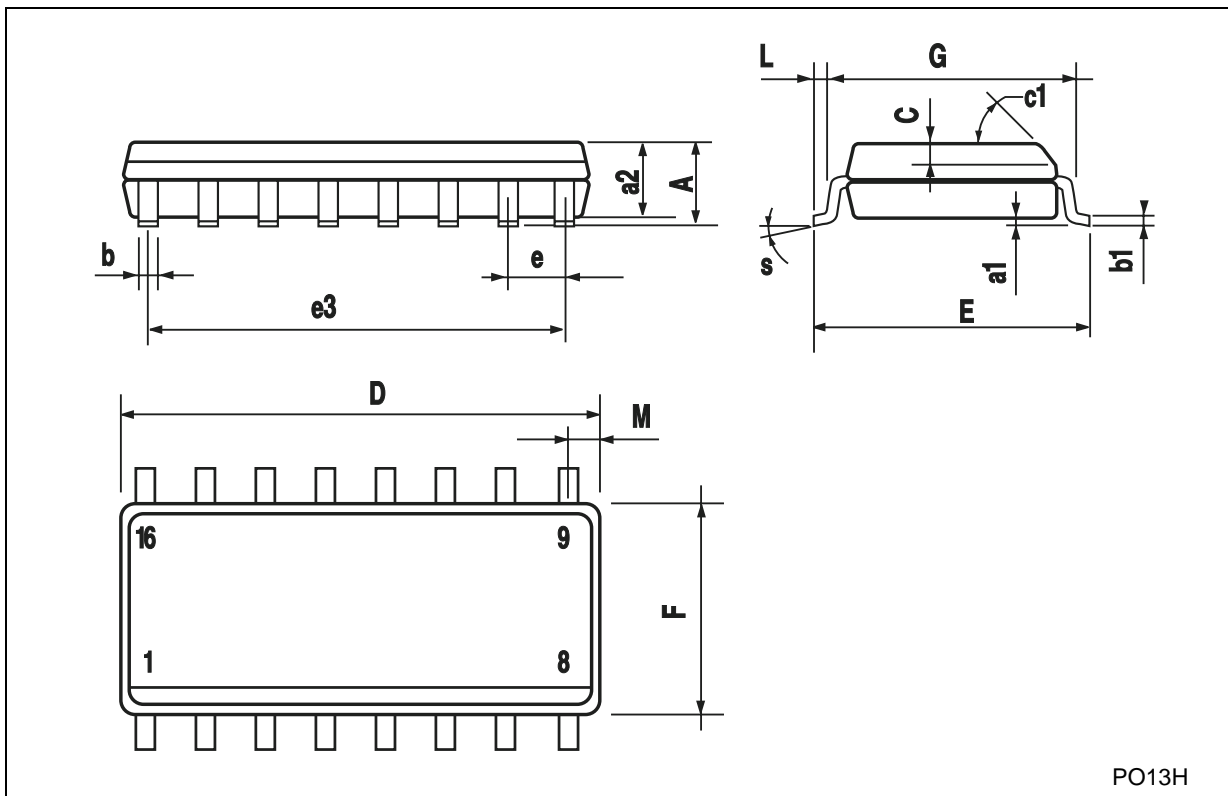
### Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



**SO-16 MECHANICAL DATA**

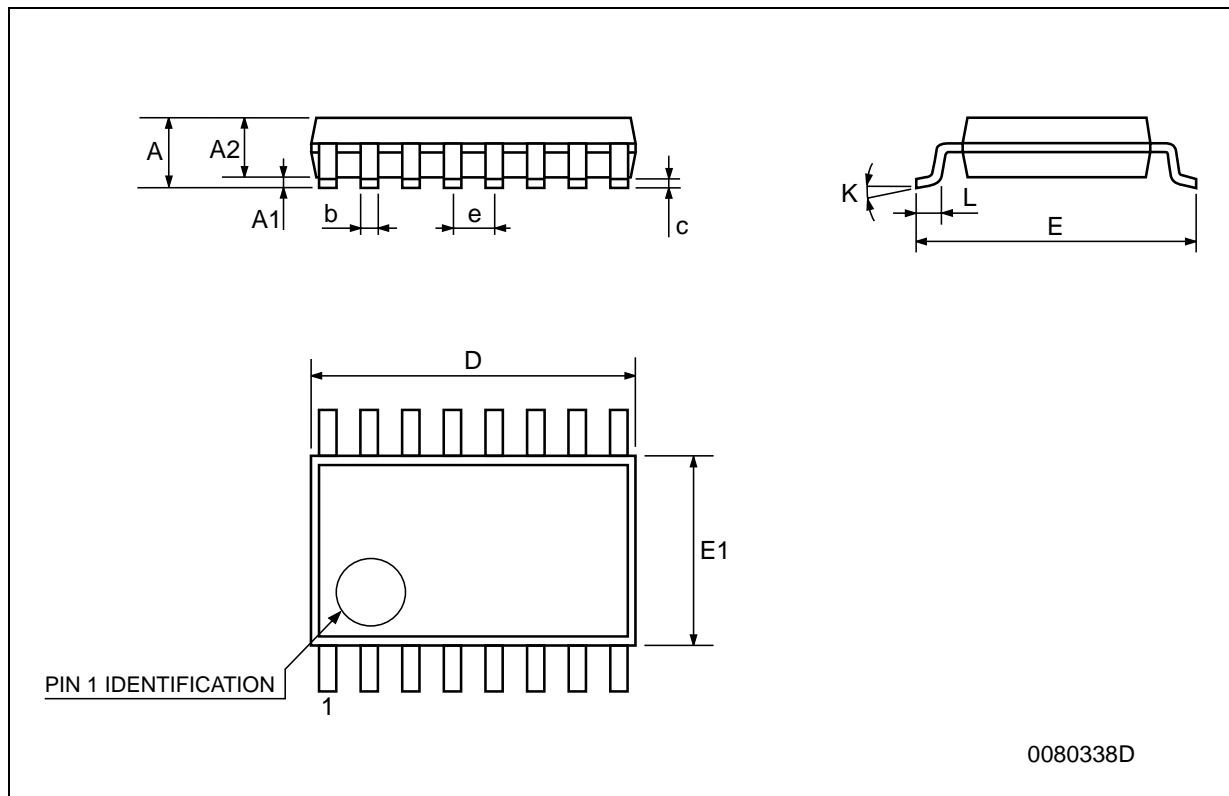
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

## TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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