

# MAX44260/MAX44261/MAX44263

## 1.8V, 15MHz Low-Offset, Low-Power, Rail-to-Rail I/O Op Amps

### General Description

The MAX44260/MAX44261/MAX44263 offer a unique combination of high speed, precision, low noise, and low-voltage operation making them ideally suited for a large number of signal processing functions such as filtering and amplification of signals in portable and industrial equipment.

The amplifiers feature an input offset of less than 50 $\mu$ V and a high-gain bandwidth product of 15MHz while maintaining a low 1.8V supply rail. The devices' rail-to-rail input/outputs and low noise guarantee maximum dynamic range in demanding applications such as 12- to 14-bit SAR ADC drivers. Unlike traditional rail-to-rail input structures, input crossover distortion is absent due to an optimized input stage with an ultra-quiet charge pump.

The MAX44260 includes a fast-power-on shutdown mode for further power savings. The MAX44261 offers a unique on-demand calibration pin where the user can invoke self-trimming of the input offset voltage. The MAX44263 is a dual amplifier.

The family of parts operates from a supply range of 1.8V to 5.5V over the -40°C to +125°C temperature range and can operate down to 1.7V over the 0°C to +70°C temperature range. The MAX44260/MAX44261 are available in small, 6-pin SC70 packages. The MAX44260 is also available in a 1mm x 1.5mm thin  $\mu$ DFN (ultra-thin LGA) package. The MAX44263 is available in a small 8-pin SC70 package.

**Ordering Information** appears at end of data sheet.

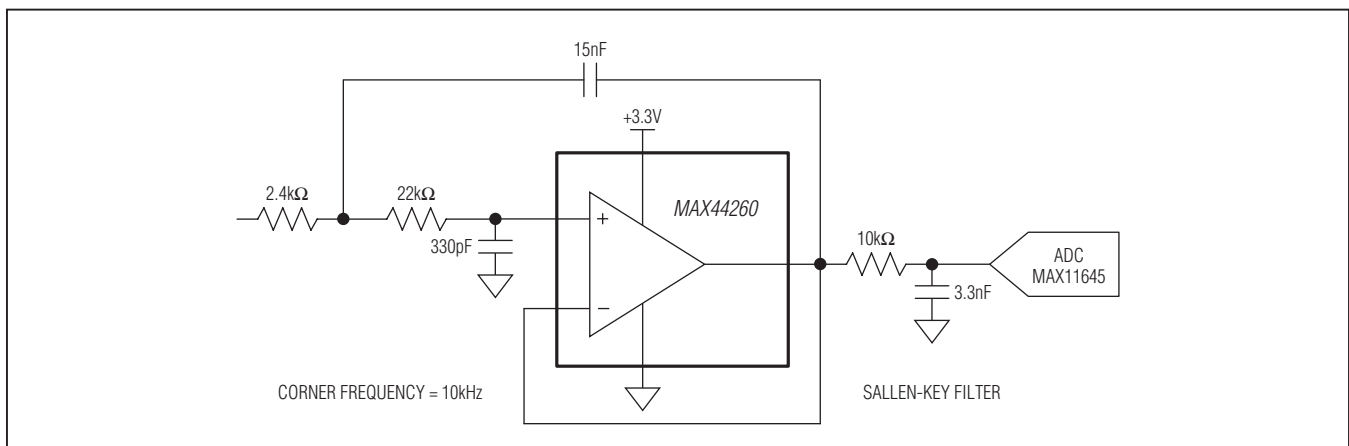
### Features

- ◆ Low 1.8V Supply Rail Over the -40°C to +125°C Range
- ◆ 1.7V Supply Rail Over the 0°C to +70°C Range
- ◆ 15MHz Unity-Gain Bandwidth
- ◆ Low 12.7nV/ $\sqrt{\text{Hz}}$  Input Voltage-Noise Density
- ◆ Low 1.2fA/ $\sqrt{\text{Hz}}$  Input Current-Noise Density
- ◆ Low 50 $\mu$ V (max)  $V_{OS}$  at +25°C
- ◆ On-Demand  $V_{OS}$  Self-Calibration (MAX44261)
- ◆ 500fA Low Input Bias Current
- ◆ 750 $\mu$ A Quiescent Current per Amplifier
- ◆ < 1 $\mu$ A Supply Current in Shutdown
- ◆ Small, 2mm x 2mm SC70 and 1mm x 1.5mm Thin  $\mu$ DFN (MAX44260) Packages
- ◆ Low 110dB Total Harmonic Distortion

### Applications

Notebooks  
 3G/4G Handsets  
 Portable Media Players  
 Portable Medical Instruments  
 Battery-Operated Devices  
 Analog-to-Digital Converter Buffers  
 Transimpedance Amplifiers  
 General-Purpose Signal Processing

### Typical Application Circuit



For related parts and recommended products to use with this part, refer to: [www.maximintegrated.com/MAX44260.related](http://www.maximintegrated.com/MAX44260.related)

**For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at [www.maximintegrated.com](http://www.maximintegrated.com).**

# MAX44260/MAX44261/MAX44263

## 1.8V, 15MHz Low-Offset, Low-Power, Rail-to-Rail I/O Op Amps

### ABSOLUTE MAXIMUM RATINGS

IN+, IN-, OUT .....	(V <sub>SS</sub> - 0.3V) to (V <sub>DD</sub> + 0.3V)	6-Pin Thin $\mu$ DFN (Ultra-Thin LGA)	
V <sub>DD</sub> to V <sub>SS</sub> .....	-0.3V to +6V	(derate 2.1mW/°C above +70°C) .....	110.2mW
SHDN, CAL .....	-0.3V to +6V	Operating Temperature Range .....	-40°C to +125°C
Output to Short-Circuit Ground Duration .....	10s	Junction Temperature .....	+150°C
Continuous Input Current into Any Pin.....	$\pm$ 20mA	Lead Temperature (soldering, 10s) .....	+300°C
Continuous Power Dissipation (T <sub>A</sub> = +70°C)		Soldering Temperature (reflow) .....	+260°C
SC70 (derate 3.1mW/°C above +70°C) .....	245mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### PACKAGE THERMAL CHARACTERISTICS (Note 1)

SC70	Thin $\mu$ DFN (Ultra-Thin LGA)
Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) ....	326.5°C/W
Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) .....	470°C/W
Junction-to-Case Thermal Resistance ( $\theta_{JC}$ ) .....	115°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

### ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = 3.3V, V<sub>SS</sub> = 0V, V<sub>IN+</sub> = V<sub>IN-</sub> = V<sub>DD</sub>/2, R<sub>L</sub> = 10k $\Omega$  to V<sub>DD</sub>/2, V<sub>CAL</sub> = V<sub>SHDN</sub> = V<sub>DD</sub>, T<sub>A</sub> = -40°C to +125°C. Typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC CHARACTERISTICS</b>						
Input Voltage Range	V <sub>IN+</sub> V <sub>IN-</sub>	Guaranteed by CMRR test	-0.1		V <sub>DD</sub> + 0.1	V
Input Offset Voltage (Note 3)	V <sub>OS</sub>	T <sub>A</sub> = +25°C		10	50	$\mu$ V
		T <sub>A</sub> = -40°C to +125°C after calibration			100	
		T <sub>A</sub> = -40°C to +125°C	MAX44260/MAX44261		500	
		MAX44263			800	
Input Offset Voltage Drift (Note 3)	V <sub>OS</sub> - TC	MAX44260/MAX44261		0.8	5	$\mu$ V/°C
		MAX44263		1	8	
Input Bias Current (Note 3)	I <sub>B</sub>	T <sub>A</sub> = +25°C	MAX44260/MAX44261	0.01	0.5	pA
			MAX44263	0.01	0.5	
		T <sub>A</sub> = -40°C to +85°C			10	
		T <sub>A</sub> = -40°C to +125°C	MAX44260/MAX44261		100	
		MAX44263			160	
Input Capacitance	C <sub>IN</sub>			0.4		pF
Common-Mode Rejection Ratio	CMRR	V <sub>CM</sub> = -0.1V to (V <sub>DD</sub> + 0.1V)	75	90		dB
Open-Loop Gain	A <sub>OL</sub>	0.4V $\leq$ V <sub>OUT</sub> $\leq$ V <sub>DD</sub> - 0.4V, R <sub>OUT</sub> = 10k $\Omega$	MAX44260/MAX44261	100	115	dB
			MAX44263	97	115	
		0.4V $\leq$ V <sub>OUT</sub> $\leq$ V <sub>DD</sub> - 0.4V, R <sub>OUT</sub> = 600 $\Omega$	MAX44260/MAX44261	91	100	
			MAX44263	86	100	
		0.4V $\leq$ V <sub>OUT</sub> $\leq$ V <sub>DD</sub> - 0.4V, R <sub>OUT</sub> = 32 $\Omega$			80	

# MAX44260/MAX44261/MAX44263

## 1.8V, 15MHz Low-Offset, Low-Power, Rail-to-Rail I/O Op Amps

### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{CAL} = \overline{V_{SHDN}} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Output Short-Circuit Current	$I_{SC}$	To $V_{DD}$ or $V_{SS}$		50		mA	
Output Voltage Swing	$V_{OL} - V_{SS}$	$R_{OUT} = 10k\Omega$			20	mV	
		$R_{OUT} = 600\Omega$			50		
		$R_{OUT} = 32\Omega$		400	700		
	$V_{DD} - V_{OH}$	$R_{OUT} = 10k\Omega$	MAX44260/MAX44261				10
			MAX44263				10
		$R_{OUT} = 600\Omega$	MAX44260/MAX44261				40
		MAX44263			50		
		$R_{OUT} = 32\Omega$		400	800		
<b>AC CHARACTERISTICS</b>							
Input Voltage-Noise Density	$e_n$	$f = 10kHz$		12.7		$nV/\sqrt{Hz}$	
Input Current-Noise Density	$i_n$	$f = 10kHz$		1.2		$fA/\sqrt{Hz}$	
Gain-Bandwidth Product	GBWP			15		MHz	
Slew Rate	SR			7		V/ $\mu s$	
Settling Time		$V_{OUT} = 2V_{P-P}$ , $V_{DD} = 3.3V$ , $A_V = 1V/V$ , $C_L = 30pF$ (load), settle to 0.01%		1.7		$\mu s$	
Capacitive Loading	$C_{LOAD}$	No sustained oscillation		300		pF	
Total Harmonic Distortion	THD	$f = 10kHz$ , $V_O = 2V_{P-P}$ , $A_V = 1$ , $R_{OUT} = 10k\Omega$		-110		dB	
Output Transient Recovery Time		$\Delta V_{OUT} = 0.2V$ , $V_{DD} = 3.3V$ , $A_V = 1V/V$ ; $R_S = 20\Omega$ , $C_L = 1nF$ (load)		1		$\mu s$	
<b>POWER-SUPPLY CHARACTERISTICS</b>							
Power-Supply Range	$V_{DD}$	Guaranteed by PSRR	1.8		5.5	V	
		$T_A = 0^\circ C$ to $+70^\circ C$	1.7		5.5		
Power-Supply Rejection Ratio	PSRR	$V_{CM} = V_{DD}/2$	MAX44260/MAX44261	82	95	dB	
			MAX44263	76	95		
Quiescent Current	$I_{DD}$	MAX44260/MAX44261		750	1200	$\mu A$	
		MAX44263 (per amplifier)		650	1100		
Shutdown Supply Current	$I_{SHDN}$	(Note 4)			1	$\mu A$	
Shutdown Input Low	$V_{IL}$	(Note 4)			0.5	V	
Shutdown Input High	$V_{IH}$	(Note 4)	1.3			V	
Output Leakage Current in Shutdown	$I_{SHDN}$	(Note 4)		100		pA	
Shutdown Input Bias Current	$I_{IL}/I_{IH}$	MAX44260			1	$\mu A$	
		MAX44261			0.1		
Shutdown Turn-On Time (Note 4)	$t_{SHDN}$	$T_A = +25^\circ C$ (Note 3)		14.4	18.9	$\mu s$	
		$T_A = -40^\circ C$ to $+125^\circ C$ (Note 3)					26.7

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{CAL} = V_{SHDN} = V_{DD}$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ . Typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Time (Note 4)	$t_{ON}$	$T_A = +25^{\circ}C$ (Note 3)		9.7	15.2	ms
		$T_A = -40^{\circ}C$ to $+125^{\circ}C$ (Note 3)			18.4	

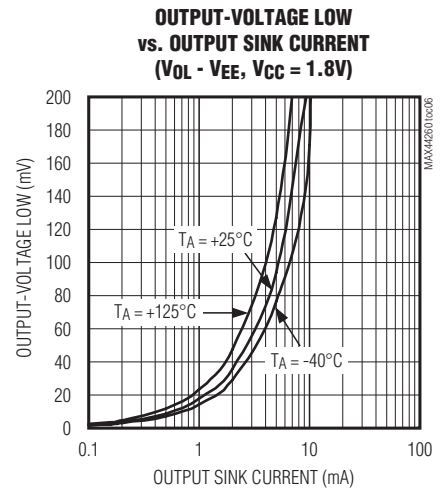
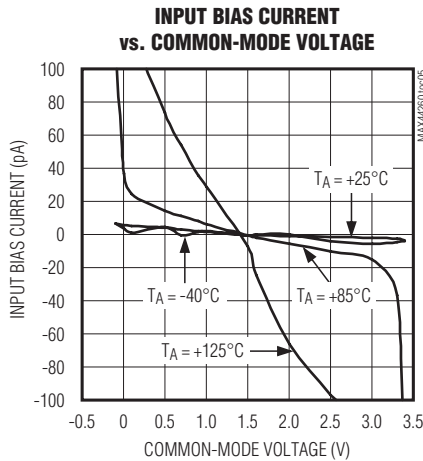
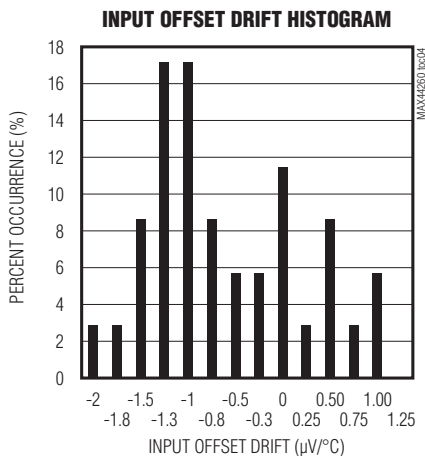
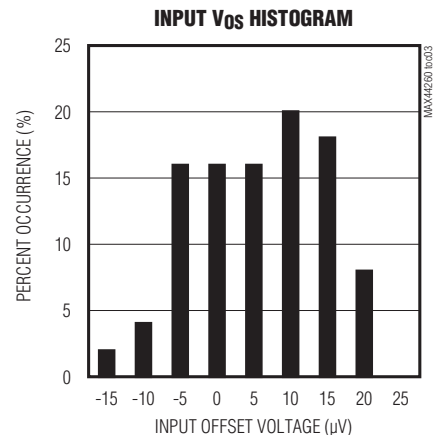
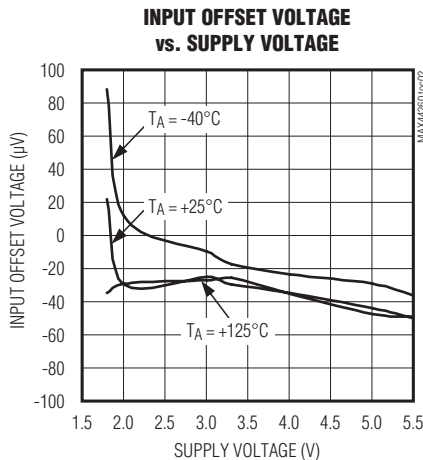
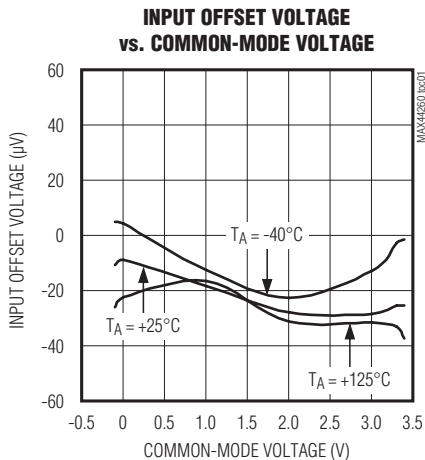
**Note 2:** All devices are 100% production tested at  $T_A = +25^{\circ}C$ . Temperature limits are guaranteed by design.

**Note 3:** Guaranteed by design.

**Note 4:** MAX44260/MAX44261 only.

### Typical Operating Characteristics

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{CAL} = V_{SHDN} = V_{DD}$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ . Typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted. All devices are 100% production tested at  $T_A = +25^{\circ}C$ . Temperature limits are guaranteed by design.)

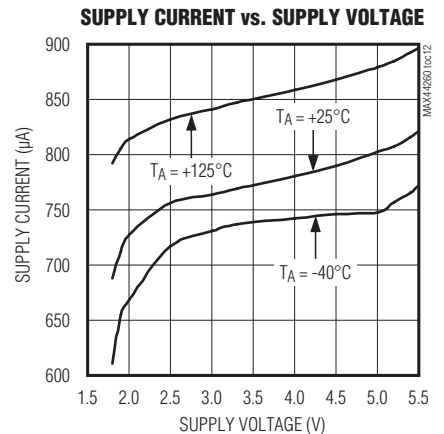
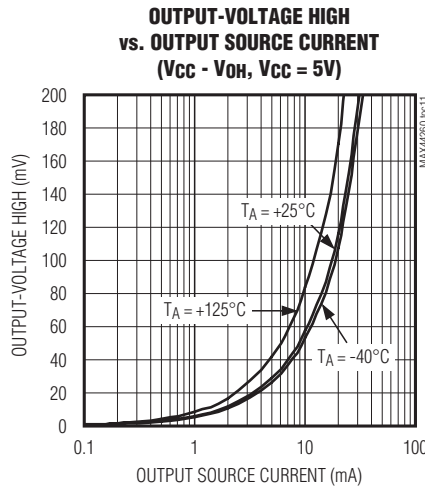
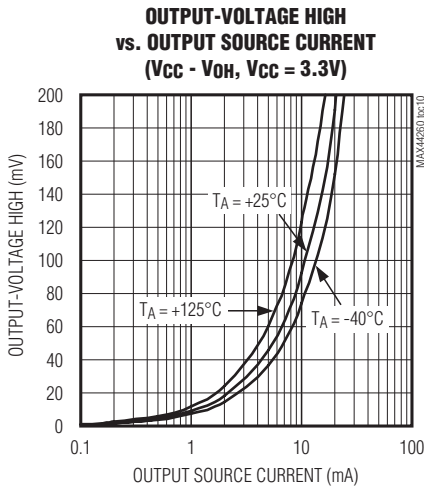
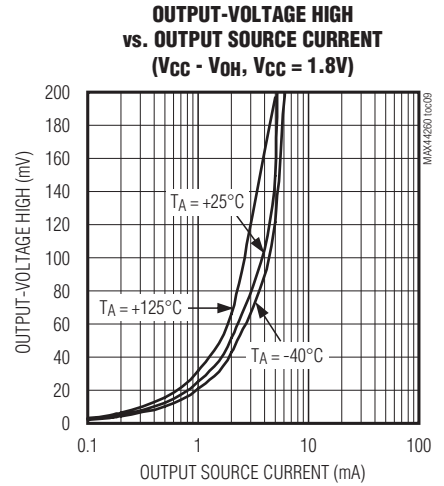
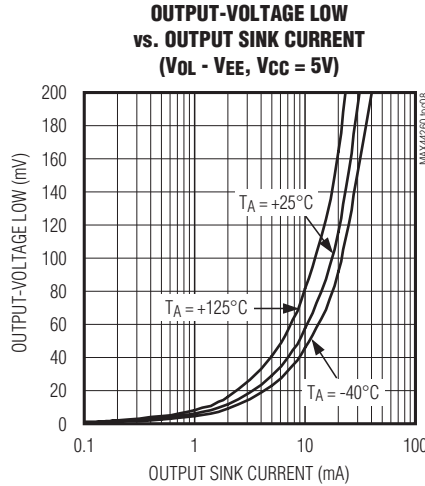
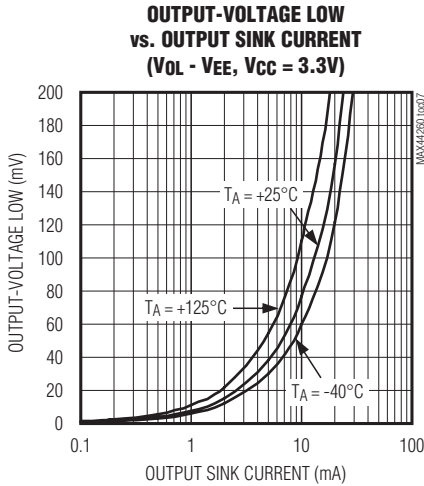


# MAX44260/MAX44261/MAX44263

## 1.8V, 15MHz Low-Offset, Low-Power, Rail-to-Rail I/O Op Amps

### Typical Operating Characteristics (continued)

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{CAL} = V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. All devices are 100% production tested at  $T_A = +25^\circ C$ . Temperature limits are guaranteed by design.)



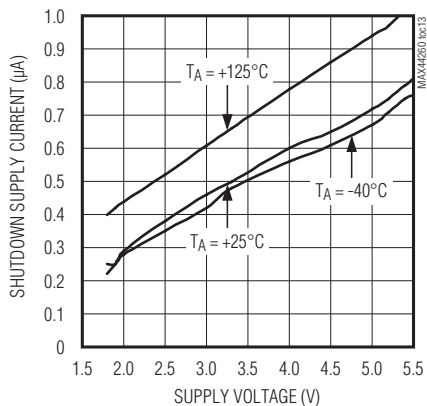
# MAX44260/MAX44261/MAX44263

## 1.8V, 15MHz Low-Offset, Low-Power, Rail-to-Rail I/O Op Amps

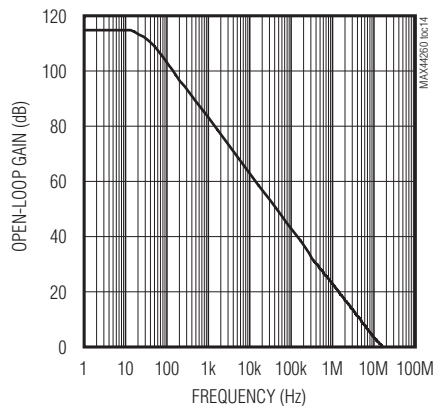
### Typical Operating Characteristics (continued)

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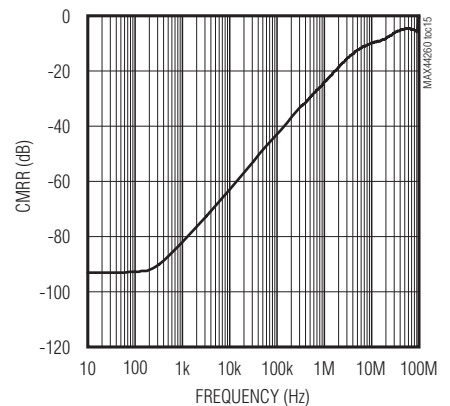
**SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE**  
( $V_{SHDN} = V_{EE}$ )



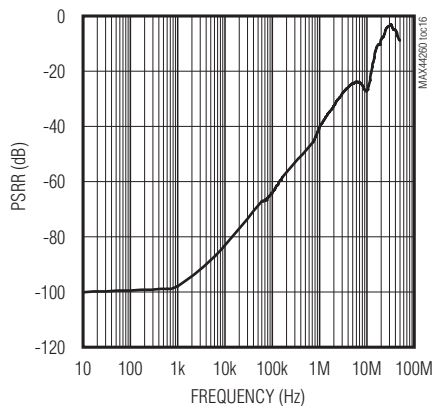
**OPEN-LOOP GAIN vs. FREQUENCY**



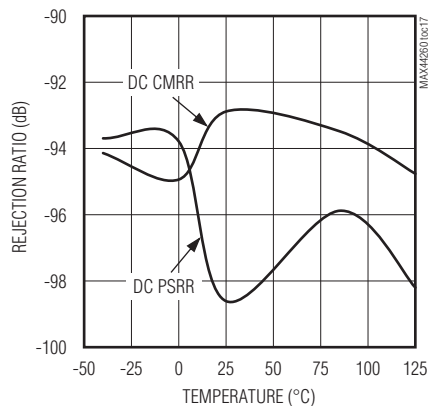
**COMMON-MODE REJECTION RATIO vs. FREQUENCY**



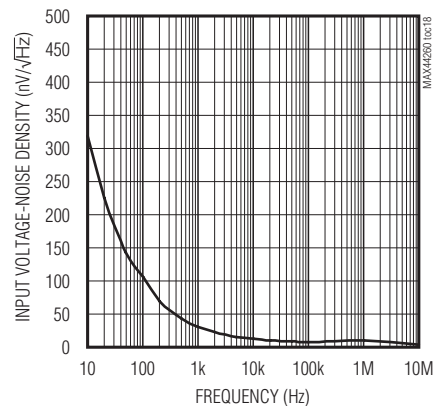
**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY**



**DC CMRR AND PSRR vs. TEMPERATURE**



**INPUT VOLTAGE-NOISE DENSITY vs. FREQUENCY**



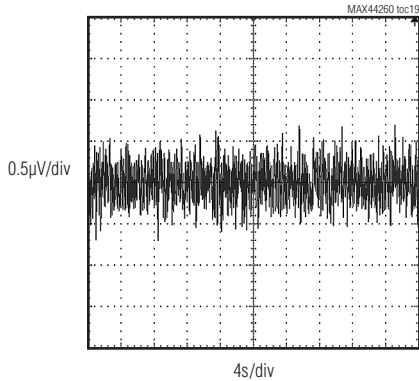
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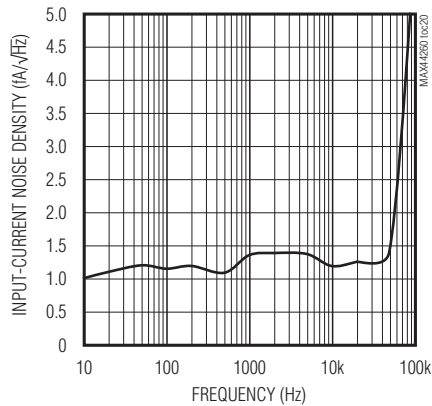
### Typical Operating Characteristics (continued)

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{CAL} = V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. All devices are 100% production tested at  $T_A = +25^\circ C$ . Temperature limits are guaranteed by design.)

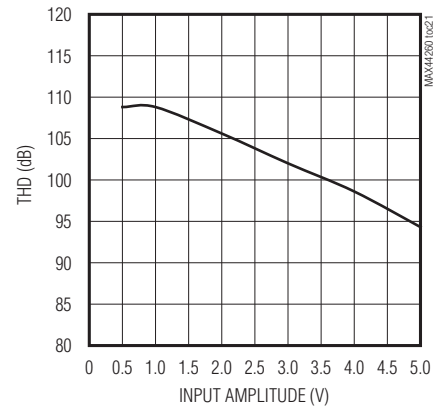
**0.1Hz TO 10Hz OUTPUT-VOLTAGE NOISE**



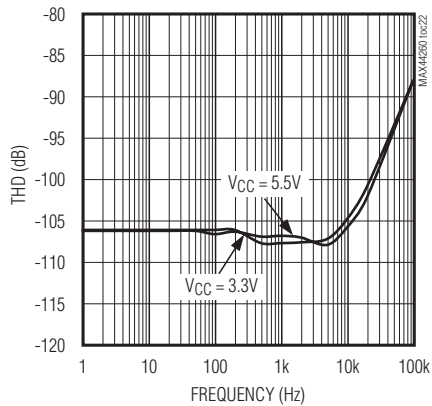
**INPUT CURRENT-NOISE DENSITY vs. FREQUENCY**



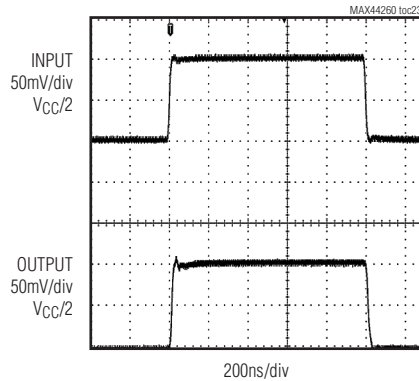
**TOTAL HARMONIC DISTORTION vs. INPUT AMPLITUDE**  
( $f = 10kHz$ ,  $V_{CC} = 5.5V$ ,  $A_v = 1V/V$ )



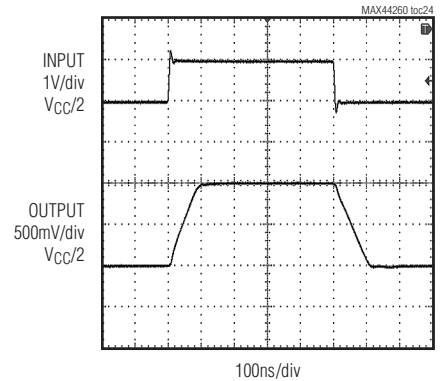
**TOTAL HARMONIC DISTORTION vs. FREQUENCY ( $V_{IN} = 2VP-P$ )**



**SMALL-SIGNAL TRANSIENT RESPONSE**



**LARGE-SIGNAL TRANSIENT RESPONSE**

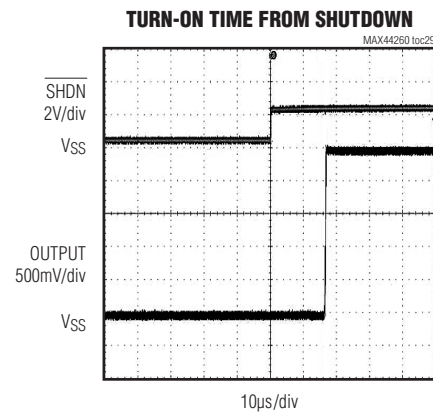
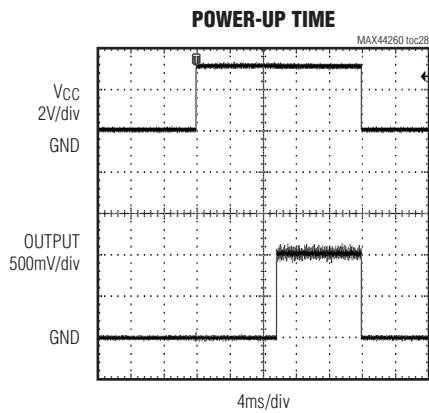
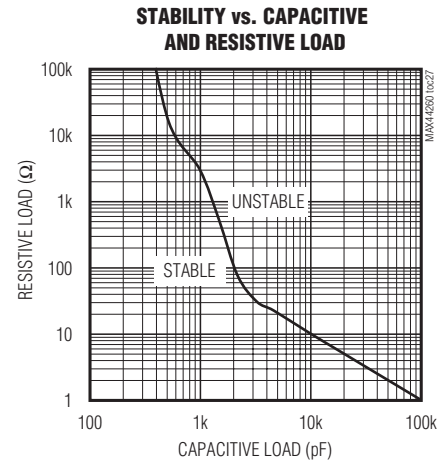
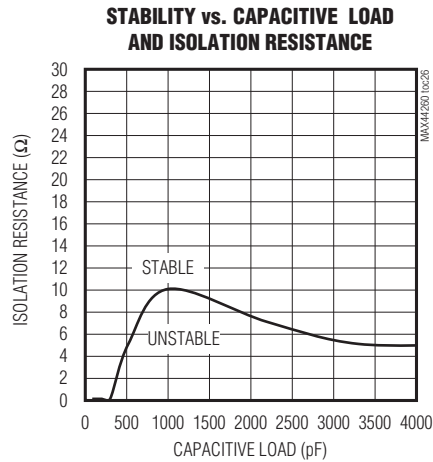
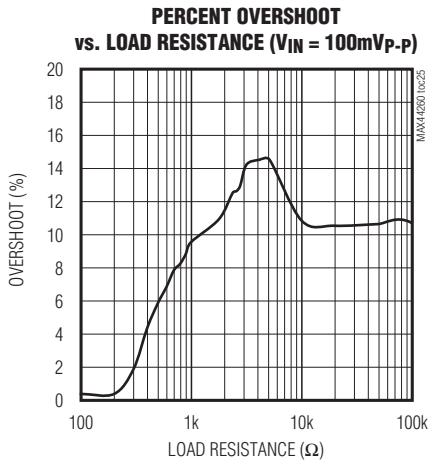


# MAX44260/MAX44261/MAX44263

## 1.8V, 15MHz Low-Offset, Low-Power, Rail-to-Rail I/O Op Amps

### Typical Operating Characteristics (continued)

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{CAL} = V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. All devices are 100% production tested at  $T_A = +25^\circ C$ . Temperature limits are guaranteed by design.)

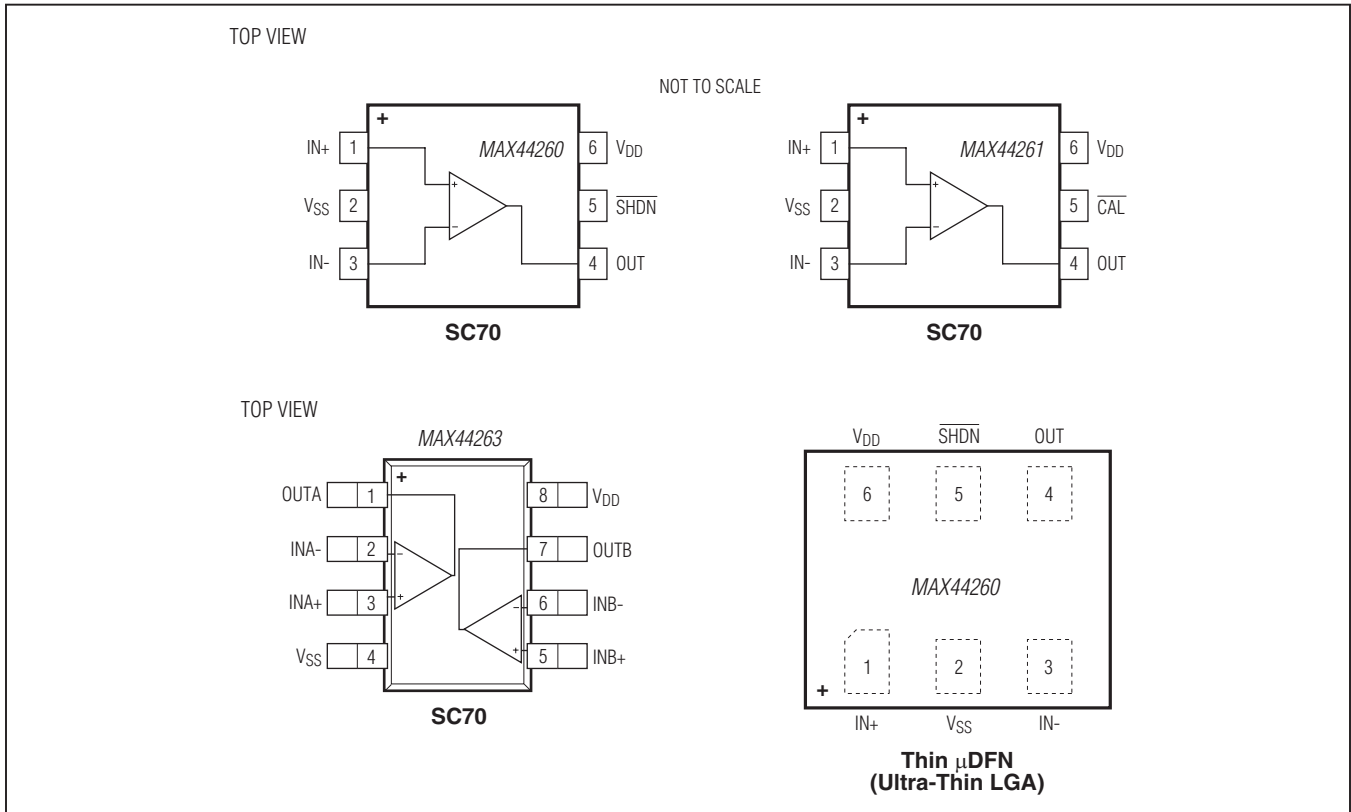




# MAX44260/MAX44261/MAX44263

## 1.8V, 15MHz Low-Offset, Low-Power, Rail-to-Rail I/O Op Amps

### Pin Configurations



### Pin Description

PIN			NAME	FUNCTION
MAX44260	MAX44261	MAX44263		
1	1	—	IN+	Positive Input
2	2	4	V <sub>SS</sub>	Negative Power Supply. Bypass with a 0.1μF capacitor to ground.
3	3	—	IN-	Negative Input
4	4	—	OUT	Output
—	5	—	$\overline{\text{CAL}}$	Active-Low Calibrate Input
5	—	—	$\overline{\text{SHDN}}$	Active-Low Shutdown
6	6	8	V <sub>DD</sub>	Positive Power Supply. Bypass with a 0.1μF capacitor to ground.
—	—	1	OUTA	Channel A Output
—	—	2	INA-	Channel A Negative Input
—	—	3	INA+	Channel A Positive Input
—	—	5	INB+	Channel B Positive Input
—	—	6	INB-	Channel B Negative Input
—	—	7	OUTB	Channel B Output

# MAX44260/MAX44261/MAX44263

## 1.8V, 15MHz Low-Offset, Low-Power, Rail-to-Rail I/O Op Amps

### Detailed Description

The MAX44260/MAX44261/MAX44263 are high-speed low-power op amps ideal for signal processing applications due to the device's high precision and low-noise CMOS inputs. The devices self-calibrate on power-up to eliminate effects of temperature and power-supply variation.

The MAX44260 also features a low-power shutdown mode that greatly reduces quiescent current while the device is not operational and recovers in 30 $\mu$ s.

The MAX44261 features a user-selectable self-calibration input that shuts down the device and allows it to be recalibrated at any time. The calibration routine takes 10ms.

### Crossover Distortion

These op amps feature a low-noise integrated charge pump that creates an internal voltage rail 1V above  $V_{DD}$ , which is used to power the input differential pair of PMOS transistors as shown in [Figure 1](#). Such a unique architecture eliminates crossover distortion common in traditional CMOS input architecture ([Figure 2](#)), especially when used in a noninverting configuration, such as for Sallen-Key filters.

The charge pump's operating frequency lies well above the unity-gain frequency of the amplifier. Thanks to its high-frequency operation and ultra-quiet circuitry, the charge pump generates little noise, does not require external components, and is entirely transparent to the user.

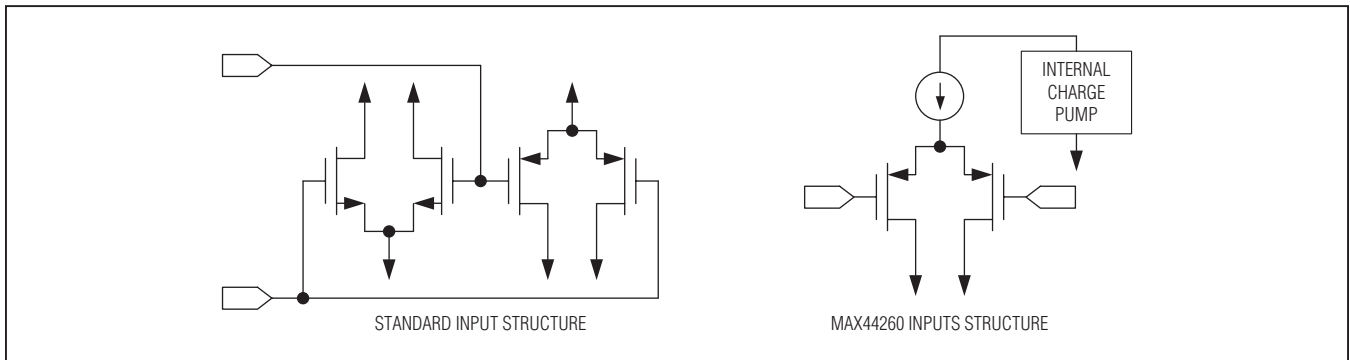


Figure 1. Comparing the Input Structure of the MAX44260 to Standard Op-Amp Inputs

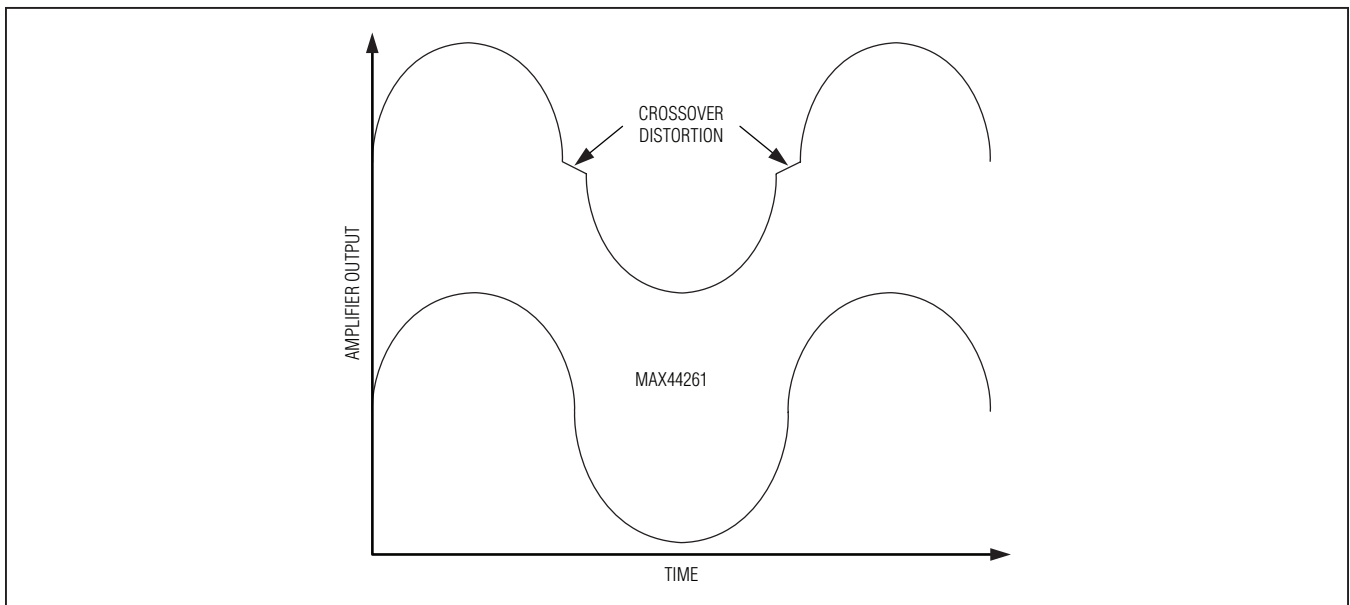


Figure 2. Crossover Distortion of Typical Amplifiers

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### Applications Information

#### Power-Up Autotrim

The ICs feature an automatic trim that self-calibrates the  $V_{OS}$  of these devices to less than  $50\mu\text{V}$  of input offset voltage on power-up. This self-calibration feature allows the device to eliminate input offset voltage effects due to power supply and operating temperature variation simply by cycling its power. The autotrim sequence takes approximately 10ms to complete and is triggered by an internal power-on-reset (POR) circuitry. During this time, the inputs and outputs are put into high impedance and left unconnected. The MAX44261 can also be forced into a self-calibration cycle by pulling the  $\overline{\text{CAL}}$  input low for  $1\mu\text{s}$ . This input also puts the part into shutdown mode.

#### Shutdown Operation

The MAX44260 features an active-low shutdown mode that puts both inputs and outputs into high impedance and substantially lowers the quiescent current to less than  $1\mu\text{A}$ . Putting the output into high impedance allows multiple outputs to be multiplexed onto a single output line without the additional external buffers. The device does not self-calibrate when exiting shutdown mode

and retains its power-up trim settings. [Figure 3](#) shows that the device also recovers from shutdown in under  $30\mu\text{s}$ .

The MAX44261 features a recalibrate input that acts the same as the shutdown mode of the MAX44260. However, when the input is pulled low, the device goes through a self-calibration sequence again ([Figure 3](#)).

The shutdown logic levels of the devices are independent of supply, allowing the shutdown feature of the device to operate off of a 1.8V or 3.3V microcontroller, regardless of supply voltage.

#### Rail-to-Rail Input/Output

The input voltage range of the ICs extends  $100\text{mV}$  above  $V_{DD}$  and below  $V_{SS}$ . The wide input common-mode voltage range allows the op amp to be used as a buffer and as a differential amplifier in a wide-variety of signal processing applications. Output voltage high/low is designed to be only  $50\text{mV}$  above  $V_{SS}$  and below  $V_{DD}$  allowing maximum dynamic range in single-supply applications. The high output current and capacitance drive capability of the devices make them ideal as an ADC driver and a line driver.

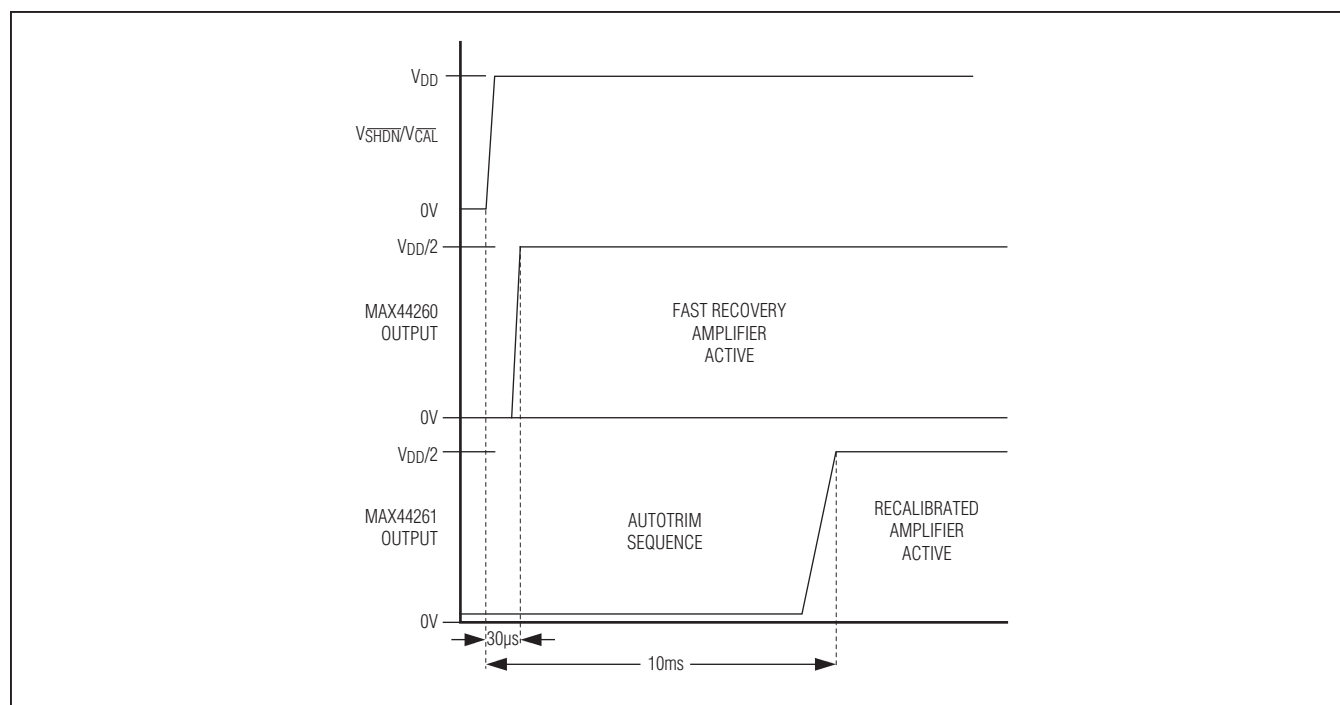


Figure 3.  $\overline{\text{CAL}}$  vs.  $\overline{\text{SHDN}}$  Input Operation

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### Input Bias Current

The ICs feature a high-impedance CMOS input stage and a specialized ESD structure that allows low-input bias current operation at low-input, common-mode voltages. Low-input bias current is useful when interfacing with high-ohmic sensors. It is also beneficial for designing transimpedance amplifiers for photodiode sensors. This makes these devices ideal for ground-referenced medical and industrial sensor applications.

### Active Filters

The MAX44260/MAX44261/MAX44263 are ideal for a wide variety of active filter circuits that make use of their wide bandwidth, rail-to-rail input/output stages and high-impedance CMOS inputs. The [Typical Application Circuit](#) shows an example Sallen-Key active filter circuit with a corner frequency of 10kHz. At low frequencies, the amplifier behaves like a simple low-distortion noninverting buffer, while its high bandwidth gives excellent stopband attenuation above its corner frequency. See the [Typical Application Circuit](#).

### Chip Information

PROCESS: BiCMOS

### Driver for Interfacing with the MAX11645 ADC

The ICs' tiny size and low noise makes them a good fit for driving 12- to 16-bit resolution ADCs in space-constrained applications. The [Typical Application Circuit](#) shows the MAX44260 amplifier output connected to a lowpass filter driving the MAX11645 ADC. The MAX11645 is part of a family of 3V and 5V, 12-bit and 10-bit, 2-channel ADCs.

The MAX11645 offers sample rates up to 94ksps and measures two single-ended inputs or one differential input. These ADCs dissipate 670 $\mu$ A at the maximum sampling rate, but just 6 $\mu$ A at 1ksps and 0.5 $\mu$ A in shut-down. Offered in the ultra-tiny, 1.9mm x 2.2mm WLP and  $\mu$ MAX-8 packages, the MAX11645 ADCs are an ideal fit to pair with the MAX44260/MAX44261/MAX44263 amplifiers in portable applications.

Where higher resolution is required, refer to the MAX1069 (14-bit) and MAX1169 (16-bit) ADC families.

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX44260AXT+	-40°C to +125°C	6 SC70	+AEB
MAX44260AYT+	-40°C to +125°C	6 Thin $\mu$ DFN (Ultra-Thin LGA)	+AY
MAX44261AXT+	-40°C to +125°C	6 SC70	+AEC
MAX44263AXA+	-40°C to +125°C	8 SC70	+AAG

+Denotes a lead(Pb)-free/RoHS-compliant package.

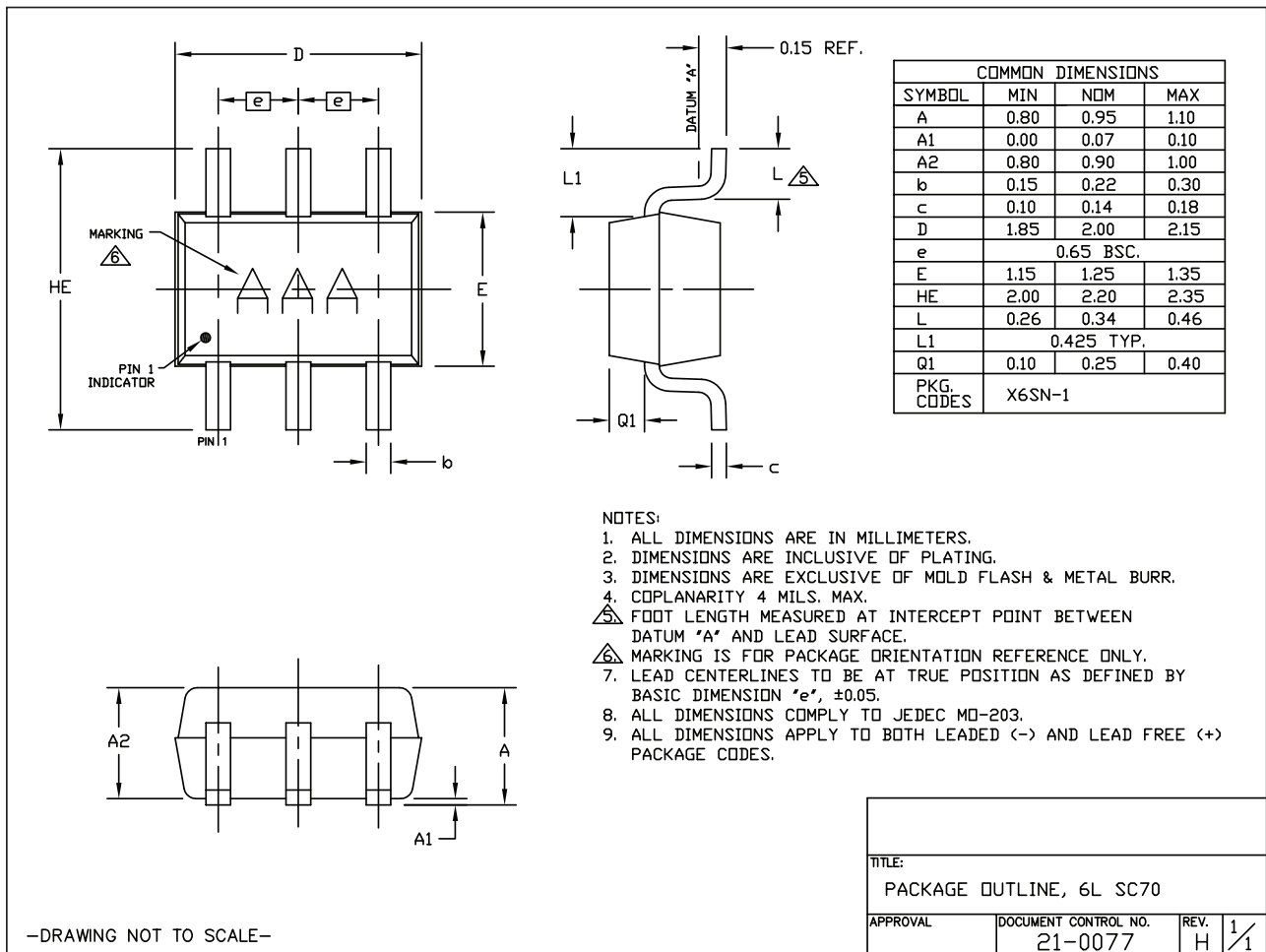
# MAX44260/MAX44261/MAX44263

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### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 SC70	X6SN+1	<a href="#">21-0077</a>	<a href="#">90-0189</a>
8 SC70	X8CN+1	<a href="#">21-0460</a>	<a href="#">90-0348</a>
6 Thin $\mu$ DFN (Ultra-Thin LGA)	Y61A1+1	<a href="#">21-0190</a>	<a href="#">90-0233</a>

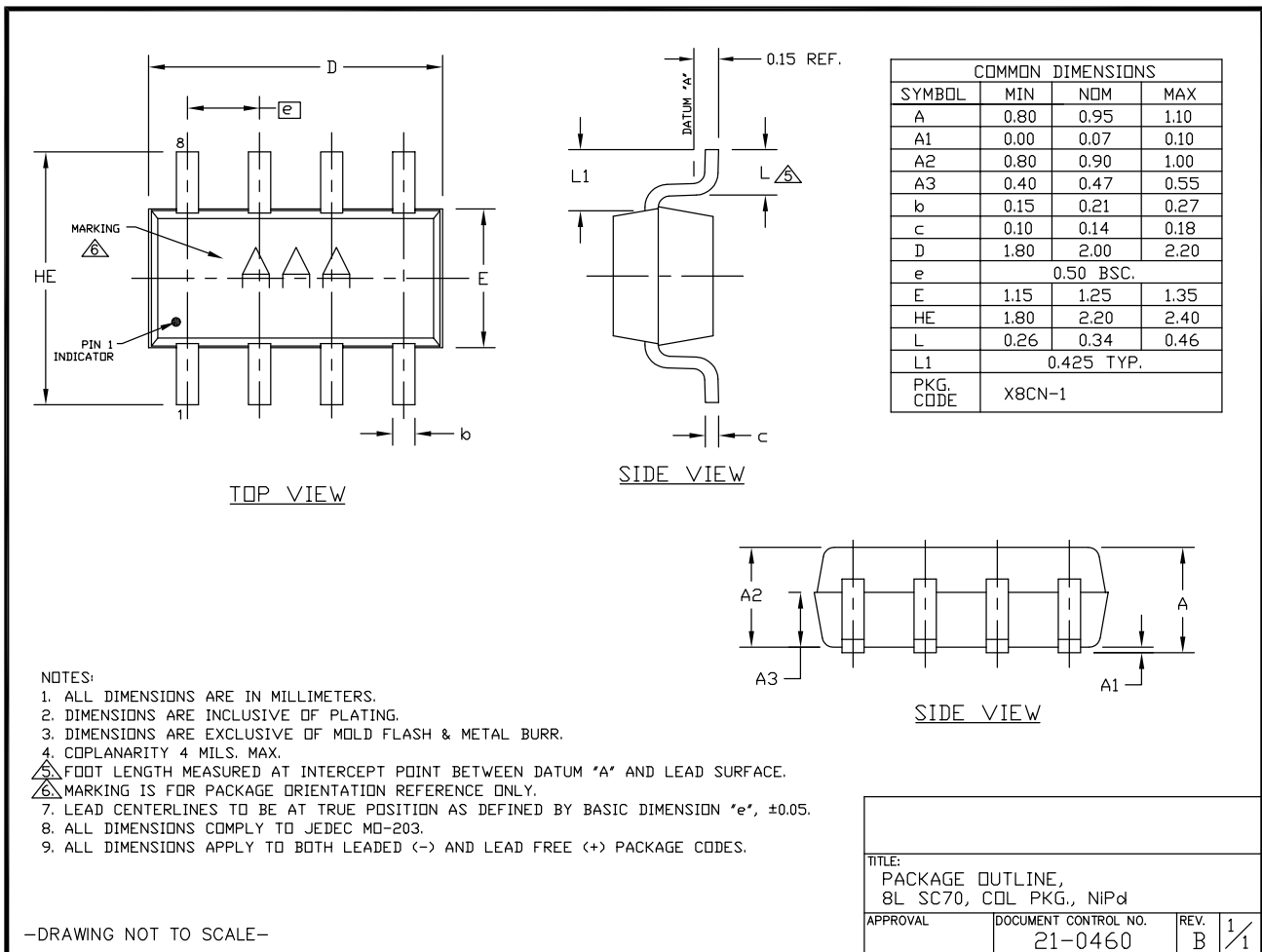


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### Package Information (continued)

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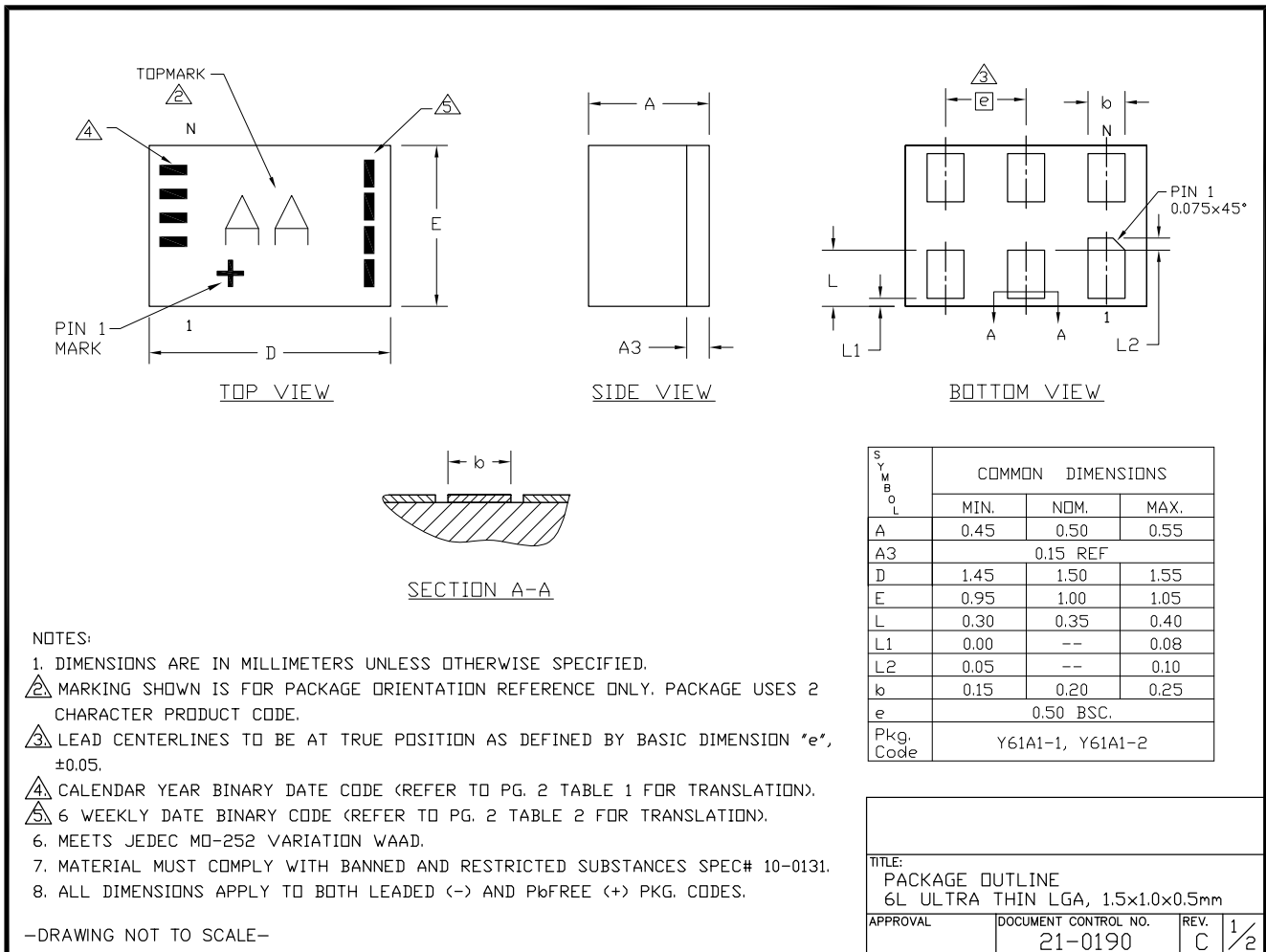


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### Package Information (continued)

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### Package Information (continued)

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**TABLE 1** Translation Table for Calendar Year Code

Calendar Year	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
	□	□	□	■	□	□	■	□	■	■
	□	□	■	□	□	■	□	■	□	□
	□	■	□	□	■	□	□	■	■	■
	■	□	□	□	■	■	■	□	□	□

Legend:  Marked with bar      Blank space - no bar required

**TABLE 2** Translation Table for Payweek Binary Coding

Payweek	06-11	12-17	18-23	24-29	30-35	36-41	42-47	48-51	52-05
	□	□	□	■	□	□	■	□	■
	□	□	■	□	□	■	□	■	□
	□	■	□	□	■	□	□	■	■
	■	□	□	□	■	■	■	□	□

Legend:  Marked with bar      Blank space - no bar required

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE 6L ULTRA THIN LGA, 1.5x1.0x0.5mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0190	REV. C	2/2



# MAX44260/MAX44261/MAX44263

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### Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	8/11	Added thin $\mu$ DFN (ultra-thin LGA) package and updated slew rate and TOC 29	1, 2, 3, 8, 9, 12
2	10/11	Removed future product information from data sheet	12
3	2/12	Revised <i>Electrical Characteristics</i> and the <i>Power-Up Autotrim</i> section	2, 3, 11
4	7/12	Revised <i>Electrical Characteristics</i> and <i>Typical Operating Characteristics</i>	3, 6
5	10/12	Added the MAX44263 and revised the <i>Electrical Characteristics</i> , <i>Pin Description</i> , and <i>Pin Configuration</i> .	1–17



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