

MC100EPT26

3.3V 1:2 Fanout Differential LVPECL/LVDS to LVTTTL Translator

Description

The MC100EPT26 is a 1:2 Fanout Differential LVPECL/LVDS to LVTTTL translator. Because LVPECL (Positive ECL) or LVDS levels are used only +3.3 V and ground are required. The small outline 8-lead package and the 1:2 fanout design of the EPT26 makes it ideal for applications which require the low skew duplication of a signal in a tightly packed PC board.

The V_{BB} output allows the EPT26 to be used in a single-ended input mode. In this mode the V_{BB} output is tied to the $\overline{D0}$ input for a non-inverting buffer or the D0 input for an inverting buffer. If used, the V_{BB} pin should be bypassed to ground with $> 0.01 \mu\text{F}$ capacitor. For a single-ended direct connection, use an external voltage reference source such as a resistor divider. Do not use V_{BB} for a single-ended direct connection or port to another device.

Features

- 1.4 ns Typical Propagation Delay
- Maximum Frequency > 275 MHz Typical
- The 100 Series Contains Temperature Compensation
- Operating Range: $V_{CC} = 3.0$ V to 3.6 V with $GND = 0$ V
- 24 mA TTL outputs
- Q Outputs Will Default LOW with Inputs Open or at V_{EE}
- V_{BB} Output
- Pb-Free Packages are Available



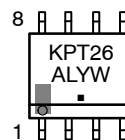
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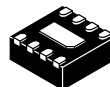
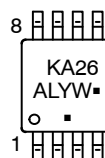
MARKING DIAGRAMS*



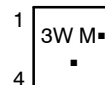
SO-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



DFN8
MN SUFFIX
CASE 506AA



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M = Date Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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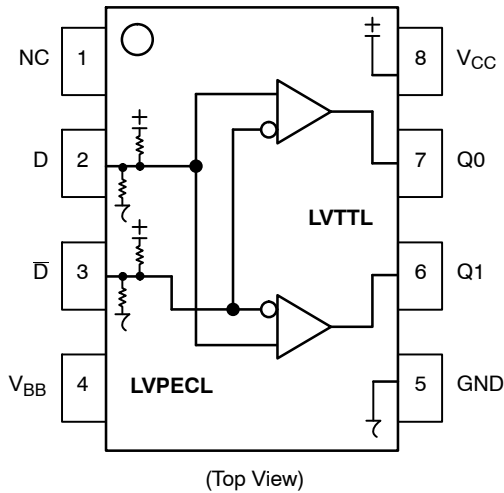


Figure 1. 8-Lead Pinout and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
Q0, Q1	LVTTTL Outputs
D0**, D1**	Differential LVPECL Inputs Pair
V _{CC}	Positive Supply
V _{BB}	Output Reference Voltage
GND	Ground
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

** Pins will default to V_{CC}/2 when left open.

Table 2. ATTRIBUTES

Characteristics	Value	
Internal Input Pulldown Resistor	50 kΩ	
Internal Input Pullup Resistor	50 kΩ	
ESD Protection	Human Body Model	> 1.5 kV
	Machine Model	> 100 V
	Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg
	SO-8	Level 1
	TSSOP-8	Level 1
	DFN8	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	117 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

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Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V		3.8	V
V _{IN}	Input Voltage	GND = 0 V	V _I ≤ V _{CC}	0 to 3.8	V
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfp 500 lfp	SOIC-8 SOIC-8	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfp 500 lfp	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfp 500 lfp	DFN8 DFN8	129 84	°C/W °C/W
T _{sol}	Wave Solder	Pb Pb-Free		265 265	°C
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

Table 4. PECL INPUT DC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0.0 V (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V _{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V _{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)	1.2		3.3	1.2		3.3	1.2		3.3	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	D D̄	-150 -150		-150 -150			-150 -150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfp. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input parameters vary 1:1 with V_{CC}.

4. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 5. TTL OUTPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $GND = 0.0\text{ V}$; $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.0\text{ mA}$	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 24\text{ mA}$			0.5	V
I_{CCH}	Power Supply Current		10	25	35	mA
I_{CCL}	Power Supply Current		15	34	40	mA
I_{OS}	Output Short Circuit Current		-50		-150	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. AC CHARACTERISTICS $V_{CC} = 3.0\text{ V}$ to 3.6 V ; $GND = 0.0\text{ V}$ (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (Figure 2)	275	350		275	350		275	350		MHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential (Note 6)	1.2 1.2	1.5 1.5	2.0 1.8	1.2 1.2	1.5 1.5	2.0 1.8	1.3 1.2	1.7 1.5	2.2 1.8	ns
t_{SK+} + t_{SK-} - t_{SKPP}	Within Device Skew++ Within Device Skew-- Device-to-Device Skew (Note 7)		15 20 100	60 85 500		15 20 100	60 85 500		20 30 100	85 85 500	ps
t_{JITTER}	Random Clock Jitter (RMS) (Figure 2) @ $\leq 200\text{ MHz}$ @ $> 200\text{ MHz}$		6 20	30 275		6 40	30 275		6 170	30 275	ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (0.8V – 2.0V) Q, \bar{Q}	330	600	950	330	600	950	330	650	950	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Measured with a 750 mV 50% duty-cycle clock source. $R_L = 500\ \Omega$ to GND and $C_L = 20\text{ pF}$ to GND. Refer to Figure 3.

6. Reference ($V_{CC} = 3.3\text{ V} \pm 5\%$; $GND = 0\text{ V}$)

7. Skews are measured between outputs under identical transitions.

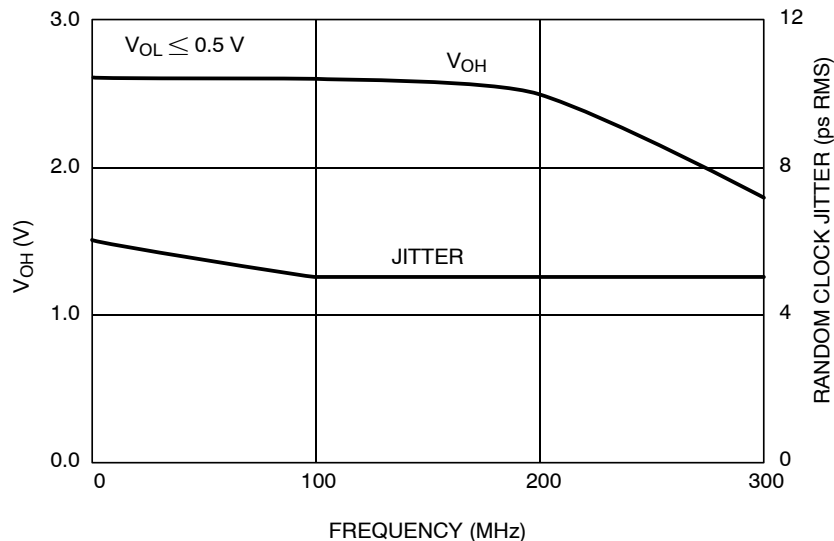


Figure 2. Typical V_{OH} / Jitter versus Frequency (25°C)

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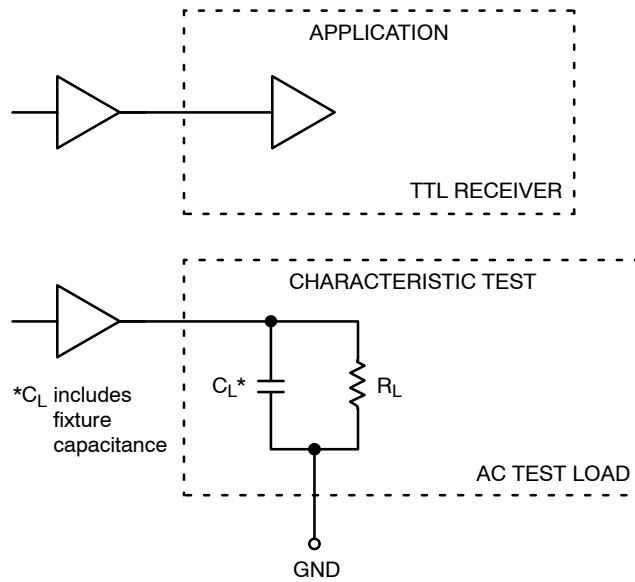


Figure 3. TTL Output Loading Used for Device Evaluation

ORDERING INFORMATION

Device	Package	Shipping [†]
MC100EPT26D	SOIC-8	98 Units / Rail
MC100EPT26DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100EPT26DR2	SOIC-8	2500 / Tape & Reel
MC100EPT26DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100EPT26DT	TSSOP-8	100 Units / Rail
MC100EPT26DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100EPT26DTR2	TSSOP-8	2500 / Tape & Reel
MC100EPT26DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100EPT26MNR4	DFN8	1000 / Tape & Reel
MC100EPT26MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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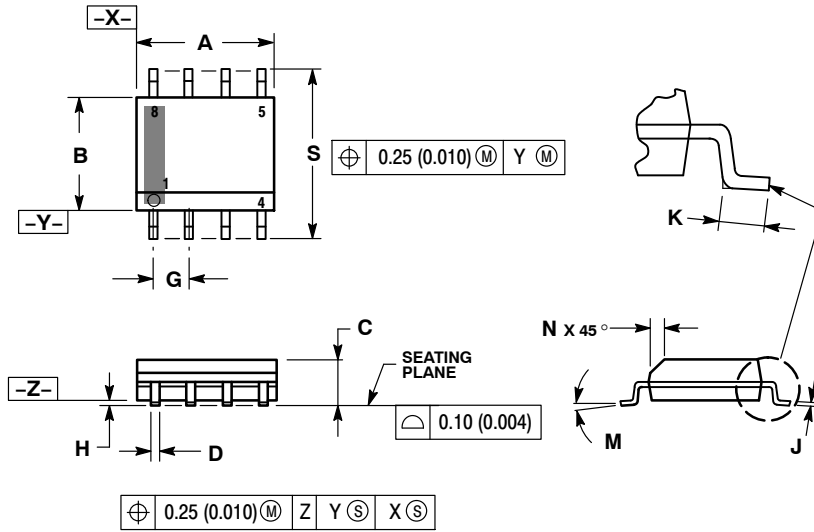
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AJ

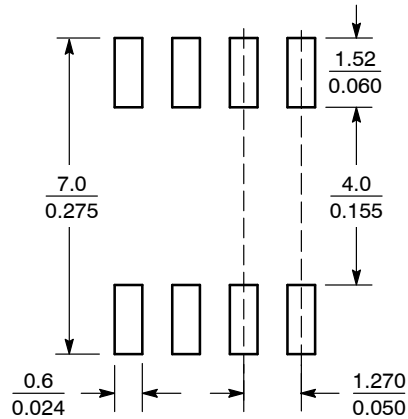


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



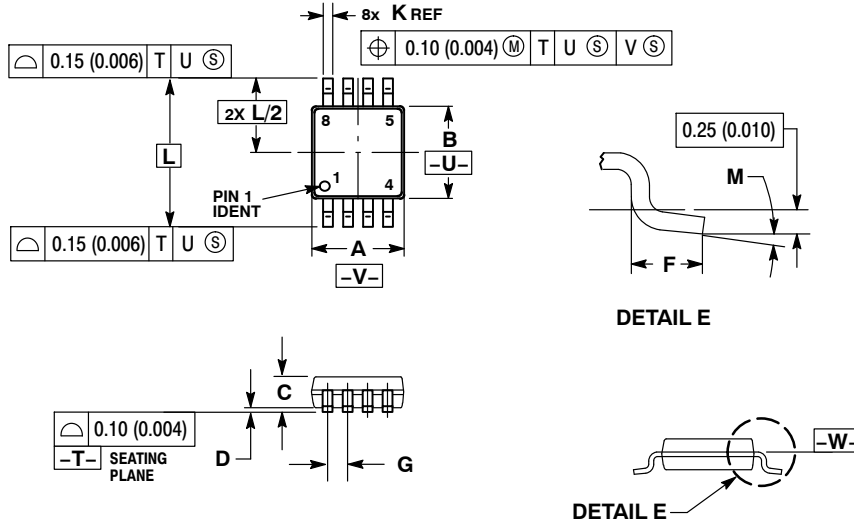
SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R-02
ISSUE A



NOTES:

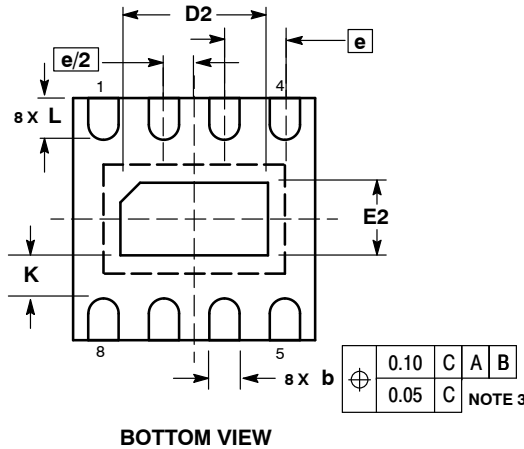
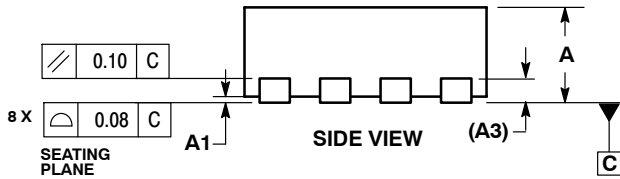
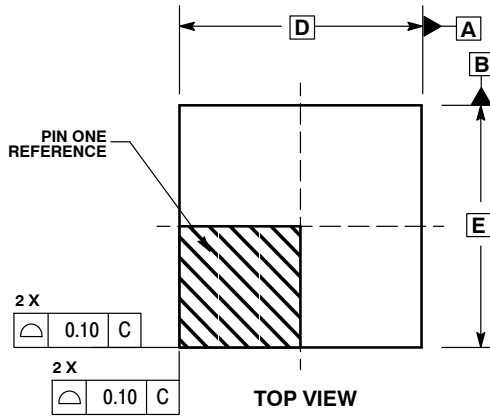
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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PACKAGE DIMENSIONS

DFN8
CASE 506AA-01
ISSUE D




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	---
L	0.25	0.35

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