- **Low Supply-Voltage Range, 1.8 V to 3.6 V**
- **Ultra-Low Power Consumption:**
  - **Active Mode: 200 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.7 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Ultra-Fast Wake-Up From Standby Mode in Less Than 1 μs**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to ±1%**
  - **Internal Very Low Power LF Oscillator**
  - **32-kHz Crystal**
  - **High-Frequency Crystal up to 16 MHz**
  - **Resonator**
  - **External Digital Clock Source**
  - **External Resistor**
- **16-Bit Timer0_A3 With Three Capture/Compare Registers**
- **16-Bit Timer1_A2 With Two Capture/Compare Registers**
- **On-Chip Comparator for Analog Signal Compare Function or Slope Analog-to-Digital (A/D) Conversion**
- **10-Bit 200-ksps A/D Converter With Internal Reference, Sample-and-Hold, Autoscan, and Data Transfer Controller**
- **Universal Serial Communication Interface**
  - **Enhanced UART Supporting Auto Baudrate Detection (LIN)**
  - **IrDA Encoder and Decoder**
  - **Synchronous SPI**
  - **I²C™**
- **Brownout Detector**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **Bootstrap Loader in Flash Devices**
- **On-Chip Emulation Module**
- **Family Members Include:**
  MSP430F2132
  8KB + 256B Flash Memory
  512B RAM
  MSP430F2122
  4KB + 256B Flash Memory
  512B RAM
  MSP430F2112
  2kB + 256B Flash Memory
  256B RAM
- **Available in 28-Pin TSSOP and 32-Pin QFN Packages (See Available Options)**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* (Literature Number SLAU144)**

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description

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μs.

The MSP430F21x2 series is an ultra-low-power microcontroller with two built-in 16-bit timers, a fast 10-bit A/D converter with integrated reference and a data transfer controller (DTC), a comparator, built-in communication capability using the universal serial communication interface, and up to 24 I/O pins.

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AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC 28-PIN TSSOP (PW)	PLASTIC 32-PIN QFN (RHB)
–40°C to 85°C	MSP430F2112IPW	MSP430F2112IRHB
	MSP430F2122IPW	MSP430F2122IRHB
	MSP430F2132IPW	MSP430F2132IRHB
–40°C to 105°C	MSP430F2112TPW	MSP430F2112TRHB
	MSP430F2122TPW	MSP430F2122TRHB
	MSP430F2132TPW	MSP430F2132TRHB

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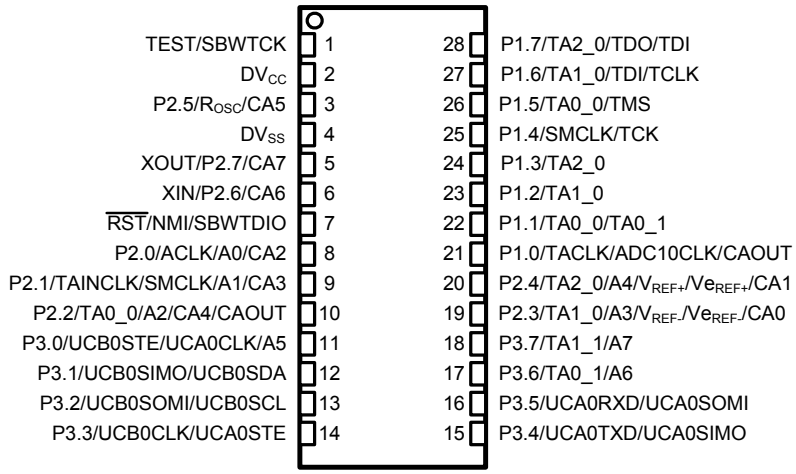
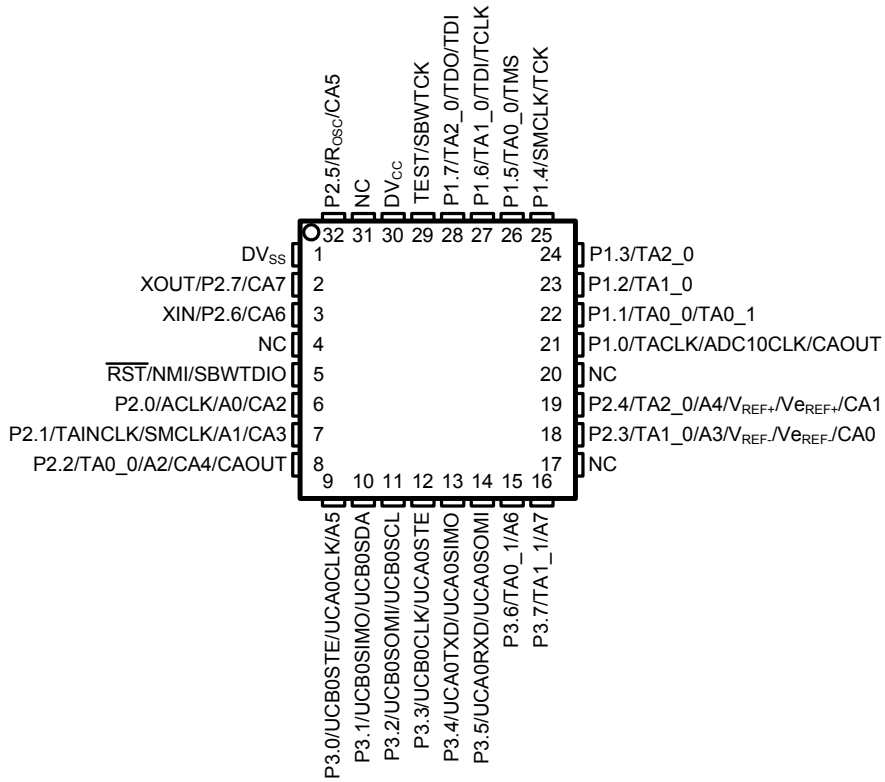
pin designation, PW package



pin designation, RHB package



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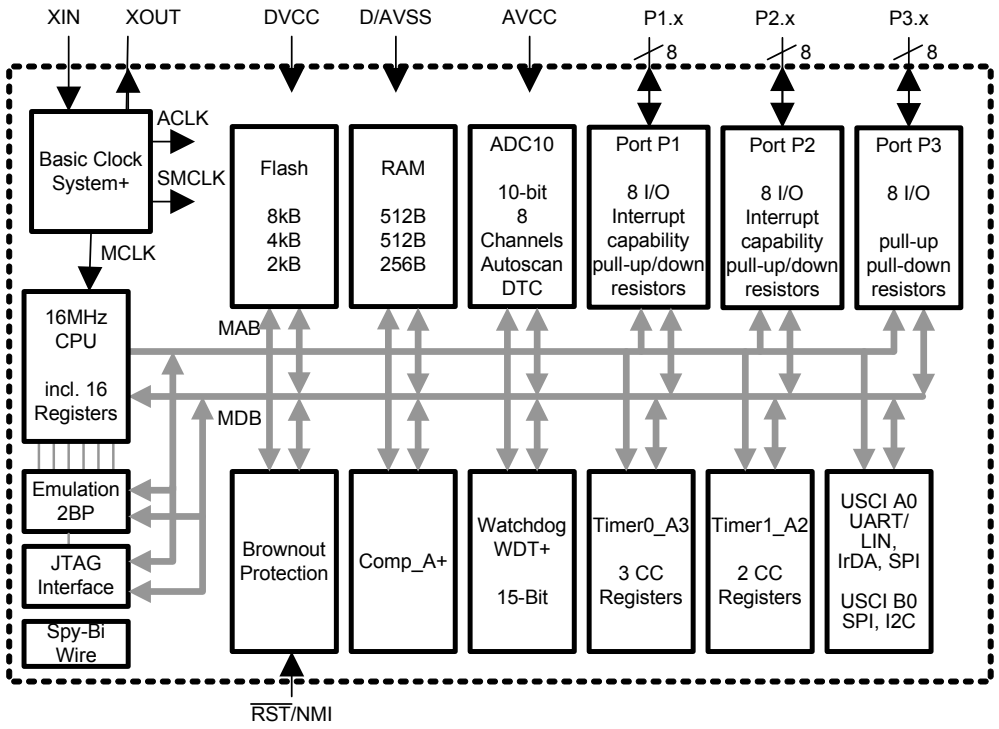
functional block diagram



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Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	28-PIN PW	32-PIN RHB		
P1.0/ TACLK/ ADC10CLK/ CAOUT	21	21	I/O	General-purpose digital I/O Timer0_A3, clock signal TACLK input Timer1_A2, clock signal TACLK input ADC10, conversion clock Comparator_A+ output
P1.1/ TA0_0/ TA0_1	22	22	I/O	General-purpose digital I/O Timer0_A3, capture: CCI0A input, compare: Out0_0 output Timer1_A2, capture: CCI0A input
P1.2/ TA1_0	23	23	I/O	General-purpose digital I/O Timer0_A3, capture: CCI1A input, compare: Out1_0 output
P1.3/ TA2_0	24	24	I/O	General-purpose digital I/O Timer0_A3, capture: CCI2A input, compare: Out2_0 output
P1.4/ SMCLK/ TCK	25	25	I/O	General-purpose digital I/O SMCLK signal output Test Clock input for device programming and test
P1.5/ TA0_0 /TMS	26	26	I/O	General-purpose digital I/O Timer0_A3, compare: Out0_0 output JTAG test mode select, input terminal for device programming and test
P1.6/ TA1_0/ TDI/TCLK	27	27	I/O	General-purpose digital I/O Timer0_A3, compare: Out1_0 output JTAG test data input or test clock input in programming and test
P1.7/ TA2_0/ TDO/TDI	28	28	I/O	General-purpose digital I/O Timer0_A3, compare: Out2_0 output JTAG test data output terminal or test data input in programming and test
P2.0/ ACLK/ A0/ CA2	8	6	I/O	General-purpose digital I/O ACLK signal output ADC10 analog input A0 Comparator_A+ input
P2.1/ TAINCLK/ SMCLK/ A1/ CA3	9	7	I/O	General-purpose digital I/O SMCLK signal output Timer0_A3, clock signal TACLK input Timer1_A2, clock signal TACLK input ADC10 analog input A1 Comparator_A+ input
P2.2/ TA0_0/ A2/ CA4/ CAOUT	10	8	I/O	General-purpose digital I/O Timer0_A3, capture: CCI0B input, compare: Out0_0 output ADC10 analog input A2 Comparator_A+ input Comparator_A+ output
P2.3/ TA1_0/ A3/ V_{REF-}/Ve_{REF-}/ CA0	19	18	I/O	General-purpose digital I/O Timer0_A3, compare: Out1_0 output ADC10 analog input A3 Negative reference Comparator_A+ input
P2.4/ TA2_0/ A4/ V_{REF+}/Ve_{REF+}/ CA1	20	19	I/O	General-purpose digital I/O Timer0_A3, compare: Out2_0 output ADC10 analog input A4 Positive reference Comparator_A+ input

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Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	28-PIN PW	32-PIN RHB		
XIN/ P2.6/ CA6	6	3	I/O	Input terminal of crystal oscillator General-purpose digital I/O Comparator_A+ input
XOUT/ P2.7/ CA7	5	2	I/O	Output terminal of crystal oscillator General-purpose digital I/O Comparator_A+ input
P3.0/ UCB0STE/ UCA0CLK/A5	11	9	I/O	General-purpose digital I/O USCI_B0 slave transmit enable/USCI_A0 clock input/output ADC10 analog input A5
P3.1/ UCB0SIMO/UCB0SDA	12	10	I/O	General-purpose digital I/O USCI_B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P3.2/ UCB0SOMI/UCB0SCL	13	11	I/O	General-purpose digital I/O USCI_B0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P3.3/ UCB0CLK/UCA0STE	14	12	I/O	General-purpose digital I/O USCI_B0 clock input/output, USCI_A0 slave transmit enable
P3.4/ UCA0TXD/UCA0SIMO	15	13	I/O	General-purpose digital I/O USCI_A0 transmit data output in UART mode, slave data in/master out in SPI mode
P3.5/ UCA0RXD/UCA0SOMI	16	14	I/O	General-purpose digital I/O USCI_A0 receive data input in UART mode, slave data out/master in in SPI mode
P3.6/ TA0_1/ A6	17	15	I/O	General-purpose digital I/O Timer1_A2, capture: CCI0B input, compare: Out0_1 output ADC10 analog input A6
P3.7/ TA1_1/ A7	18	16	I/O	General-purpose digital I/O Timer1_A2, capture: CCI1A input, compare: Out1_1 output ADC10 analog input A7
$\overline{\text{RST}}$/NMI/ SBWTDIO	7	5	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCK	1	29	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST.
P2.5/ R_{OSC}/ CA5	3	32	I/O	General-purpose digital I/O Input for external resistor defining the DCO nominal frequency Comparator_A+ input
DV_{CC}	2	30		Digital supply voltage
DV_{SS}	4	1		Digital supply voltage
NC	NA	4, 17, 20, 31		Not connected internally. Recommended connection to V_{SS}.

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	e.g., CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 --> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)--> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) --> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) --> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) --> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) --> R11 R10 + 2--> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 --> M(TONI)

NOTE: S = source, D = destination

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operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
    ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
    ACLK and SMCLK remain active, MCLK is disabled
    DCO's dc generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
    ACLK is disabled
    MCLK and SMCLK are disabled
    DCO's dc generator is disabled
    Crystal oscillator is stopped

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interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0xFFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. If the reset vector (0xFFFE) contains 0xFFFF (e.g., flash is not programmed), the CPU enters LPM4 after power–up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Flash key violation PC out of range (see Note 1)	PORIFG RSTIFG WDTIFG KEYV (see Note 2)	reset	0xFFFE	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (see Notes 2 and 6)	(non)maskable (non)maskable (non)maskable	0xFFFC	30
Timer1_A2	TA1CCR0 CCIFG (see Note 3)	maskable	0xFFFA	29
Timer1_A2	TA1CCR1 CCIFG, TA1CTL TAIFG (see Notes 2 and 3)	maskable	0xFFF8	28
Comparator_A+	CAIFG	maskable	0xFFF6	27
Watchdog timer	WDTIFG	maskable	0xFFF4	26
Timer0_A3	TA0CCR0 CCIFG (see Note 3)	maskable	0xFFF2	25
Timer0_A3	TA0CCR1 CCIFG, TA0CCR2 CCIFG, TA0CTL TAIFG (see Notes 2 and 3)	maskable	0xFFF0	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG (see Note 2 and 4)	Maskable	0xFFEE	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive / transmit	UCA0TXIFG, UCB0TXIFG (see Note 2 and 5)	Maskable	0xFFEC	22
ADC10	ADC10IFG (see Note 3)	maskable	0xFFEA	21
			0xFFE8	20
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7 (see Notes 2 and 3)	maskable	0xFFE6	19
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 2 and 3)	maskable	0xFFE4	18
			0xFFE2	17
			0xFFE0	16
See Note 7			0xFFDE	15
See Note 8			0xFFDC to 0xFFC0	14 to 0, lowest

NOTES:
1. A reset is executed if the CPU tries to fetch instructions from within the module register memory address range (0x0000 to 0x01FF).
2. Multiple source flags.
3. Interrupt flags are located in the module.
4. In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, and UCSTPIFG.
5. In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, and UCB0TXIFG.
6. Non–maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot.
7. This location is used as bootstrap loader security key (BSLSKEY).
   A 0xAA55 at this location disables the BSL completely.
   A zero (0h) disables the erasure of the flash if an invalid password is supplied.
8. The interrupt vectors at addresses 0xFFDC to 0xFFC0 are not used in this device and can be used for regular program code if necessary.

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special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.

OFIE Oscillator fault enable

NMIIE (Non)maskable interrupt enable

ACCVIE Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0

UCA0RXIE USCI_A0 receive-interrupt enable

UCA0TXIE USCI_A0 transmit-interrupt enable

UCB0RXIE USCI_B0 receive-interrupt enable

UCB0TXIE USCI_B0 transmit-interrupt enable

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interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG Set on Watchdog Timer overflow or security key violation.
Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.

OFIFG Flag set on oscillator fault

PORIFG Power-on interrupt flag. Set on V_{CC} power up.

RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power up.

NMIIFG Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h					UCB0TX IFG	UCB0RX IFG	UCA0TX IFG	UCA0RX IFG
					rw-1	rw-0	rw-1	rw-0

UCA0RXIFG USCI_A0 receive-interrupt flag

UCA0TXIFG USCI_A0 transmit-interrupt flag

UCB0RXIFG USCI_B0 receive-interrupt flag

UCB0TXIFG USCI_B0 transmit-interrupt flag

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
	rw-(0,1):	Bit can be read and written. It is Reset or Set by POR.
		SFR bit is not present in device

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memory organization

		MSP430F2122	MSP430F2122	MSP430F2132
Memory Main: interrupt vector Main: code memory	Size Flash Flash	2KB 0xFFFF to 0xFFC0 0xFFFF to 0xF800	4KB 0xFFFF to 0xFFC0 0xFFFF to 0xF000	8KB 0xFFFF to 0xFFC0 0xFFFF to 0xE000
Information memory	Size Flash	256 Byte 0x10FFh to 0x1000	256 Byte 0x10FFh to 0x1000	256 Byte 0x10FFh to 0x1000
Boot memory	Size ROM	1KB 0x0FFF to 0x0C00	1KB 0x0FFF to 0x0C00	1KB 0x0FFF to 0x0C00
RAM	Size	256B 0x02FF to 0x0200	512B 0x03FF to 0x0200	512B 0x03FF to 0x0200
Peripherals	16-bit 8-bit 8-bit SFR	0x01FF to 0x0100 0x00FF to 0x0010 0x000F to 0x0000	0x01FF to 0x0100 0x00FF to 0x0010 0x000F to 0x0000	0x01FF to 0x0100 0x00FF to 0x0010 0x000F to 0x0000

bootstrap loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by a user-defined password. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader* (literature number SLAA089).

BSL FUNCTION	28-PIN PW PACKAGE PINS	32-PIN RHB PACKAGE PINS
Data rransmit	22 – P1.1	22 – P1.1
Data receive	10 – P2.2	8 – P2.2

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called information memory.
- Segment A contains calibration data. After reset segment A is protected against programming or erasing. It can be unlocked but care should be taken not to erase this segment if the calibration data is required.

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peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator, an internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal or the internal very-low-power LF oscillator
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

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calibration data stored in information memory segment A

Calibration data is stored for both the DCO and for ADC10 organized in a tag-length-value structure.

TAGS USED BY THE ADC CALIBRATION TAGS			
NAME	ADDRESS	VALUE	DESCRIPTION
TAG_DCO_30	0x10F6	0x01	DCO frequency calibration at V_{CC} = 3.0 V and T_A = 30°C at calibration
TAG_ADC10_1	0x10DA	0x10	ADC10_1 calibration tag
TAG_EMPTY	–	0xFE	Identifier for empty memory areas

LABELS USED BY THE ADC CALIBRATION TAGS			
LABEL	CONDITION AT CALIBRATION / DESCRIPTION	SIZE	ADDRESS OFFSET
CAL_ADC_25T85	INCHx = 0x1010, REF2_5 = 1, T_A = 85°C	Word	0x000E
CAL_ADC_25T30	INCHx = 0x1010, REF2_5 = 1, T_A = 30°C	Word	0x000C
CAL_ADC_25VREF_FACTOR	REF2_5 = 1, T_A = 30°C, I_{VREF+} = 1.0 mA	Word	0x000A
CAL_ADC_15T85	INCHx = 0x1010, REF2_5 = 0, T_A = 85°C	Word	0x0008
CAL_ADC_15T30	INCHx = 0x1010, REF2_5 = 0, T_A = 30°C	Word	0x0006
CAL_ADC_15VREF_FACTOR	REF2_5 = 0, T_A = 30°C, I_{VREF+} = 0.5 mA	Word	0x0004
CAL_ADC_OFFSET	External Vref = 1.5 V, $f_{ADC12CLK}$ = 5 MHz	Word	0x0002
CAL_ADC_GAIN_FACTOR	External Vref = 1.5 V, $f_{ADC12CLK}$ = 5 MHz	Word	0x0000
CAL_BC1_1MHz	–	Byte	0x0007
CAL_DCO_1MHz	–	Byte	0x0006
CAL_BC1_8MHz	–	Byte	0x0005
CAL_DCO_8MHz	–	Byte	0x0004
CAL_BC1_12MHz	–	Byte	0x0003
CAL_DCO_12MHz	–	Byte	0x0002
CAL_BC1_16MHz	–	Byte	0x0001
CAL_DCO_16MHz	–	Byte	0x0000

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brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

digital I/O

There are three 8-bit I/O ports implemented—ports P1 through P3.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

The MSP430F21x2 devices provides up to 24 total port I/O pins available externally. See the device pinout for more information.

watchdog timer + (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

ADC10

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and data transfer controller, or DTC, for automatic conversion result handling allowing ADC samples to be converted and stored without any CPU intervention.

comparator_A+

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

timer0_A3

Timer0_A3 is a 16-bit timer/counter with three capture/compare registers. Timer0_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer0_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer0_A3 SIGNAL CONNECTIONS

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
28-PIN PW	32-PIN RHB					28-PIN PW	32-PIN RHB
21 – P1.0	21 – P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
9 – P2.1	7 – P2.1	TAINCLK	INCLK				
22 – P1.1	22 – P1.1	TA0	CCI0A	CCR0	TA0	22 – P1.1	22 – P1.1
10 – P2.2	8 – P2.2	TA0	CCI0B			26 – P1.5	26 – P1.5
		DV_{SS}	GND			10 – P2.2	8 – P2.2
		DV_{CC}	V_{CC}			ADC10 (internal)	ADC10 (internal)
23 – P1.2	23 – P1.2	TA1	CCI1A	CCR1	TA1	23 – P1.2	23 – P1.2
		CAOUT (internal)	CCI1B			27 – P1.6	27 – P1.6
		DV_{SS}	GND			19 - P2.3	18 – P2.3
		DV_{CC}	V_{CC}			ADC10 (internal)	ADC10 (internal)
24 – P1.3	24 – P1.3	TA2	CCI2A	CCR2	TA2	24 – P1.3	24 – P1.3
		ACLK (internal)	CCI2B			28 – P1.7	28 – P1.7
		DV_{SS}	GND			20 - P2.4	19 – P2.4
		DV_{CC}	V_{CC}			ADC10 (internal)	ADC10 (internal)

PRODUCT PREVIEW

timer1_A2

Timer1_A2 is a 16-bit timer/counter with two capture/compare registers. Timer1_A2 can support multiple capture/compares, PWM outputs, and interval timing. Timer1_A2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer1_A2 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
28-PIN PW	32-PIN RHB					28-PIN PW	32-PIN RHB
21 – P1.0	21 – P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
9 – P2.1	7 – P2.1	TAINCLK	INCLK				
22 – P1.1	22 – P1.1	TA0	CCI0A	CCR0	TA0	17 – P3.6	15 – P3.6
17 – P3.6	15 – P3.6	TA0	CCI0B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
18 – P3.7	16 – P3.7	TA1	CCI1A	CCR1	TA1	18 – P3.7	16 – P3.7
		CAOUT (internal)	CCI1B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				

universal serial communication interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 pin or 4 pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA. Not all packages support the USCI functionality.

USCI_A0 provides support for SPI (3 pin or 4 pin), UART, enhanced UART, and IrDA.

USCI_B0 provides support for SPI (3 pin or 4 pin) and I2C.

PRODUCT PREVIEW

peripheral file map

PERIPHERALS WITH WORD ACCESS			
ADC10	ADC data transfer start address	ADC10SA	0x01BC
	ADC memory	ADC10MEM	0x01B4
	ADC control register 1	ADC10CTL1	0x01B2
	ADC control register 0	ADC10CTL0	0x01B0
	ADC analog enable 0	ADC10AE0	0x004A
	ADC analog enable 1	ADC10AE1	0x004B
	ADC data transfer control register 1	ADC10DTC1	0x0049
	ADC data transfer control register 0	ADC10DTC0	0x0048
Timer0_A3	Capture/compare register	TA0CCR2	0x0176
	Capture/compare register	TA0CCR1	0x0174
	Capture/compare register	TA0CCR0	0x0172
	Timer0_A3 register	TA0R	0x0170
	Capture/compare control	TA0CCTL2	0x0166
	Capture/compare control	TA0CCTL1	0x0164
	Capture/compare control	TA0CCTL0	0x0162
	Timer0_A3 control	TA0CTL	0x0160
	Timer0_A3 interrupt vector	TA0IV	0x012E
Timer1_A2	Capture/compare register	TA1CCR1	0x0194
	Capture/compare register	TA1CCR0	0x0192
	Timer1_A2 register	TA1R	0x0190
	Capture/compare control	TA1CCTL1	0x0184
	Capture/compare control	TA1CCTL0	0x0182
	Timer1_A2 control	TA1CTL	0x0180
	Timer1_A2 interrupt vector	TA1IV	0x011E
Flash Memory	Flash control 3	FCTL3	0x012C
	Flash control 2	FCTL2	0x012A
	Flash control 1	FCTL1	0x0128
Watchdog Timer+	Watchdog/timer control	WDTCTL	0x0120
PERIPHERALS WITH BYTE ACCESS			
USCI_B0	USCI_B0 transmit buffer	UCB0TXBUF	0x06F
	USCI_B0 receive buffer	UCB0RXBUF	0x06E
	USCI_B0 status	UCB0STAT	0x06D
	USCI B0 I2C Interrupt enable	UCB0CIE	0x06C
	USCI_B0 bit rate control 1	UCB0BR1	0x06B
	USCI_B0 bit rate control 0	UCB0BR0	0x06A
	USCI_B0 control 1	UCB0CTL1	0x069
	USCI_B0 control 0	UCB0CTL0	0x068
	USCI_B0 I2C slave address	UCB0SA	0x011A
	USCI_B0 I2C own address	UCB0OA	0x0118
USCI_A0	USCI_A0 transmit buffer	UCA0TXBUF	0x0067
	USCI_A0 receive buffer	UCA0RXBUF	0x0066
	USCI_A0 status	UCA0STAT	0x0065
	USCI_A0 modulation control	UCA0MCTL	0x0064
	USCI_A0 baud rate control 1	UCA0BR1	0x0063
	USCI_A0 baud rate control 0	UCA0BR0	0x0062
	USCI_A0 control 1	UCA0CTL1	0x0061
	USCI_A0 control 0	UCA0CTL0	0x0060
	USCI_A0 IrDA receive control	UCA0IRRCTL	0x005F
	USCI_A0 IrDA transmit control	UCA0IRTCTL	0x005E
	USCI_A0 auto baud rate control	UCA0ABCTL	0x005D

PRODUCT PREVIEW

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Comparator_A+	Comparator_A port disable	CAPD	0x005B
	Comparator_A control2	CACTL2	0x005A
	Comparator_A control1	CACTL1	0x0059
Basic Clock System+	Basic clock system control 3	BCSCTL3	0x0053
	Basic clock system control 2	BCSCTL2	0x0058
	Basic clock system control 1	BCSCTL1	0x0057
	DCO clock frequency control	DCOCTL	0x0056
Port P3	Port P3 resistor enable	P3REN	0x0010
	Port P3 selection	P3SEL	0x001B
	Port P3 direction	P3DIR	0x001A
	Port P3 output	P3OUT	0x0019
	Port P3 input	P3IN	0x0018
Port P2	Port P2 selection 2	P2SEL2	0x0042
	Port P2 resistor enable	P2REN	0x002F
	Port P2 selection	P2SEL	0x002E
	Port P2 interrupt enable	P2IE	0x002D
	Port P2 interrupt edge select	P2IES	0x002C
	Port P2 interrupt flag	P2IFG	0x002B
	Port P2 direction	P2DIR	0x002A
	Port P2 output	P2OUT	0x0029
	Port P2 input	P2IN	0x0028
Port P1	Port P1 selection 2 register	P1SEL2	0x0041
	Port P1 resistor enable	P1REN	0x0027
	Port P1 selection	P1SEL	0x0026
	Port P1 interrupt enable	P1IE	0x0025
	Port P1 interrupt edge select	P1IES	0x0024
	Port P1 interrupt flag	P1IFG	0x0023
	Port P1 direction	P1DIR	0x0022
	Port P1 output	P1OUT	0x0021
	Port P1 input	P1IN	0x0020
Special Function	SFR interrupt flag 2	IFG2	0x0003
	SFR interrupt flag 1	IFG1	0x0002
	SFR interrupt enable 2	IE2	0x0001
	SFR interrupt enable 1	IE1	0x0000

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MSP430F2112IPW	PREVIEW	TSSOP	PW	28	2000	TBD	Call TI	Call TI
MSP430F2112IRHB	PREVIEW	QFN	RHB	32	250	TBD	Call TI	Call TI
MSP430F2112TPW	PREVIEW	TSSOP	PW	28	2000	TBD	Call TI	Call TI
MSP430F2112TRHB	PREVIEW	QFN	RHB	32	250	TBD	Call TI	Call TI
MSP430F2122IPW	PREVIEW	TSSOP	PW	28	2000	TBD	Call TI	Call TI
MSP430F2122IRHB	PREVIEW	QFN	RHB	32	250	TBD	Call TI	Call TI
MSP430F2122TPW	PREVIEW	TSSOP	PW	28	2000	TBD	Call TI	Call TI
MSP430F2122TRHB	PREVIEW	QFN	RHB	32	250	TBD	Call TI	Call TI
MSP430F2132IPW	PREVIEW	TSSOP	PW	28	50	TBD	Call TI	Call TI
MSP430F2132IRHB	PREVIEW	QFN	RHB	32	250	TBD	Call TI	Call TI
MSP430F2132TPW	PREVIEW	TSSOP	PW	28	50	TBD	Call TI	Call TI
MSP430F2132TRHB	PREVIEW	QFN	RHB	32	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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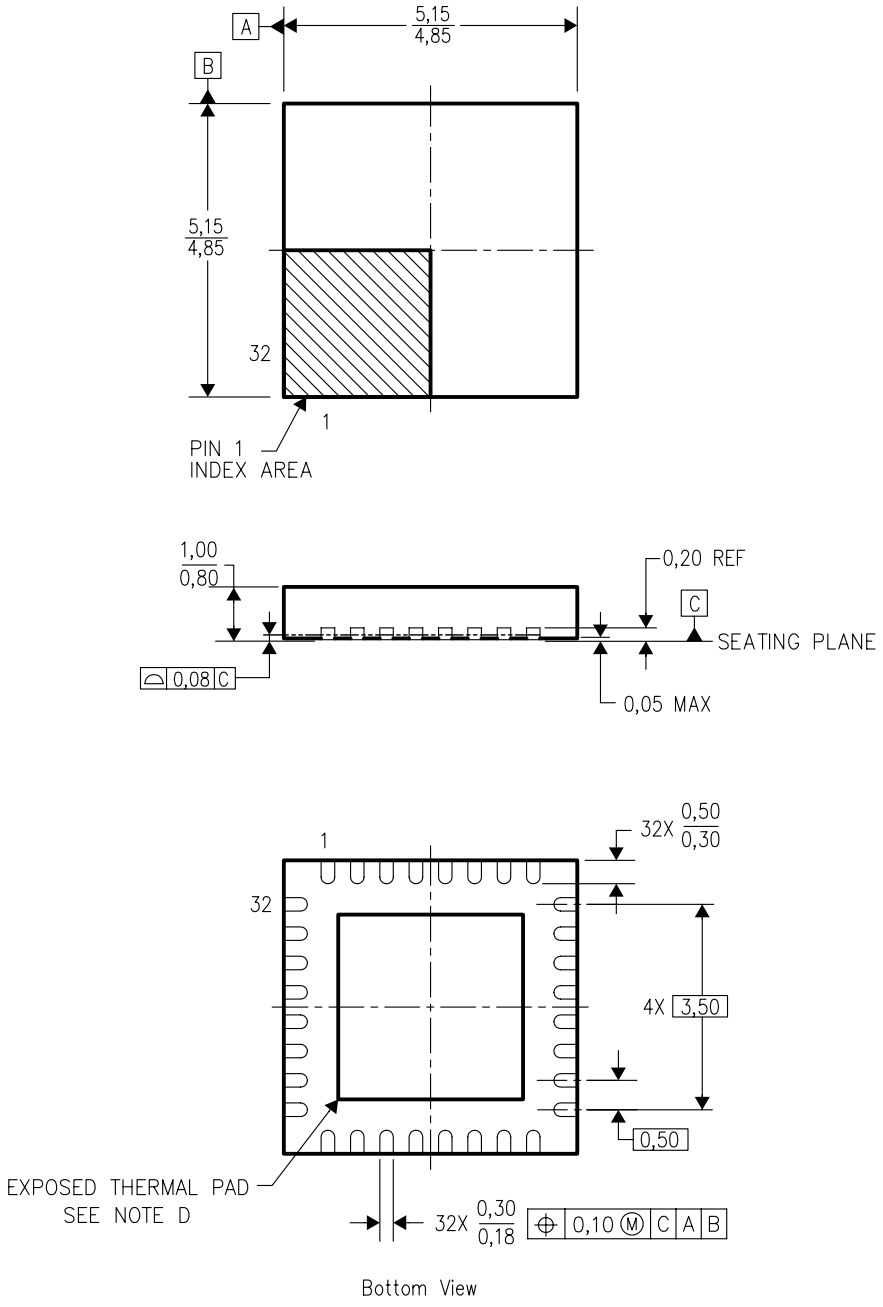
RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK

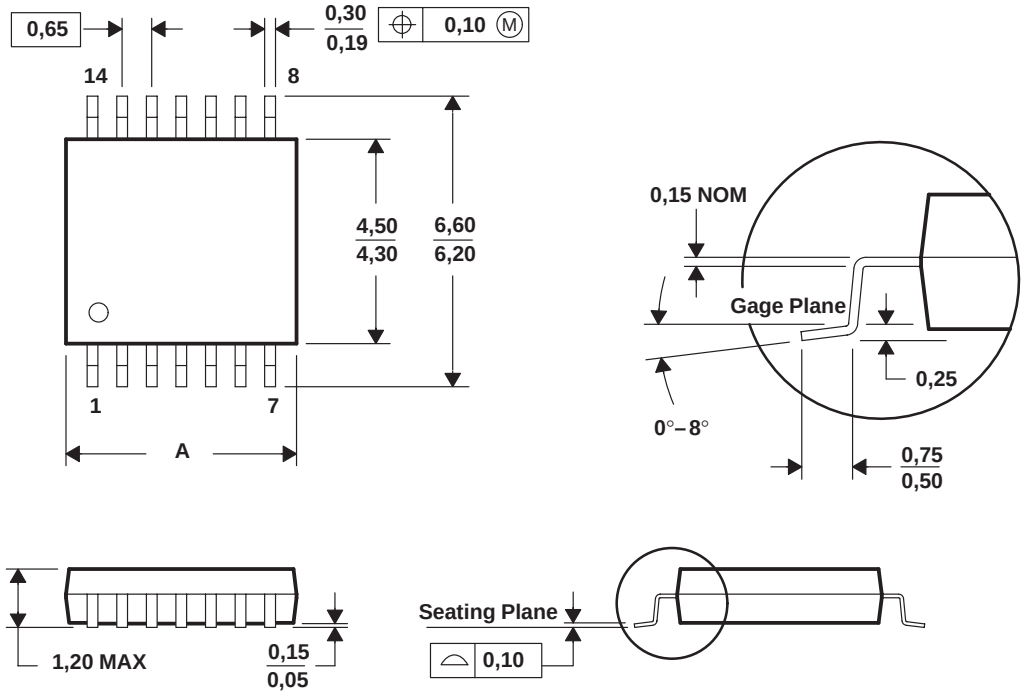


4204326/C xx/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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