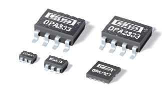


SBOS351 − MARCH 2006

1.8V, *micro*POWER CMOS OPERATIONAL AMPLIFIERS Zer∅-Drift Series

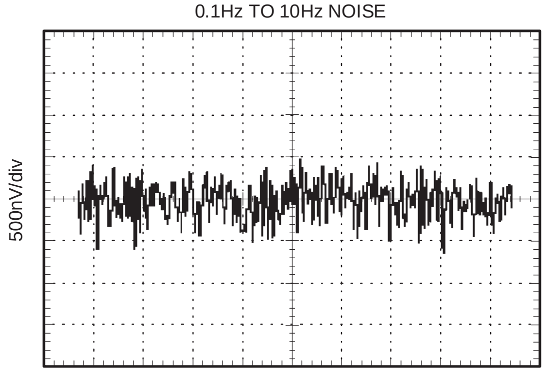
FEATURES

- LOW OFFSET VOLTAGE: 10μV (max)
- ZERO DRIFT: 0.05μV/°C (max)
- 0.01Hz to 10Hz NOISE: 1.1μV_{PP}
- QUIESCENT CURRENT: 17μA
- SINGLE-SUPPLY OPERATION
- SUPPLY VOLTAGE: 1.8V to 5.5V
- RAIL-TO-RAIL INPUT/OUTPUT
- *micro*SIZE PACKAGES: SC70 and SOT23

APPLICATIONS

- TRANSDUCER APPLICATIONS
- TEMPERATURE MEASUREMENTS
- ELECTRONIC SCALES
- MEDICAL INSTRUMENTATION
- BATTERY-POWERED INSTRUMENTS
- HANDHELD TEST EQUIPMENT

0.1Hz TO 10Hz NOISE



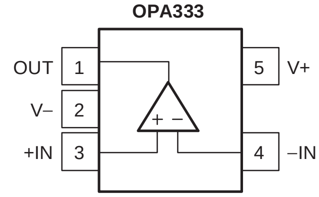
DESCRIPTION

The OPA333 series of CMOS operational amplifiers uses a proprietary auto-calibration technique to simultaneously provide very low offset voltage (10μV max) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100mV beyond the rails and rail-to-rail output that swings within 50mV of the rails. Single or dual supplies as low as +1.8V (±0.9V) and up to +5.5V (±2.75V) may be used. They are optimized for low-voltage, single-supply operation.

The OPA333 family offers excellent CMRR without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

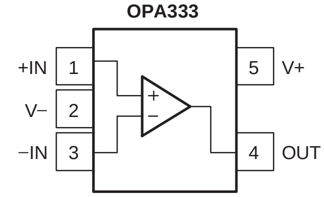
The OPA333 (single version) is available in the SC70-5, SOT23-5, and SO-8 packages. The OPA2333 (dual version) is offered in DFN-8 (3mm x 3mm, available Q2 '06) and SO-8 packages. All versions are specified for operation from −40°C to +125°C.

OPA333



SOT23−5

OPA333



SC70−5

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+7V
Signal Input Terminals, Voltage(2)	−0.3V to (V+) + 0.3V
Signal Input Terminals, Voltage(2)	±10mA
Output Short-Circuit(3)	Continuous
Operating Temperature	−40°C to +150°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
ESD Rating	
Human Body Model	4000V
Charged Device Model	1000V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

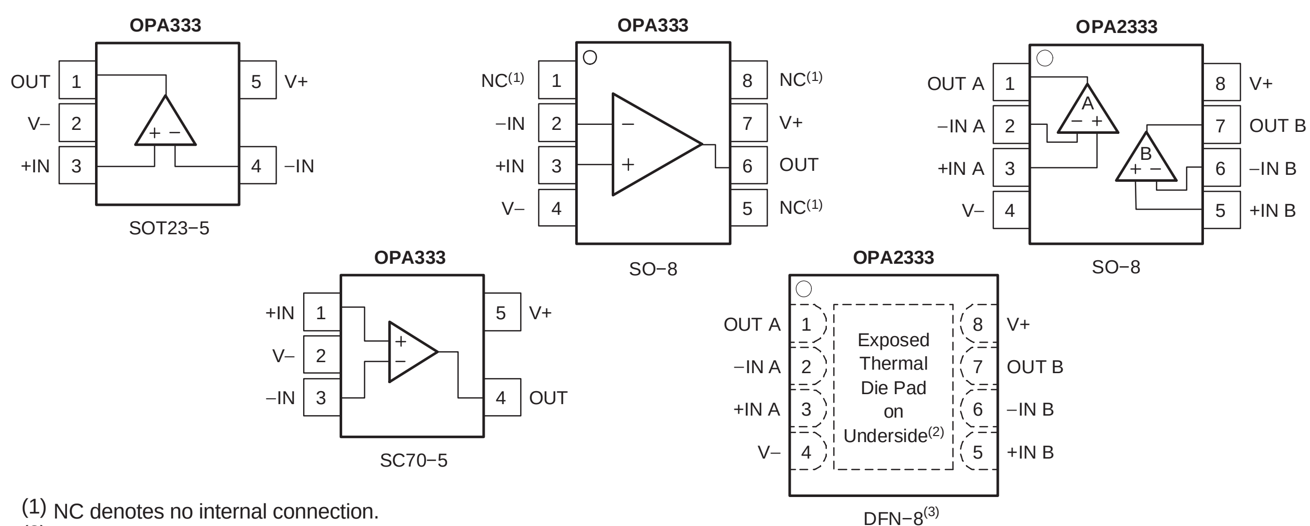
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA333	SOT23-5	DBV	OAXQ
OPA333	SC70-5	DCK	BQY
OPA333	SO-8	D	O333A
OPA2333	SO-8	D	O2333A
OPA2333	DFN-8(2)	DRB	BQZ

(1) For the most current specification and package information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Available Q2 ’06.

PIN CONFIGURATIONS



(1) NC denotes no internal connection.
(2) Connect thermal die pad to V−.
(3) Available Q2 ’06.

ELECTRICAL CHARACTERISTICS: V_S = +1.8V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = −40°C to +125°C.**

At T_A = +25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

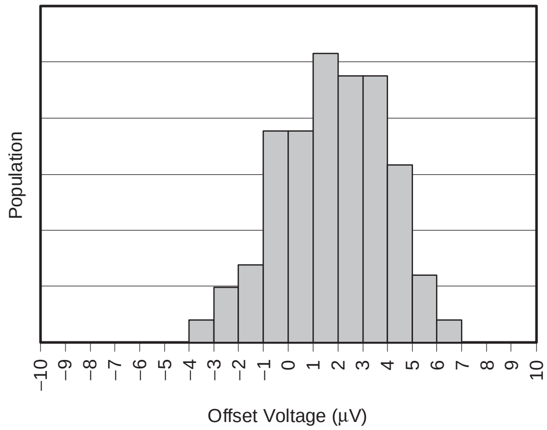
PARAMETER		TEST CONDITIONS	OPA333, OPA2333 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = +5V		2	10	μV
vs Temperature	**dV_{OS}/dT**			**0.02**	**0.05**	**μV/°C**
vs Power Supply	**PSRR**	**V_S = +1.8V to +5.5V**		**1**	**5**	**μV/V**
Long-Term Stability(1)				See Note (1)		
Channel Separation, dc				0.1		μV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			±70	±200	pA
over Temperature				**±150**		**pA**
Input Offset Current	I_{OS}			±140	±400	pA
NOISE						
Input Voltage Noise, f = 0.01Hz to 1Hz				0.3		μV_{PP}
Input Voltage Noise, f = 0.1Hz to 10Hz				1.1		μV_{PP}
Input Current Noise, f = 10Hz	i_n			100		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) − 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	**CMRR**	**(V−) − 0.1V < V_{CM} < (V+) + 0.1V**	**106**	**130**		**dB**
INPUT CAPACITANCE						
Differential				2		pF
Common-Mode				4		pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	**A_{OL}**	**(V−) + 100mV < V_O < (V+) − 100mV, R_L = 10kΩ**	**106**	**130**		**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	C_L = 100pF		350		kHz
Slew Rate	SR	G = +1		0.16		V/μs
OUTPUT						
Voltage Output Swing from Rail		R_L = 10kΩ		30	50	mV
over Temperature		**R_L = 10kΩ**			**70**	**mV**
Short-Circuit Current	I_{SC}			±5		mA
Capacitive Load Drive	C_L			See Typical Characteristics		
Open-Loop Output Impedance		f = 350kHz, I_O = 0		2		kΩ
POWER SUPPLY						
Specified Voltage Range	V_S		1.8		5.5	V
Quiescent Current Per Amplifier	I_Q	I_O = 0		17	25	μA
over Temperature					**28**	**μA**
Turn-On Time		V_S = +5V		100		μs
TEMPERATURE RANGE						
Specified Range			−40		+125	°C
Operating Range			−40		+150	°C
Storage Range			−65		+150	°C
Thermal Resistance	θ_{JA}					°C/W
SOT23-5				200		°C/W
SO-8				150		°C/W
DFN-8				50		°C/W
SC70-5				250		°C/W

(1) 300-hour life test at +150°C demonstrated randomly distributed variation of approximately 1μV.

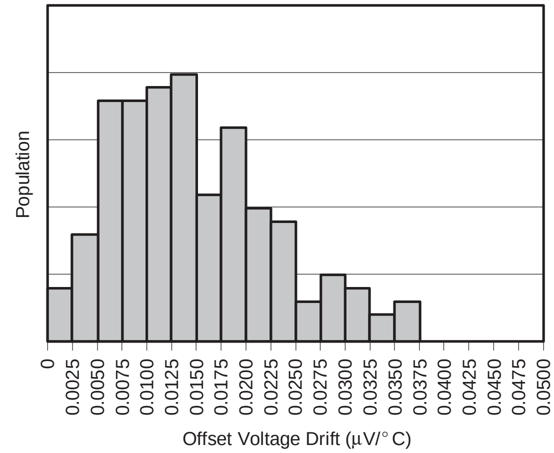
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, and C_L = 0pF, unless otherwise noted.

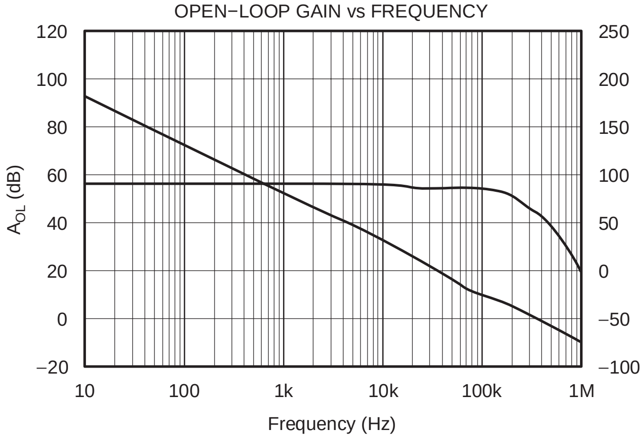
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



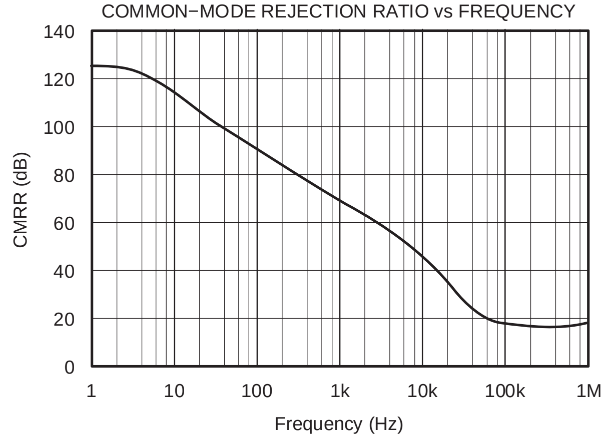
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



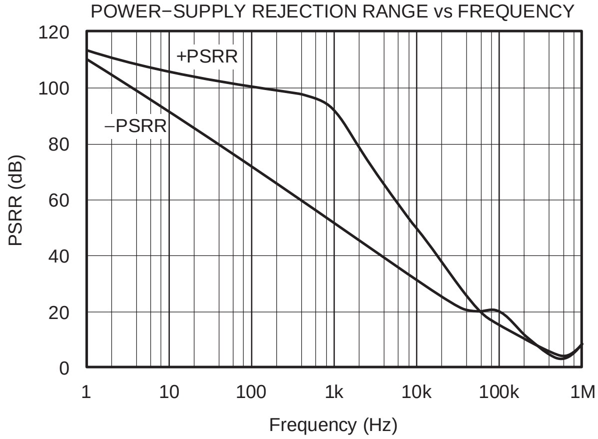
OPEN−LOOP GAIN vs FREQUENCY



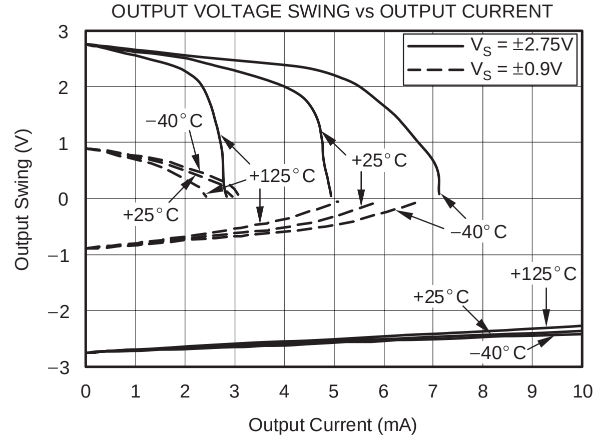
COMMON−MODE REJECTION RATIO vs FREQUENCY



POWER−SUPPLY REJECTION RANGE vs FREQUENCY

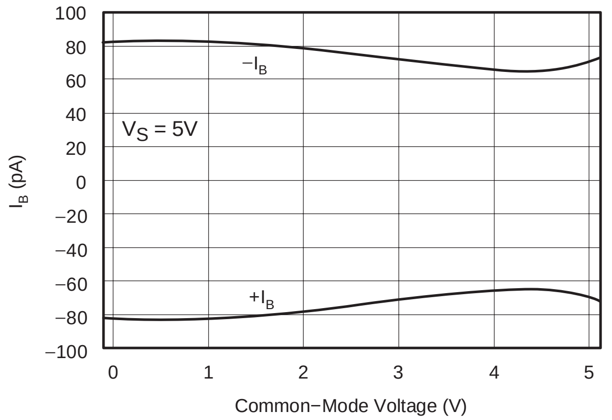


OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

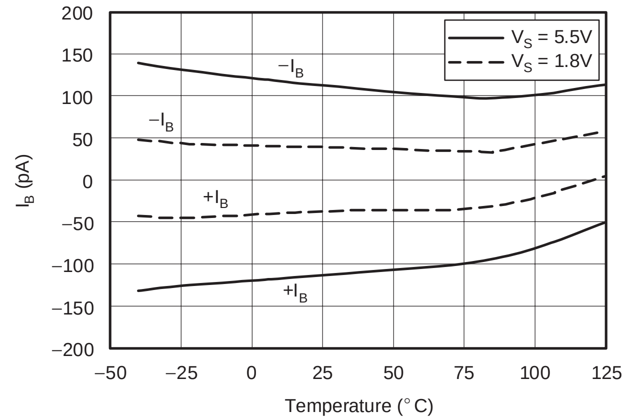


TYPICAL CHARACTERISTICS (continued)

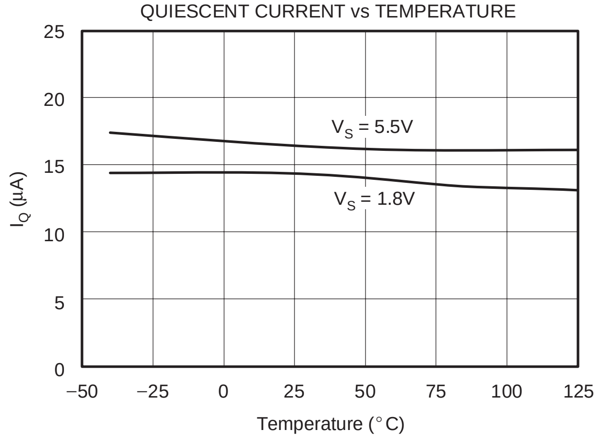
At T_A = +25°C, V_S = +5V, and C_L = 0pF, unless otherwise noted.



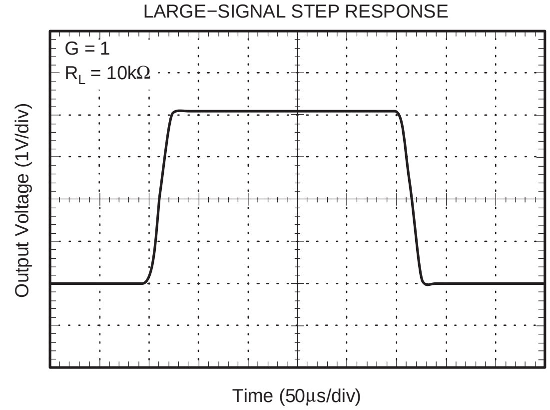
INPUT BIAS CURRENT vs COMMON−MODE VOLTAGE



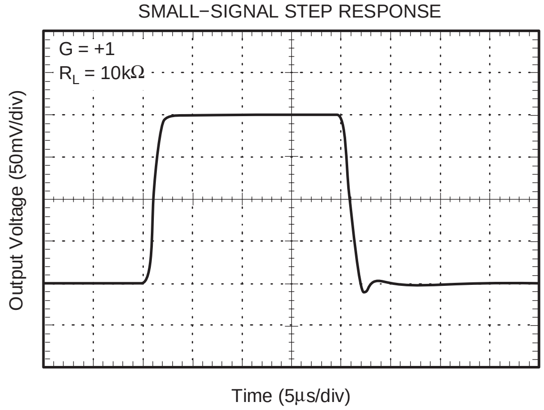
INPUT BIAS CURRENT vs TEMPERATURE



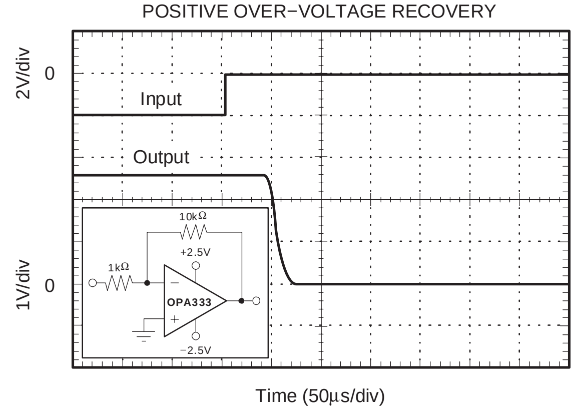
QUIESCENT CURRENT vs TEMPERATURE



LARGE−SIGNAL STEP RESPONSE



SMALL−SIGNAL STEP RESPONSE

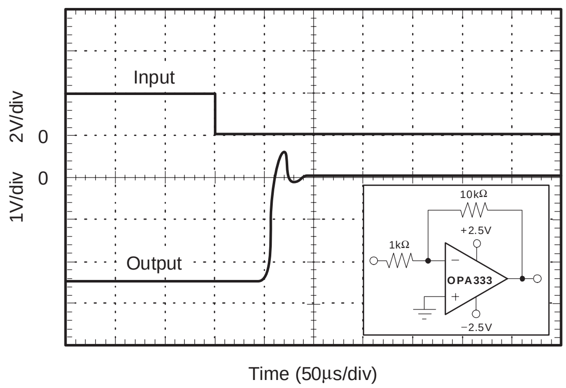


POSITIVE OVER−VOLTAGE RECOVERY

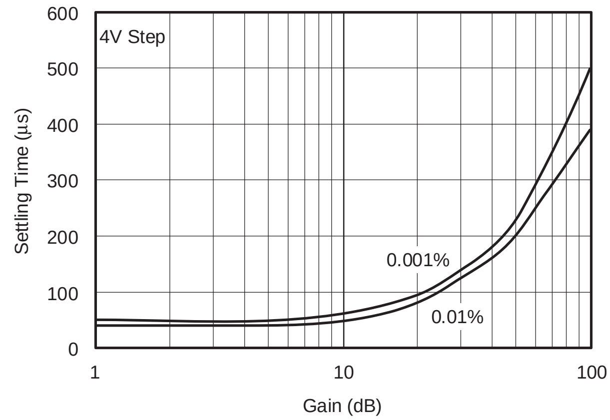
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, and C_L = 0pF, unless otherwise noted.

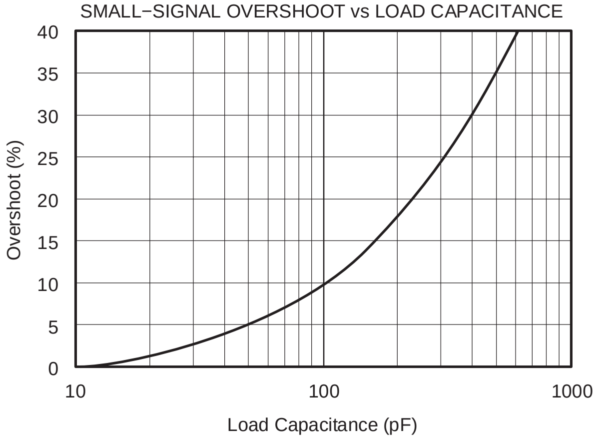
NEGATIVE OVER−VOLTAGE RECOVERY



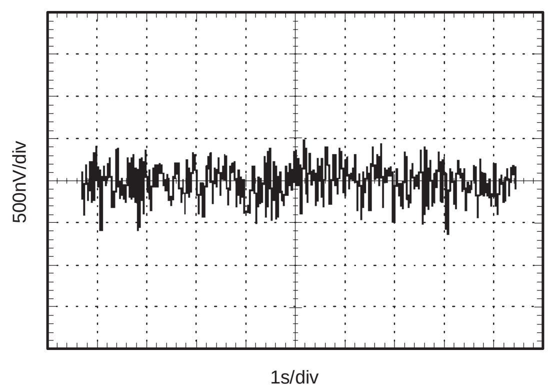
SETTLING TIME vs CLOSED−LOOP GAIN



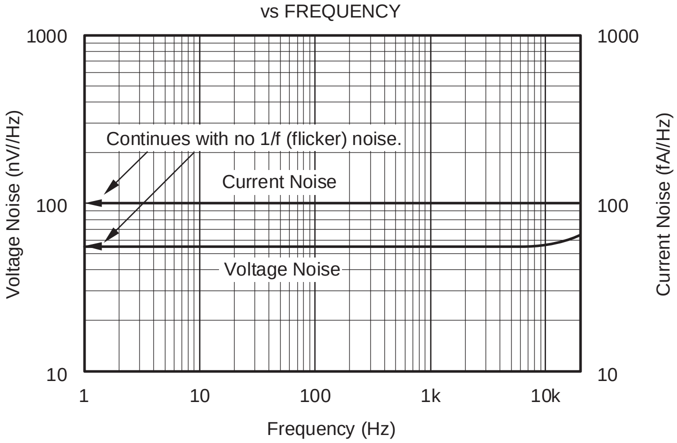
SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



0.1Hz TO 10Hz NOISE



CURRENT AND VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY



APPLICATIONS INFORMATION

The OPA333 and OPA2333 are unity-gain stable and free from unexpected output phase reversal. They use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1µV/°C or higher, depending on materials used.

OPERATING VOLTAGE

The OPA333 and OPA2333 op amps operate over a power-supply range of +1.8V to +5.5V (±0.9V to ±2.75V). Supply voltages higher than +7V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

INPUT VOLTAGE

The OPA333 and OPA2333 input common-mode voltage range extends 0.1V beyond the supply rails. The OPA333 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Normally, input bias current is about 70pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This limitation is easily accomplished with an input resistor, as shown in Figure 1.

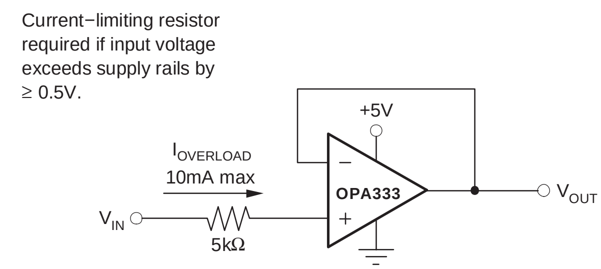


Figure 1. Input Current Protection

INTERNAL OFFSET CORRECTION

The OPA333 and OPA2333 op amps use an auto-calibration technique with a time-continuous 350kHz op amp in the signal path. This amplifier is zero-corrected every 8µs using a proprietary technique. Upon power-up, the amplifier requires approximately 100µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

ACHIEVING OUTPUT SWING TO THE OP AMP NEGATIVE RAIL

Some applications require output voltage swings from 0V to a positive full-scale voltage (such as +2.5V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA333 and OPA2333 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. A pull-down resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 2.

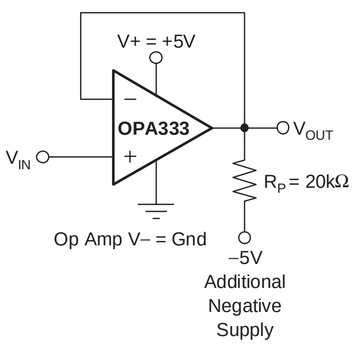


Figure 2. For V_{OUT} Range to Ground

The OPA333 and OPA2333 have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA333 and OPA2333 have been characterized to perform with this technique; however, the recommended resistor value is approximately 20kΩ. Note that this configuration will increase the current consumption by several hundreds of microamps. Accuracy is excellent down to 0V and as low as −2mV. Limiting and nonlinearity occurs below−2mV, but excellent accuracy returns as the output is again driven above −2mV. Lowering the resistance of the pull-down resistor will allow the op amp to swing even further below the negative rail. Resistances as low as 10kΩ can be used to achieve excellent accuracy down to −10mV.

GENERAL LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI (electromagnetic-interference) susceptibility.

Operational amplifiers vary in their susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The OPA333 has been specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels..

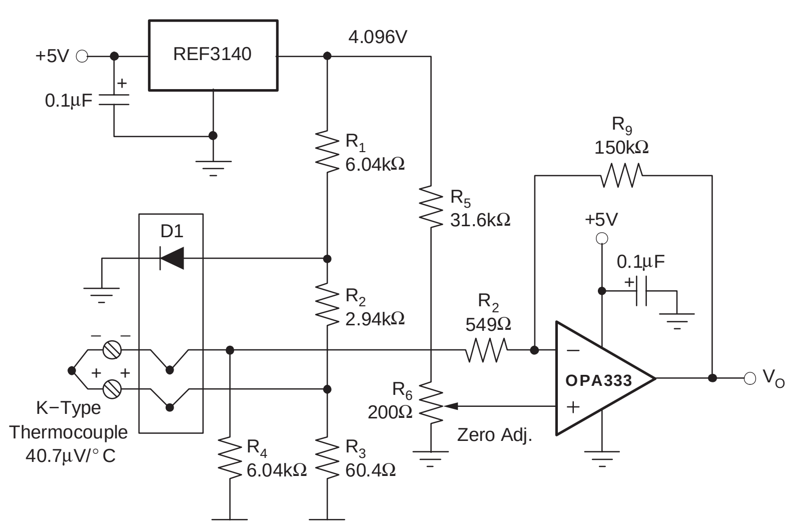


Figure 3. Temperature Measurement

Figure 4 shows the basic configuration for a bridge amplifier.

A low-side current shunt monitor is shown in Figure 5. R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I²C bus. Since the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5V power supply is sufficiently stable, the REF3130 may be omitted.

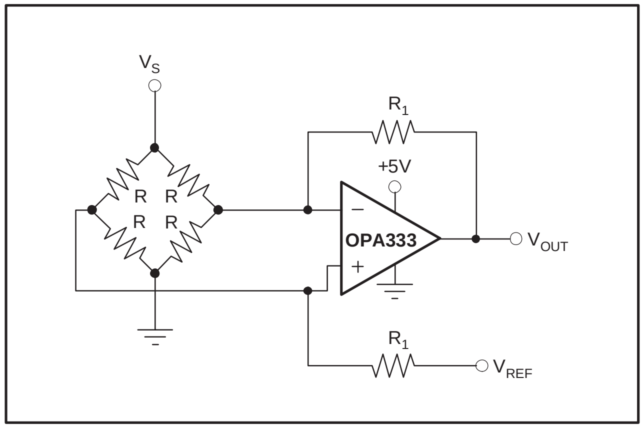


Figure 4. Single Op Amp Bridge Amplifier

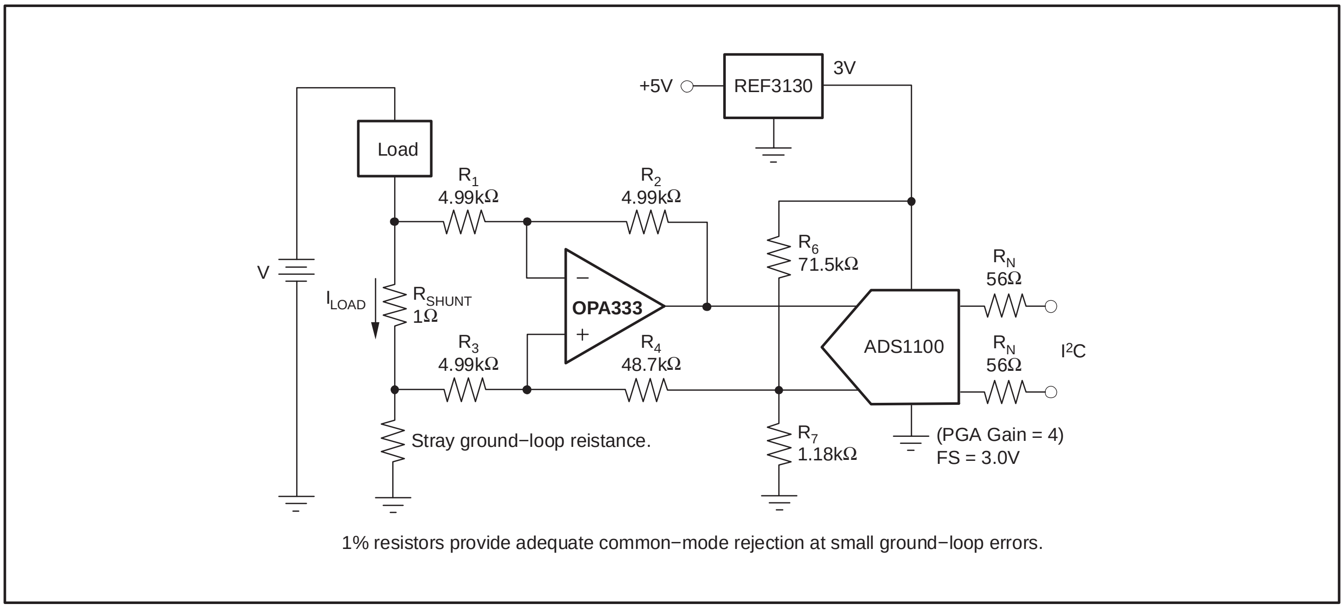


Figure 5. Low-Side Current Monitor

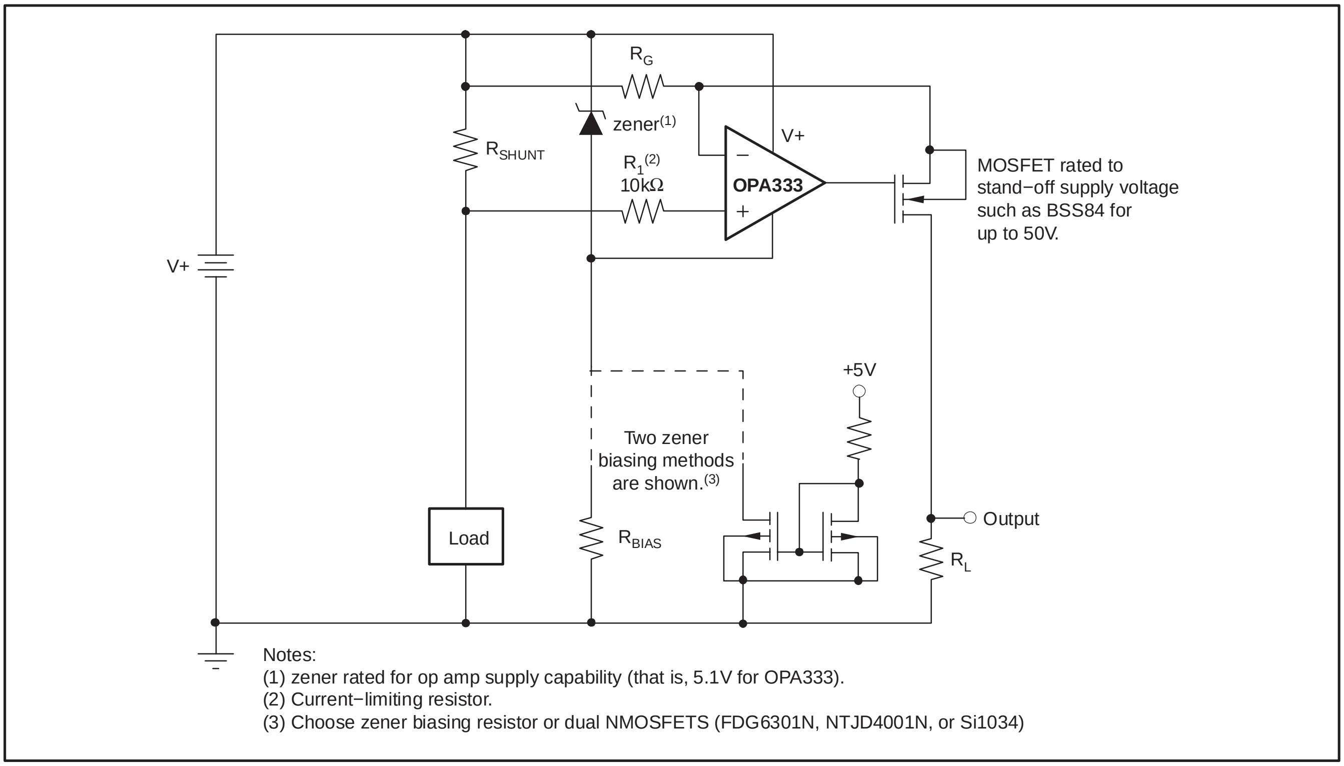


Figure 6. High-Side Current Monitor

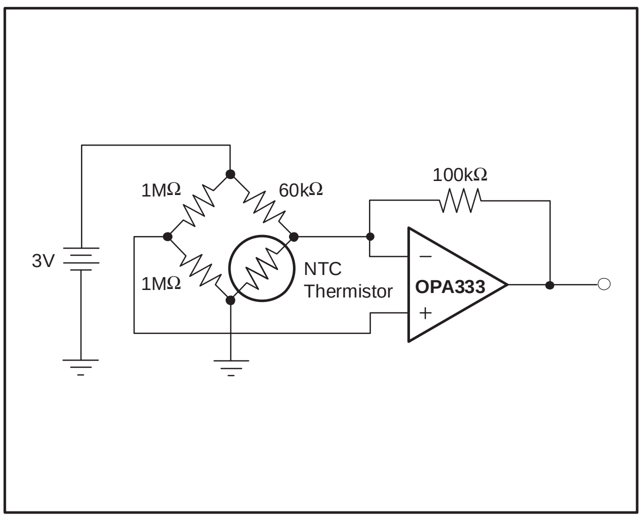


Figure 7. Thermistor Measurement

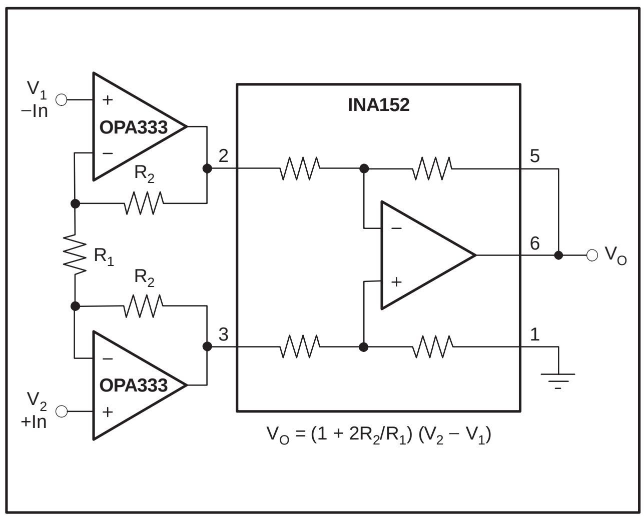


Figure 8. Precision Instrumentation Amplifier

DFN PACKAGE

The OPA2333 is offered in an DFN-8 package (also known as SON). The DFN is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See Application Note *QFN/SON PCB Attachment* (SLUA271) and Application Report *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com.

The exposed leadframe die pad on the bottom of the package should be connected to V− or left unconnected.

DFN LAYOUT GUIDELINES

The exposed leadframe die pad on the DFN package should be soldered to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be necessary based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA2333AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA2333AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA2333AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA2333AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA333AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA333AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA333AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA333AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA333AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA333AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA333AIDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA333AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA333AIDCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA333AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA333AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA333AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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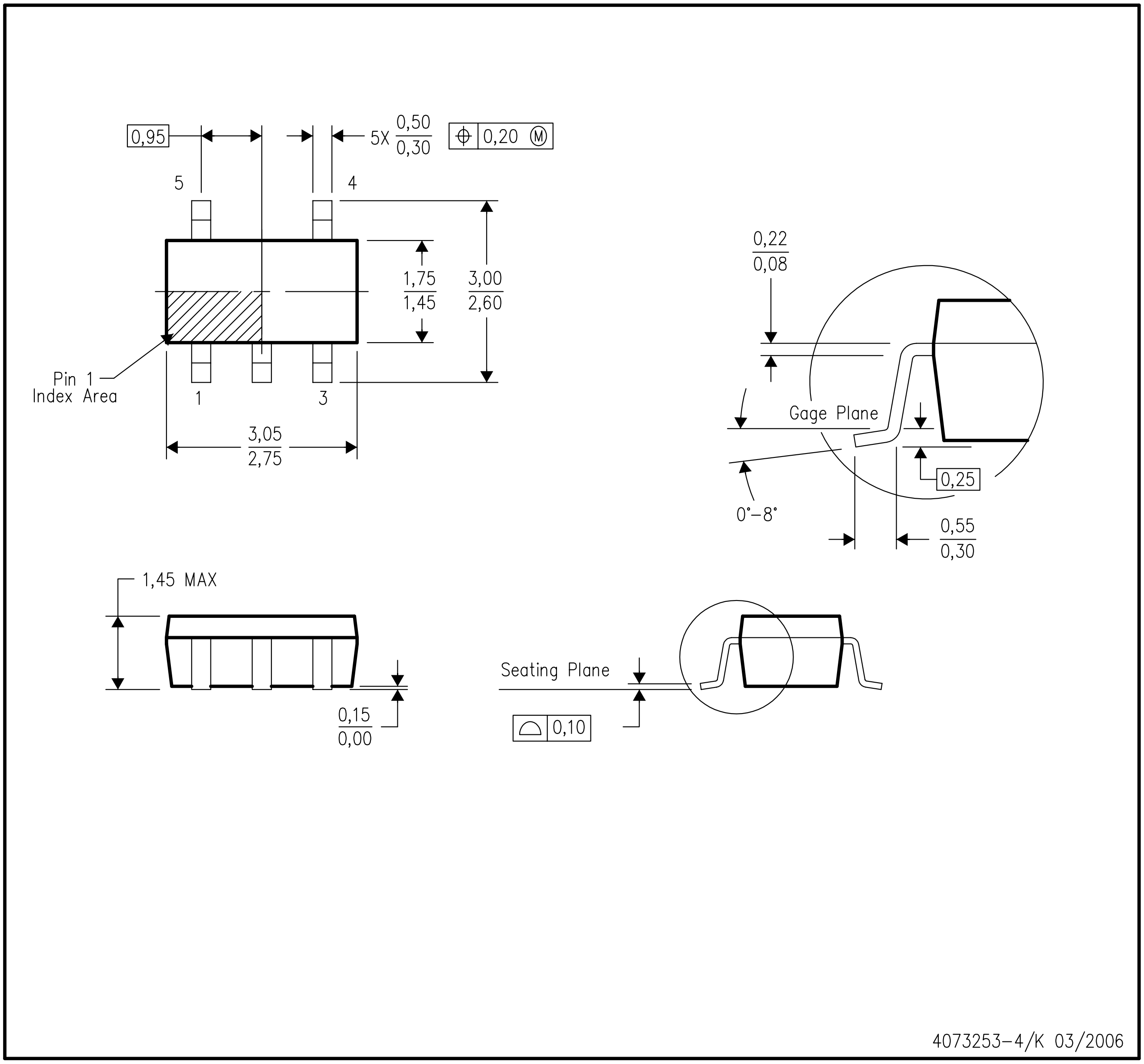
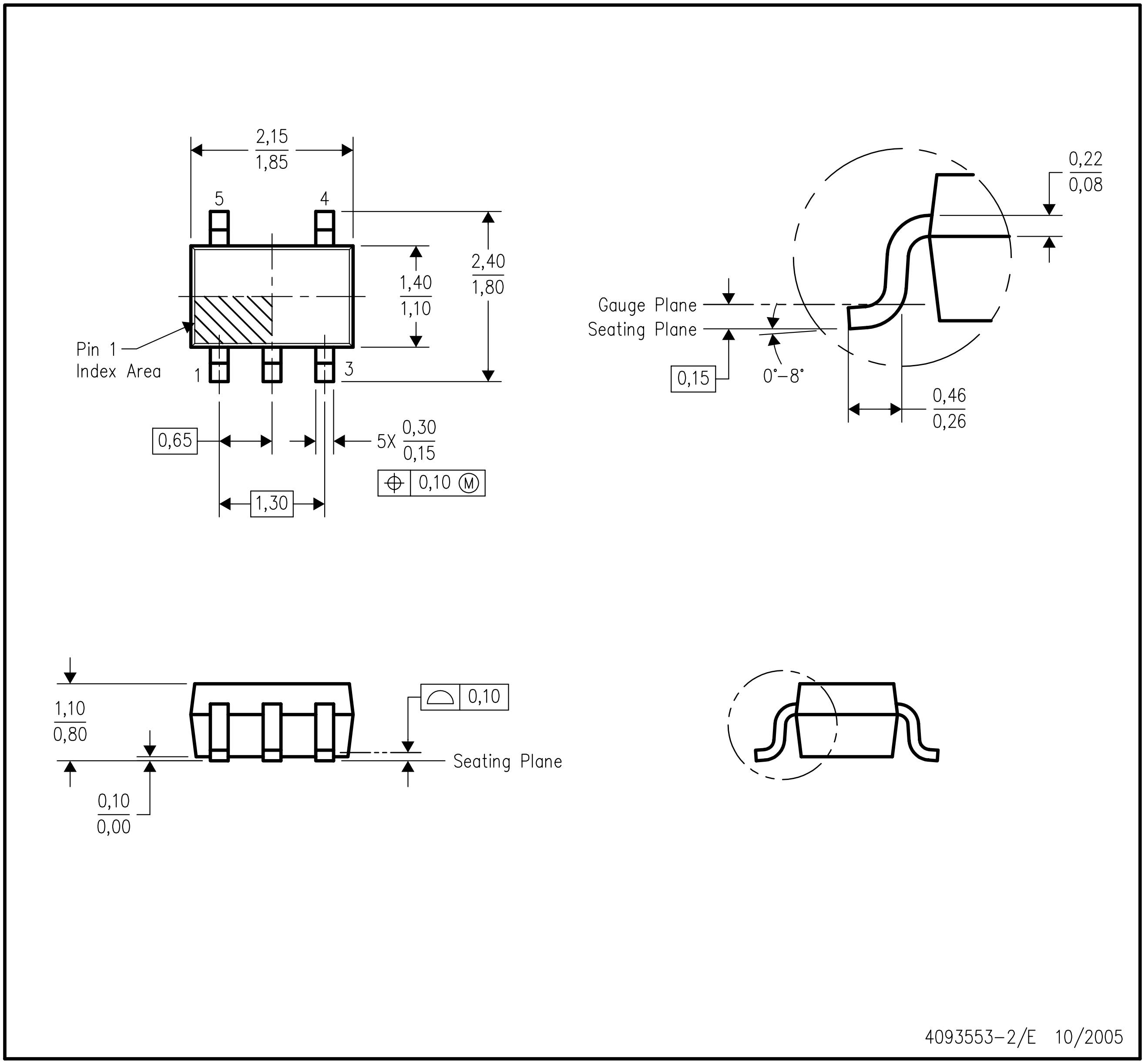
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



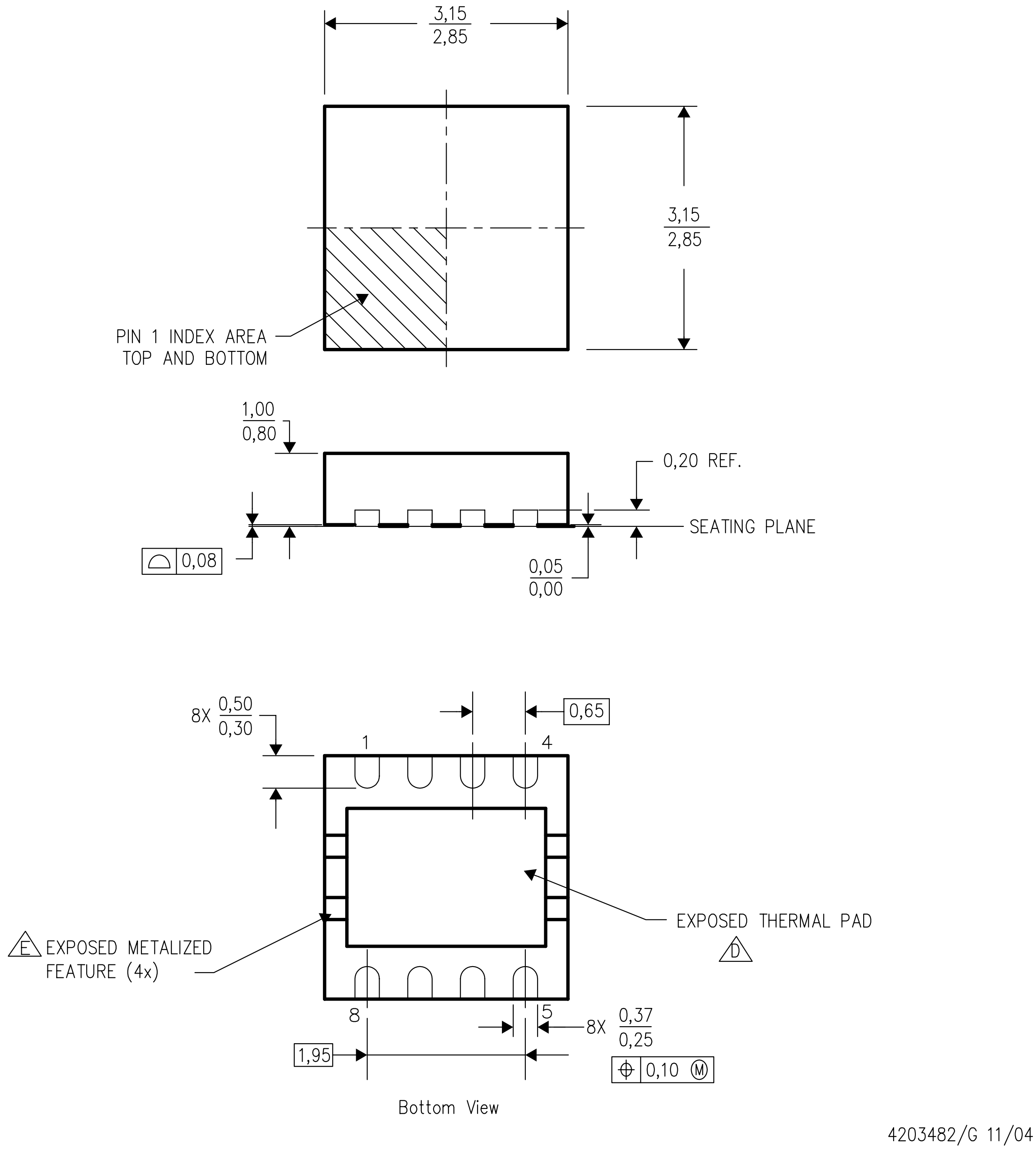
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



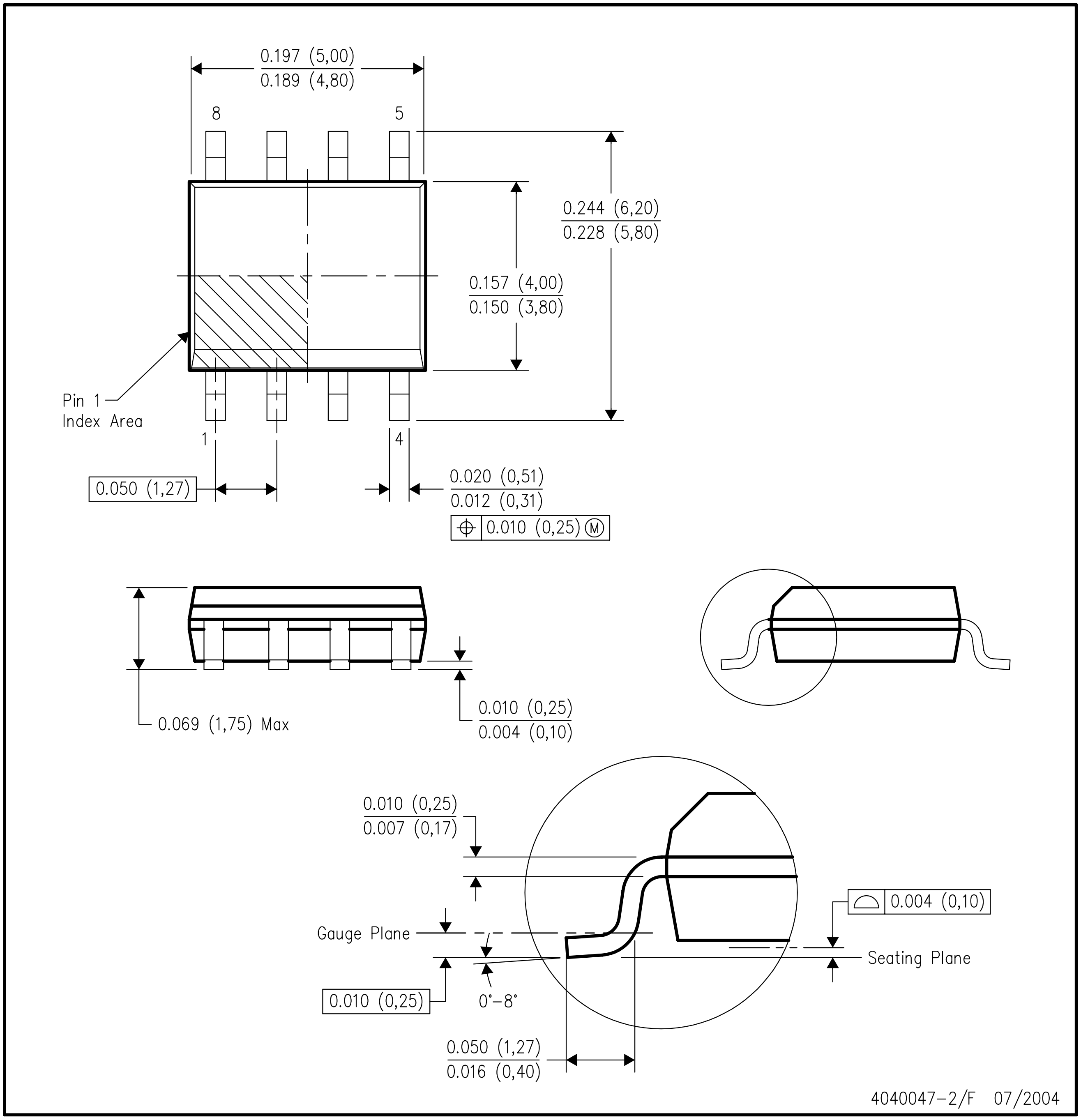
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Metalized features are supplier options and may not be on the package.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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