DATA SHEET

P82B96
Dual bi-directional bus buffer

Product data
Supersedes data of 2003 Apr 02

2004 Mar 26

Philips
Semiconductors

PHILIPS

Dual bi-directional bus buffer P82B96

FEATURES

- Bi-directional data transfer of I²C-bus signals
- Isolates capacitance allowing 400 pF on Sx/Sy side and 4000 pF on Tx/Ty side
- Tx/Ty outputs have 60 mA sink capability for driving low impedance or high capacitive buses
- 400 kHz operation over at least 20 meters of wire (see *AN10148*)
- Supply voltage range of 2 V to 15 V with I²C logic levels on Sx/Sy side independent of supply voltage
- Splits I²C signal into pairs of forward/reverse Tx/Rx, Ty/Ry signals for interface with opto-electrical isolators and similar devices that need uni-directional input and output signal paths.
- Low power supply current
- ESD protection exceeds 3500 V HBM per JESD22-A114, 250 V DIP package / 400 V SO package MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up free (bipolar process with no latching structures)
- Packages offered: DIP, SO, and TSSOP

TYPICAL APPLICATIONS

- Interface between I²C buses operating at different logic levels (e.g., 5 V and 3 V or 15 V)
- Interface between I²C and SMB (350 μA) bus standard.
- Simple conversion of I²C SDA or SCL signals to multi-drop differential bus hardware, e.g., via compatible PCA82C250.
- Interfaces with Opto-couplers to provide Opto isolation between I²C-bus nodes up to 400 kHz.

DESCRIPTION

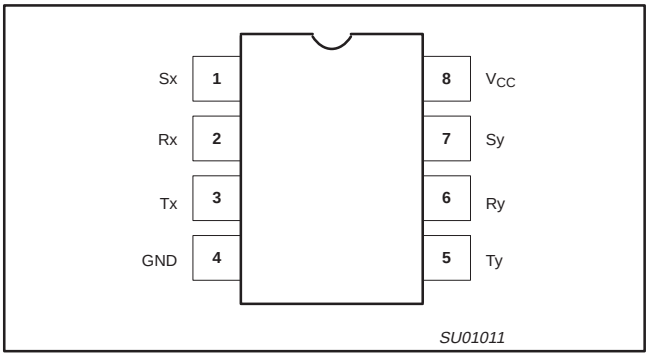
The P82B96 is a bipolar IC that creates a non-latching, bi-directional, logic interface between the normal I²C-bus and a range of other bus configurations. It can interface I²C-bus logic signals to similar buses having different voltage and current levels.

For example it can interface to the 350 μA SMB bus, to 3.3 V logic devices, and to 15 V levels and/or low impedance lines to improve noise immunity on longer bus lengths.

It achieves this interface without any restrictions on the normal I²C protocols or clock speed. The IC adds minimal loading to the I²C node, and loadings of the new bus or remote I²C nodes are not transmitted or transformed to the local node. Restrictions on the number of I²C devices in a system, or the physical separation between them, are virtually eliminated. Transmitting SDA/SCL signals via balanced transmission lines (twisted pairs) or with galvanic isolation (opto-coupling) is simple because separate directional Tx and Rx signals are provided. The Tx and Rx signals may be directly connected, without causing latching, to provide an alternative bi-directional signal line with I²C properties.

PIN CONFIGURATIONS

8-pin dual in-line, SO, TSSOP



PINNING

SYMBOL	PIN	DESCRIPTION
Sx	1	I²C-bus (SDA or SCL)
Rx	2	Receive signal
Tx	3	Transmit signal
GND	4	Negative Supply
Ty	5	Transmit signal
Ry	6	Receive signal
Sy	7	I²C-bus (SDA or SCL)
V_{CC}	8	Positive supply

SPECIAL NOTE:

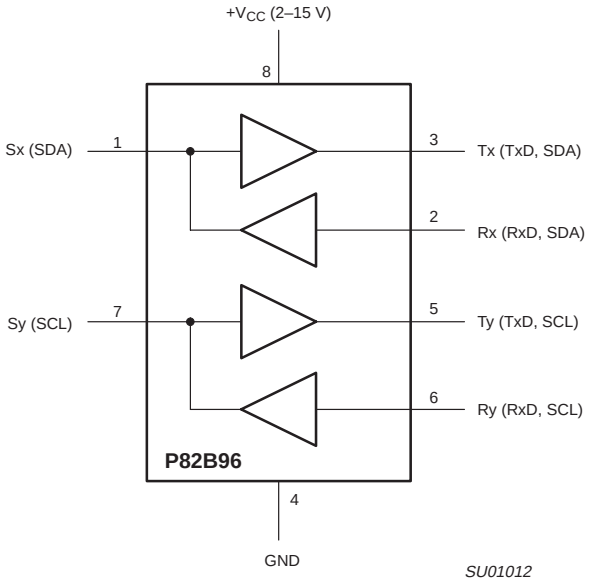
Two or more Sx or Sy I/Os must not be interconnected. The P82B96 design does not support this configuration. Bi-directional I²C signals do not allow any direction control pin so, instead, slightly different logic low voltage levels are used at Sx/Sy to avoid latching of this buffer. A “regular I²C low” applied at the Rx/Ry of a P82B96 will be propagated to Sx/Sy as a “buffered low” with a slightly higher voltage level. If this special “buffered low” is applied to the Sx/Sy of another P82B96 that second P82B96 will not recognize it as a “regular I²C-bus low” and will not propagate it to its Tx/Ty output. The Sx/Sy side of P82B96 may not be connected to similar buffers that rely on special logic thresholds for their operation, for example PCA9511, PCA9515, or PCA9518. The Sx/Sy side is only intended for, and compatible with, the normal I²C logic voltage levels of I²C master and slave chips—or even Tx/Rx signals of a second P82B96 if required. The Tx/Rx and Ty/Ry I/O pins use the standard I²C logic voltage levels of all I²C parts. There are NO restrictions on the interconnection of the Tx/Rx and Ty/Ry I/O pins to other P82B96s, for example in a star or multi-point configuration with the Tx/Rx and Ty/Ry I/O pins on the common bus and the Sx/Sy side connected to the line card slave devices. For more details see *Application Note AN255*.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
8-pin plastic dual In-line package	–40 °C to +85 °C	P82B96PN	P82B96PN	SOT97-1
8-pin plastic small outline package	–40 °C to +85 °C	P82B96TD	P82B96T	SOT96-1
8-pin plastic thin shrink small outline package	–40 °C to +85 °C	P82B96DP	82B96	SOT505-1

NOTE:
1. Standard packing quantities and other packaging data are available at www.philipslogic.com/packaging.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The P82B96 has two identical buffers allowing buffering of both of the I^2C (SDA and SCL) signals. Each buffer is made up of two logic signal paths, a forward path from the I^2C interface pin which drives the buffered bus, and a reverse signal path from the buffered bus input to drive the I^2C-bus interface.

Thus these paths are:
1. Sense the voltage state of the I^2C pin Sx (or Sy) and transmit this state to the pin Tx (Ty resp.), and
2. Sense the state of the pin Rx (Ry) and pull the I^2C pin LOW whenever Rx (Ry) is LOW.

The rest of this discussion will address only the “x” side of the buffer: the “y” side is identical.

The I^2C pin (Sx) is designed to interface with a normal I^2C-bus.

The logic threshold voltage levels on the I^2C-bus are independent of the IC supply V_{CC} The maximum I^2C-bus supply voltage is 15 V and the guaranteed static sink current is 3 mA.

The logic level of Rx is determined from the power supply voltage V_{CC} of the chip. Logic LOW is below 42 % of V_{CC}, and logic HIGH is above 58 % of V_{CC}: with a typical switching threshold of half V_{CC}.

Tx is an open collector output without ESD protection diodes to V_{CC}. It may be connected via a pull-up resistor to a supply voltage in excess of $V_{CC,}$ as long as the 15 V rating is not exceeded. It has a larger current sinking capability than a normal I^2C device, being able to sink a static current of greater than 30 mA, and typical 100 mA dynamic pull-down capability as well.

A logic LOW is only transmitted to Tx when the voltage at the I^2C pin (Sx) is below 0.6 V. A logic LOW at Rx will cause the I^2C-bus (Sx) to be pulled to a logic LOW level in accordance with I^2C requirements (max. 1.5 V in 5 V applications) but not low enough to be looped back to the Tx output and cause the buffer to latch LOW.

The minimum LOW level this chip can achieve on the I^2C-bus by a LOW at Rx is typically 0.8 V.

If the supply voltage V_{CC} fails, then neither the I^2C nor the Tx output will be held LOW. Their open collector configuration allows them to be pulled up to the rated maximum of 15 V even without V_{CC} present. The input configuration on Sx and Rx also present no loading of external signals even when V_{CC} is not present.

The effective input capacitance of any signal pin, measured by its effect on bus rise times, is less than 7 pF for all bus voltages and supply voltages including V_{CC} = 0 V.

MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages with respect to pin GND (pin 4).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC} to GND	Supply voltage range V_{CC}	–0.3	+18	V
V_{bus}	Voltage range on I^2C Bus, SDA or SCL	–0.3	+18	V
V_{Tx}	Voltage range on buffered output	–0.3	+18	V
V_{Rx}	Voltage range on receive input	–0.3	+18	V
I	DC current (any pin)	—	250	mA
R_{tot}	Power dissipation	—	300	mW
T_{stg}	Storage temperature range	–55	+125	°C
T_{amb}	Operating ambient temperature range	–40	+85	°C

CHARACTERISTICS

At T_{amb} = 25 °C; Voltages are specified with respect to GND with V_{CC} = 5 V unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supply						
V_{CC}	Supply voltage (operating)		2.0	—	15	V
I_{CC}	Supply current, buses HIGH		—	0.9	1.8	mA
I_{CC}	Supply current at V_{CC} = 15 V, buses HIGH		—	1.1	2.5	mA
I_{CC}	Additional supply current per Tx or Ty LOW		—	1.7	3.5	mA
Bus pull-up (load) voltages and currents						
V_{Sx}, V_{Sy}	Maximum input/output voltage level	Open collector; I^2C-bus and V_{Rx}, V_{Ry} = HIGH	—	—	15	V
I_{Sx}, I_{Sy}	Static output loading on I^2C-bus (Note 1)	V_{Sx}, V_{Sy} = 1.0 V; V_{Rx}, V_{Ry} = LOW	0.2	—	3	mA
I_{Sx}, I_{Sy}	Dynamic output sink capability on I^2C-bus	V_{Sx}, V_{Sy} > 2 V; V_{Rx}, V_{Ry} = LOW	7	18	—	mA
I_{Sx}, I_{Sy}	Leakage current on I^2C-bus	V_{Sx}, V_{Sy} = 5 V; V_{Rx}, V_{Ry} = HIGH	—	—	1	µA
I_{Sx}, I_{Sy}	Leakage current on I^2C-bus	V_{Sx}, V_{Sy} = 15 V; V_{Rx}, V_{Ry} = HIGH	—	1	—	µA
V_{Tx}, V_{Ty}	Maximum output voltage level	Open collector	—	—	15	V
I_{Tx}, I_{Ty}	Static output loading on buffered bus	V_{Tx}, V_{Ty} = 0.4 V; V_{Sx}, V_{Sy} = LOW on I^2C-bus = 0.4 V	—	—	30	mA
I_{Tx}, I_{Ty}	Dynamic output sink capability, buffered bus	V_{Tx}, V_{Ty} > 1 V V_{Sx}, V_{Sy} = LOW on I^2C-bus = 0.4 V	60	100	—	mA
I_{Tx}, I_{Ty}	Leakage current on buffered bus	V_{Tx}, V_{Ty} = V_{CC} = 15 V; V_{Sx}, V_{Sy} = HIGH	—	1	—	µA
Input Currents						
I_{Sx}, I_{Sy}	Input current from I^2C-bus	bus LOW V_{Rx}, V_{Ry} = HIGH	—	–1	—	µA
I_{Rx}, I_{Ry}	Input current from buffered bus	bus LOW V_{Rx}, V_{Ry} = 0.4 V	—	–1	—	µA
I_{Rx}, I_{Ry}	Leakage current on buffered bus input	V_{Rx}, V_{Ry} = V_{CC}	—	1	—	µA
Output Logic LOW Levels						
V_{Sx}, V_{Sy}	Output logic level LOW, on normal I^2C bus (Note 2)	I_{Sx}, I_{Sy} = 3 mA	0.8	0.88	1.0	V
V_{Sx}, V_{Sy}	Output logic level LOW, on normal I^2C bus (Note 2)	I_{Sx}, I_{Sy} = 0.2 mA	670	730	790	mV
dV_{Sx}/dT, dV_{Sy}/dT	Temperature coefficient of output LOW levels (Note 2)	I_{Sx}, I_{Sy} = 0.2 mA	—	–1.8	—	mV/K

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input logic switching threshold voltages						
V_{Sx}, V_{Sy}	Input logic voltage LOW (Note 3)	On normal I^2C-bus	—	640	600	mV
V_{Sx}, V_{Sy}	Input logic level HIGH threshold (Note 3)	On normal I^2C-bus	700	650	—	mV
dV_{Sx}/dT, dV_{Sy}/dT	Temperature coefficient of input thresholds		—	–2	—	mV/K
V_{Rx}, V_{Ry}	Input logic HIGH level	Fraction of applied V_{CC}	0.58	—	—	V
V_{Rx}, V_{Ry}	Input threshold	Fraction of applied V_{CC}	—	0.5	—	V
V_{Rx}, V_{Ry}	Input logic LOW level	Fraction of applied V_{CC}	—	—	0.42	V
Logic level threshold difference						
V_{Sx}, V_{Sy}	Input/Output logic level difference (Note 1)	V_{SX} output LOW at 0.2 mA – V_{SX} input HIGH max	50	85	—	mV

NOTES:
1. The minimum value requirement for pull-up current, 200 μA, guarantees that the minimum value for V_{SX} output LOW will always exceed the minimum V_{SX} input HIGH level to eliminate any possibility of latching. The specified difference is guaranteed by design within any IC. While the tolerances on absolute levels allow a small probability the LOW from one S_X output is recognized by an S_X input of another P82B96 this has no consequences for normal applications. In any design the S_X pins of different ICs should never be linked because the resulting system would be very susceptible to induced noise and would not support all I^2C operating modes.
2. The output logic LOW depends on the sink current. For scaling, see *Application Note AN255*.
3. The input logic threshold is independent of the supply voltage.

CHARACTERISTICS

At T_{amb} = 25 °C; Voltages are specified with respect to GND with V_{CC} = 5 V unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Bus Release on V_{CC} Failure						
V_{Sx}, V_{Sy}, V_{Tx}, V_{Ty}	V_{CC} voltage at which all buses are guaranteed to be released		—	—	1	V
dV/dT	Temperature coefficient of guaranteed release voltage		—	–4	—	mV/K
Buffer response time						
$T_{fall\ delay}$ V_{Sx} to V_{Tx} V_{Sy} to V_{Ty}	Buffer time delay on FALLING input between V_{Sx} = input switching threshold, and V_{Tx} output falling 50%.	R_{Tx} pull-up = 160 Ω, no capacitive load, V_{CC} = 5 V	—	70	—	ns
$T_{rise\ delay}$ V_{Sx} to V_{Tx} V_{Sy} to V_{Ty}	Buffer time delay on RISING input between V_{Sx} = input switching threshold, and V_{Tx} output reaching 50% V_{CC}	R_{Tx} pull-up = 160 Ω, no capacitive load, V_{CC} = 5 V	—	90	—	ns
$T_{fall\ delay}$ V_{Rx} to V_{Sx} V_{Ry} to V_{Sy}	Buffer time delay on FALLING input between V_{Rx} = input switching threshold, and V_{Sx} output falling 50%.	R_{Sx} pull-up = 1500 Ω, no capacitive load, V_{CC} = 5 V	—	250	—	ns
$T_{rise\ delay}$ V_{Rx} to V_{Sx} V_{Ry} to V_{Sy}	Buffer time delay on RISING input between V_{Rx} = input switching threshold, and V_{Sx} output reaching 50% V_{CC}	R_{Sx} pull-up = 1500 Ω, no capacitive load, V_{CC} = 5 V	—	270	—	ns
Input capacitance						
C_{in}	Effective input capacitance of any signal pin measured by incremental bus rise times		—	—	7	pF

NOTES ON RESPONSE TIME

The fall-time of V_{TX} from 5 V to 2.5 V in the test is approximately 15 ns.
The fall-time of V_{SX} from 5 V to 2.5 V in the test is approximately 50 ns.
The rise-time of V_{TX} from 0 V to 2.5 V in the test is approximately 20 ns.
The rise-time of V_{SX} from 0.9 V to 2.5 V in the test is approximately 70 ns.

TYPICAL APPLICATIONS

See *AN460* and *AN255* for more application detail.

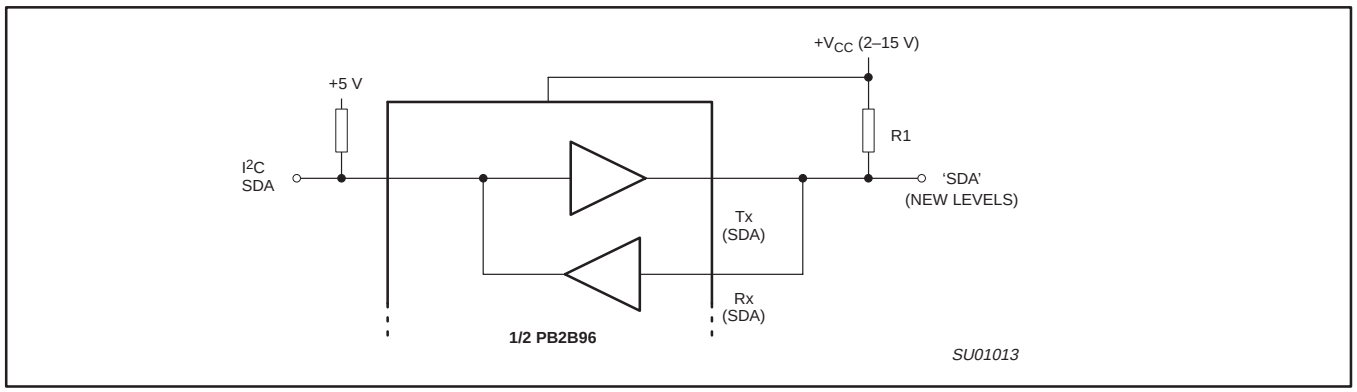


Figure 1. Interfacing an 'I²C' type of bus with different logic levels.

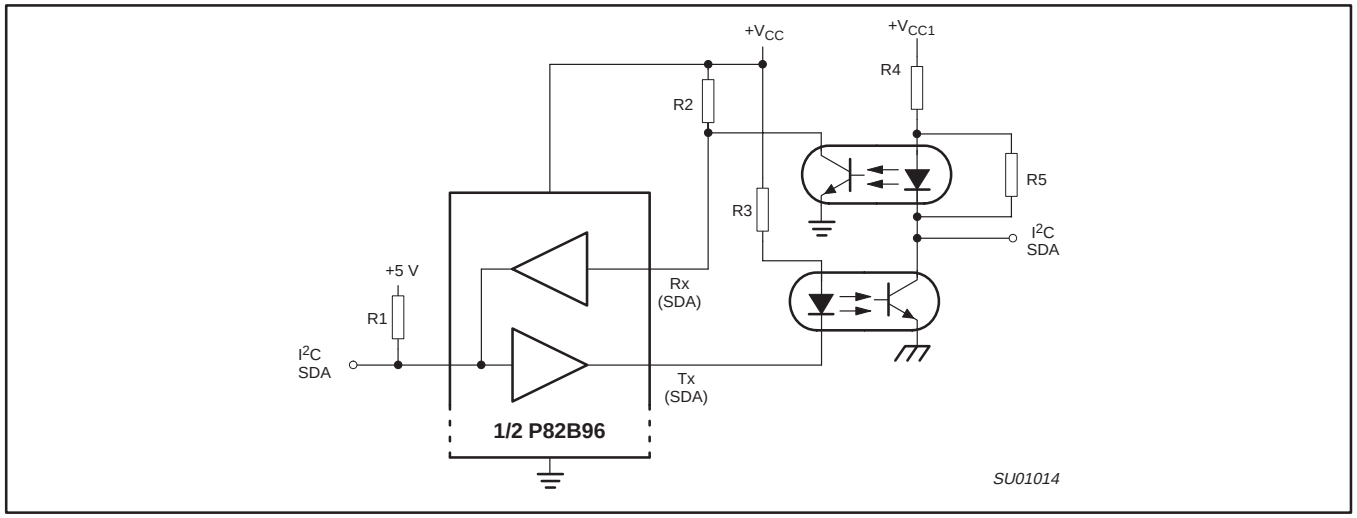


Figure 2. Galvanic isolation of I²C nodes via opto-couplers

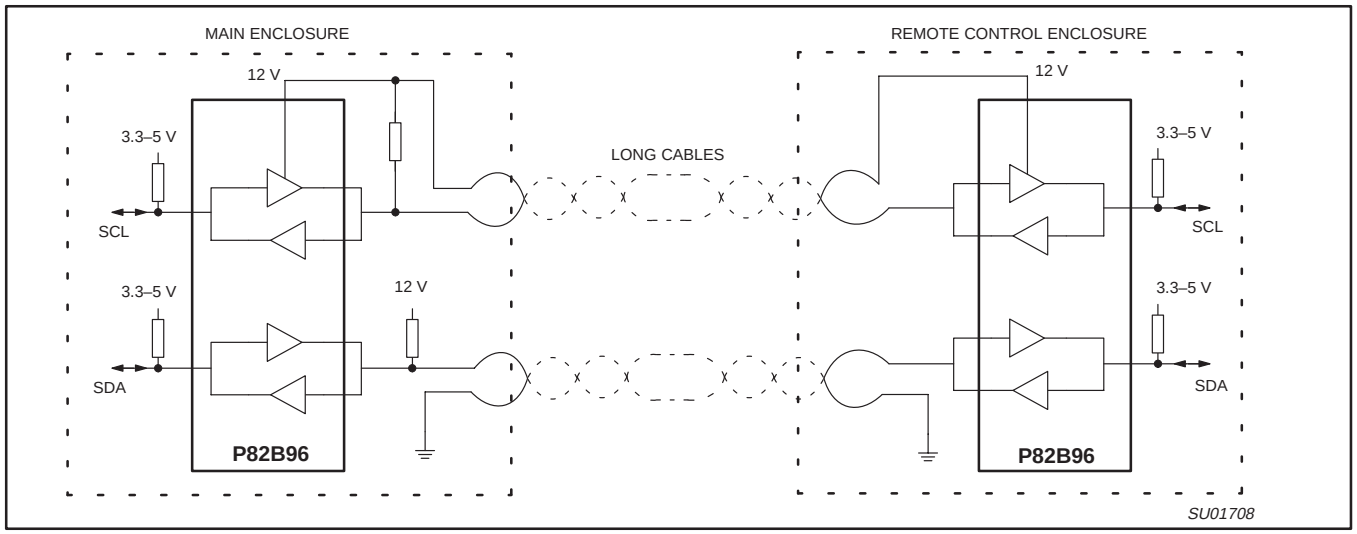


Figure 3. Long distance I²C communications

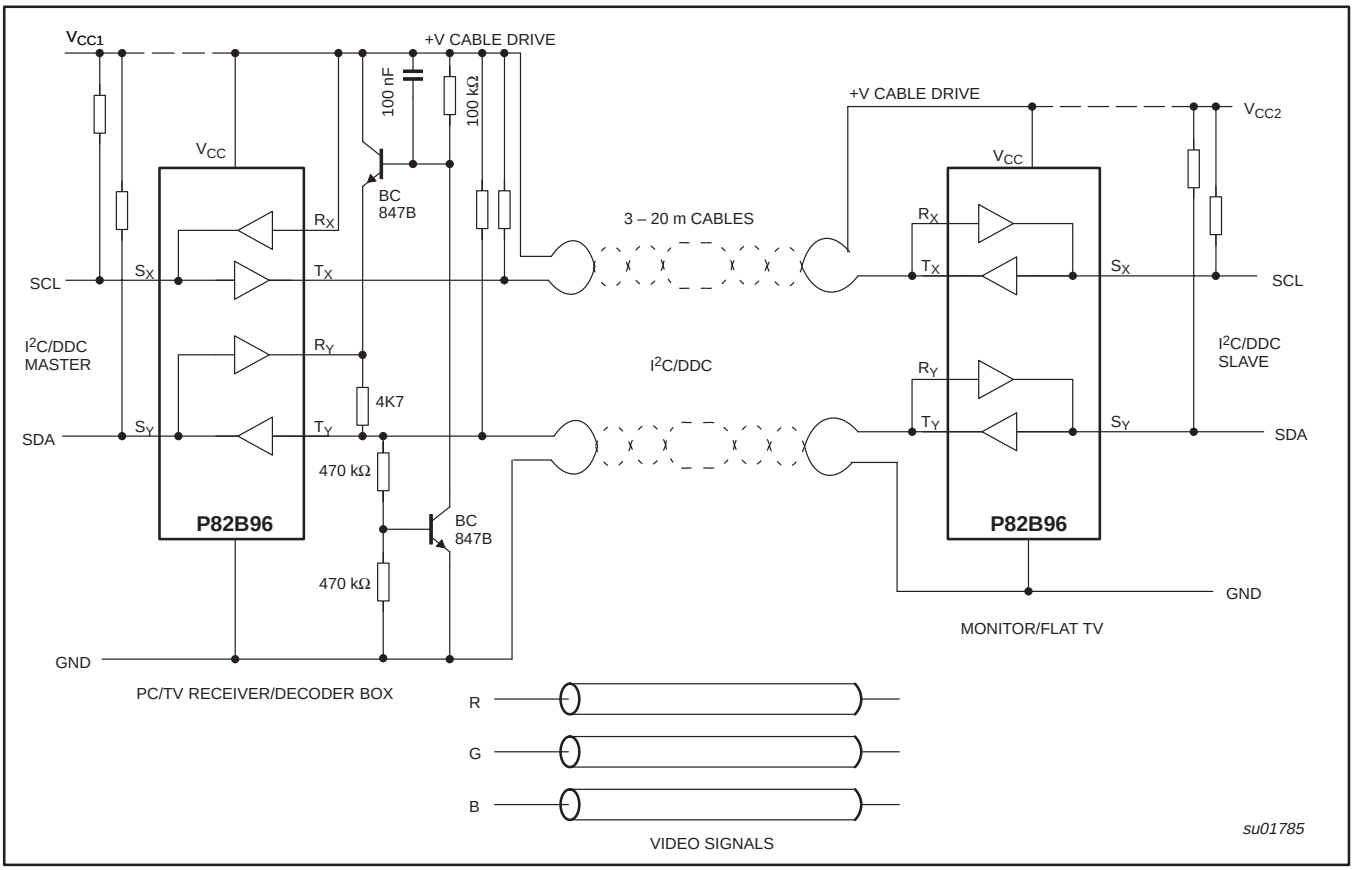


Figure 4. Extending a DCC bus

Figure 4 shows how a master I²C-bus can be protected against short circuits or failures in applications that involve plug/socket connections and long cables that may become damaged. A simple circuit is added to monitor the SDA bus and if its LOW time exceeds the design value then the master bus is disconnected. P82B96 will free all its I/Os if its supply is removed, so one option is to connect its V_{CC} to the output of a logic gate from, say, the 74LVC family. The SDA and SCL lines could be timed and V_{CC} disabled via the gate if one or other lines exceeds a design value of 'LOW' period as in *Figure 28 of AN255*. If the supply voltage of logic gates restricts the choice of V_{CC} supply then the low-cost discrete circuit in Figure 4 can be used. If the SDA line is held LOW, the 100 nF capacitor will charge and the R_y input will be pulled towards V_{CC}. When it exceeds $V_{CC}/2$ the R_y input will set the S_y input HIGH, which in practice means simply releasing it.

In this example the SCL line is made uni-directional by tying the R_x pin to V_{CC}. The state of the buffered SCL line cannot affect the master clock line which is allowed when clock-stretching is not required. It is simple to add an additional transistor or diode to control the R_x input in the same way as R_y when necessary. The +V cable drive can be any voltage up to 15 V and the bus may be run at a lower impedance by selecting pull-up resistors for a static sink current up to 30 mA. V_{CC1} and V_{CC2} may be chosen to suit the connected devices. Because DDC uses relatively low speeds (<100 kHz), the cable length is not restricted to 20 m by the I²C signalling, but it may be limited by the video signalling.

Figure 5 shows that P82B96 can achieve high clock rates over long cables. While calculating with lumped wiring capacitance yields reasonable approximations to actual timing, even 25 meters of cable is better treated using transmission line theory. Flat ribbon cables connected as shown, with the bus signals on the outer edge, will have a characteristic impedance in the range 100 – 200 Ω. For simplicity they cannot be terminated in their characteristic impedance but a practical compromise is to use the minimum pull-up allowed for P82B96 and place half this termination at each end of the cable. When each pull-up is below 330 Ω, the rising edge waveforms have their first voltage 'step' level above the logic threshold at Rx and cable timing calculations can be based on the fast rise/fall times of resistive loading plus simple one-way propagation delays. When the pull-up is larger, but below 750 Ω, the threshold at Rx will be crossed after one signal reflection. So at the sending end it is crossed after 2 times the one-way propagation delay and at the receiving end after 3 times that propagation delay. For flat cables with partial plastic dielectric insulation (by using outer cores) the one-way propagation delays will be about 5 ns/meter. The 10% to 90% rise and fall times on the cable will be between 20 ns and 50 ns, so their delay contributions are small. There will be ringing on falling edges that can be damped, if required, using Schottky diodes as shown.

When the Master SCL HIGH and LOW periods can be programmed separately, e.g. using control registers I2SCLH and I2SCLL of 89LPC932, the timings can allow for bus delays. The LOW period should be programmed to achieve the minimum 1300 ns plus the net delay in the slave's response data signal caused by bus and buffer delays. The longest data delay is the sum of the delay of the falling edge of SCL from master to slave and the delay of the rising edge of SDA from slave data to master. Because the buffer will 'stretch' the programmed SCL LOW period, the actual SCL

frequency will be lower than calculated from the programmed clock periods. In the example for 25 meters the clock is stretched 400 ns, the falling edge of SCL is delayed 490 ns and the SDA rising edge is delayed 570 ns. The required additional LOW period is (490 + 570) = 1060 ns and the I²C-bus specifications already include an allowance for a worst case bus risetime 0 to 70% of 425 ns. (The bus risetime can be 300 ns 30% to 70%, which means it can be 425 ns 0–70%. The 25-meter cable delay times as quoted already include all rise/fall times.) Therefore, the micro only needs to be programmed with an addtional (1060 – 400 – 425) = 235 ns, making a total programmed LOW period 1535 ns. The programmed LOW will the be stretched by 400 ns to yield an actual bus LOW time of 1935 ns, which, allowing the minimum HIGH period of 600 ns, yields a cycle period of 2535 ns or 394 kHz.

Note that in both the 100-meter and 250-meter examples the capacitive loading on the I²C-buses at each end is within the maximum allowed Standard mode loading of 400 pF, but exceeds the Fast mode limit. This is an example of a 'hybrid' mode because it relies on the response delays of Fast mode parts but uses (allowable) Standard mode bus loadings with rise times that contribute significantly to the system delays. The cables cause large propagation delays so these systems need to operate well below the 400 kHz limit but illustrate how they can still exceed the 100 kHz limit provided all parts are capable of Fast mode operation. The fastest example illustrates how the 400 kHz limit can be exceeded provided master and slave parts have delay specifications smaller than the maximum allowed. Many Philips slaves have delays shorter than 600 ns, but none have that guaranteed.

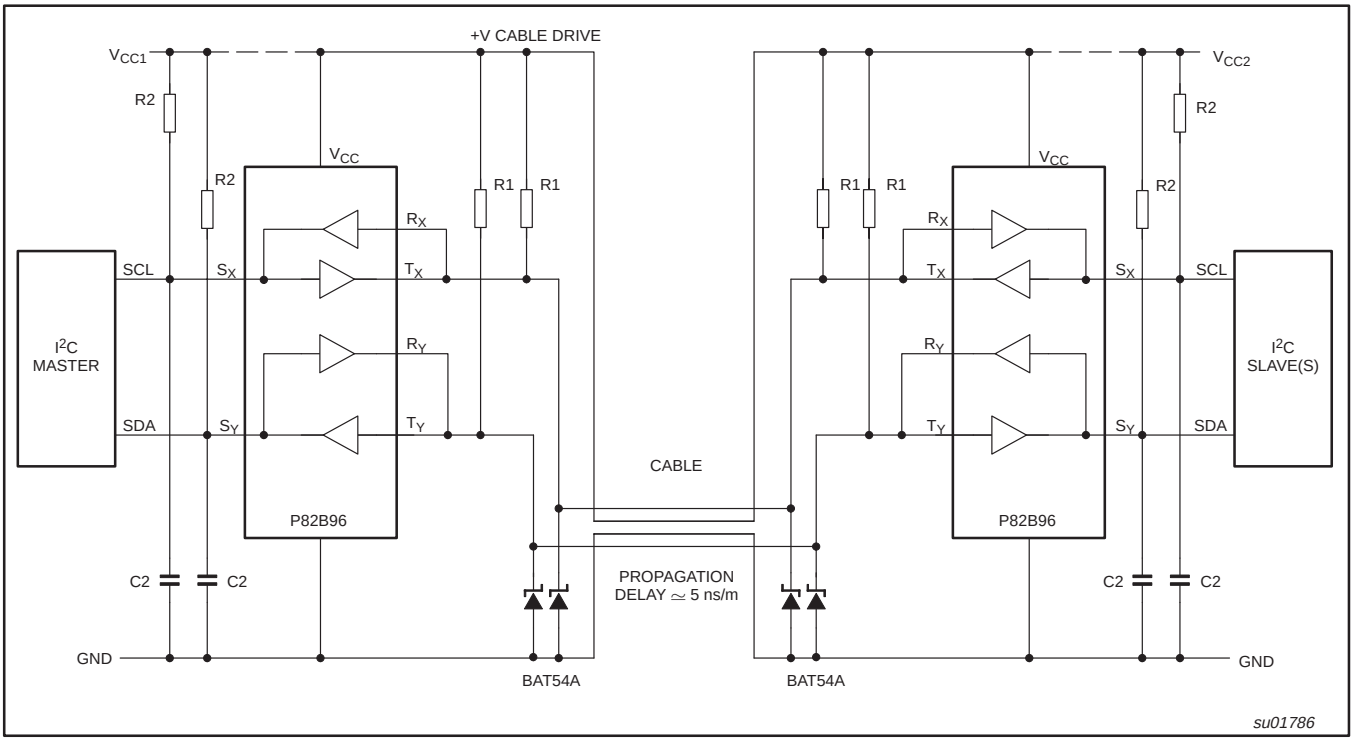


Figure 5. Driving ribbon or flat telephone cables

EXAMPLES OF BUS CAPABILITY (refer to Figure 5)

$+V_{CC1}$	+V CABLE	$+V_{CC2}$	R1	R2	C2 (pF)	CABLE LENGTH	CABLE CAPACITANCE	CABLE DELAY	SET MASTER NOMINAL SCL		EFFECTIVE BUS CLOCK SPEED	MAXIMUM SLAVE RESPONSE DELAY
									HIGH PERIOD	LOW PERIOD		
5 V	12 V	5 V	750	2.2 k	400	250 m	Not applicable (delay based)	1.25 µs	600 ns	4000 ns	120 kHz	Normal spec. 400 kHz parts
5 V	12 V	5 V	750	2.2 k	220	100 m	Not applicable (delay based)	500 ns	600 ns	2600 ns	185 kHz	Normal spec. 400 kHz parts
3.3 V	5 V	3.3 V	330	1 k	220	25 m	1 nF	125 ns	600 ns	1500 ns	390 kHz	Normal spec. 400 kHz parts
3.3 V	5 V	3.3 V	330	1 k	100	3 m	120 pF	15 ns	600 ns	1000 ns	500 kHz	600 ns

CALCULATING SYSTEM DELAYS AND BUS CLOCK FREQUENCY FOR A FAST MODE SYSTEM

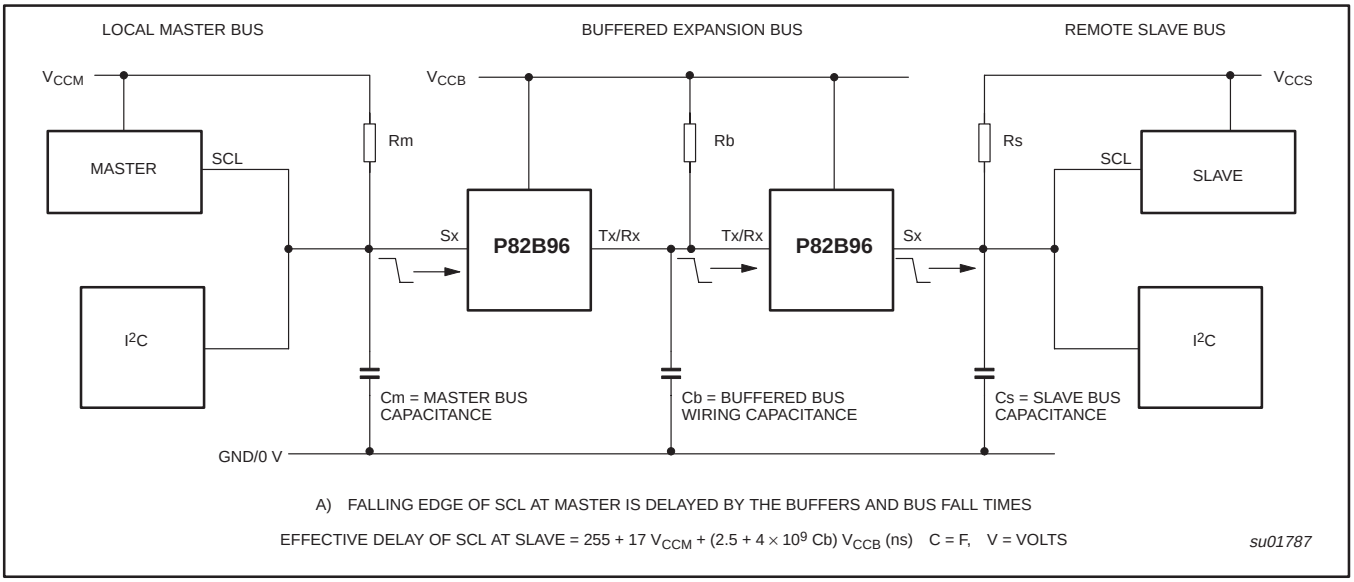


Figure 6.

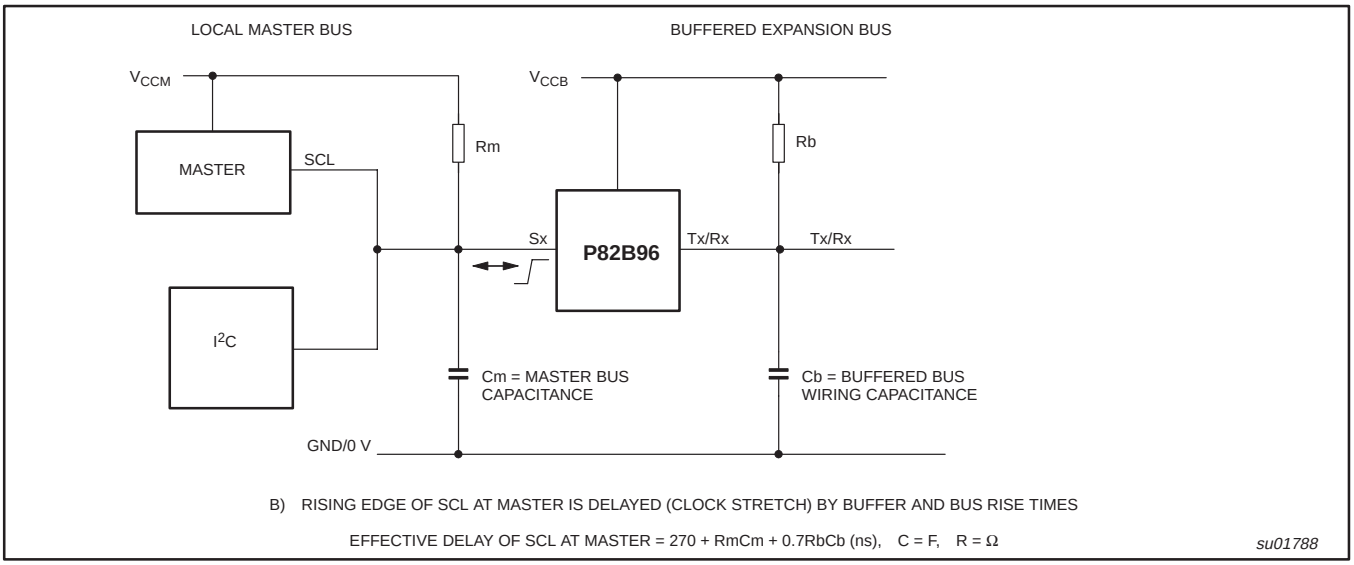


Figure 7.

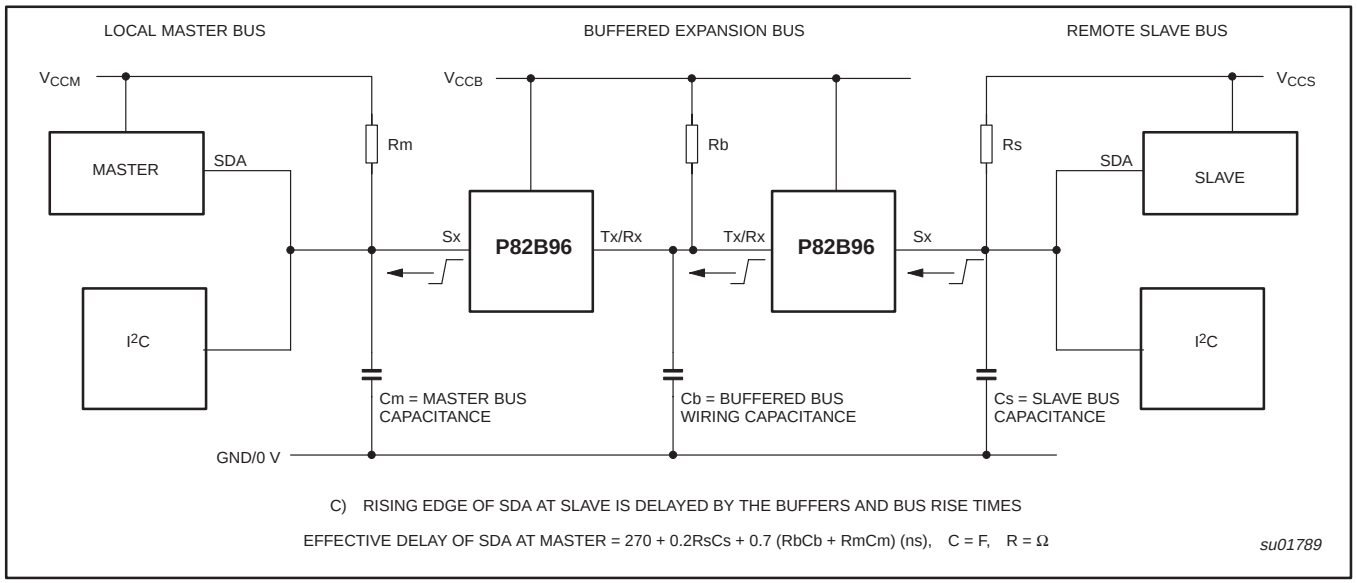


Figure 8.

Figures 6, 7, and 8 show the P82B96 used to drive extended bus wiring, with relatively large capacitance, linking two Fast mode I^2C-bus nodes. It includes simplified expressions for making the relevant timing calculations for 3.3/5 V operation. Because the buffers and the wiring introduce timing delays, it may be necessary to decrease the nominal SCL frequency below 400 kHz. In most cases the actual bus frequency will be lower than the nominal Master timing due to bit-wise stretching of the clock periods.

The delay factors involved in calculation of the allowed bus speed are:

A) The propagation delay of the Master signal through the buffers and wiring to the Slave. The important delay is that of the falling edge of SCL because this edge 'requests' the data or Acknowledge from a Slave.

B) The effective stretching of the nominal LOW period of SCL at the Master caused by the buffer and bus rise times

C) The propagation delay of the Slave's response signal through the buffers and wiring back to the Master. The important delay is that of a rising edge in the SDA signal. Rising edges are always slower and are therefore delayed by a longer time than falling edges. (The rising edges are limited by the passive pull-up while falling edges are actively driven)

The timing requirement in any I^2C system is that a Slave's data response (which is provided in response to a falling edge of SCL) must be received at the Master before the end of the corresponding low period of SCL as appears on the bus wiring at the Master. Since all Slaves will, as a minimum, satisfy the worst case timing requirements of a 400 kHz part, they must provide their response within the minimum allowed clock LOW period of 1300 ns. Therefore in systems that introduce additional delays it is only necessary to extend that minimum clock low period by any "effective" delay of the Slave's response. The effective delay of the slaves response = total delays in SCL falling edge from the Master reaching the Slave (A) – the effective delay (stretch) of the SCL rising edge (B) + total delays in the Slave's response data, carried on SDA, reaching the Master (C).

The Master microcontroller should be programmed to produce a nominal SCL LOW period = (1300 + A – B + C) ns, and should be programmed to produce the nominal minimum SCL HIGH period of 600 ns. Then a check should be made to ensure the cycle time is not shorter than the minimum 2500 ns. If found necessary, just increase either clock period.

Due to clock stretching, the SCL cycle time will always be longer than (600 + 1300 + A + C) ns.

Example:

The Master bus has an RmCm product of 100 ns and V_{CCM} = 5 V.

The buffered bus has a capacitance of 1 nF and a pull-up resistor of 160 ohms to 5 V giving an RbCb product of 160 ns. The Slave bus also has an RsCs product of 100 ns.

The microcontroller LOW period should be programmed to ≥ (1300 + 372.5 – 482 + 472) ns, that is ≥ 1662.5 ns.

Its HIGH period may be programmed to the minimum 600 ns.

The nominal microcontroller clock period will be ≥ (1662.5 + 600) ns = 2262.5 ns, equivalent to a frequency of 442 kHz.

The actual bus clock period, including the 482 ns clock stretch effect, will be below (nominal + stretch) = (2262.5 + 482) ns or ≥ 2745 ns, equivalent to an allowable frequency of 364 kHz.

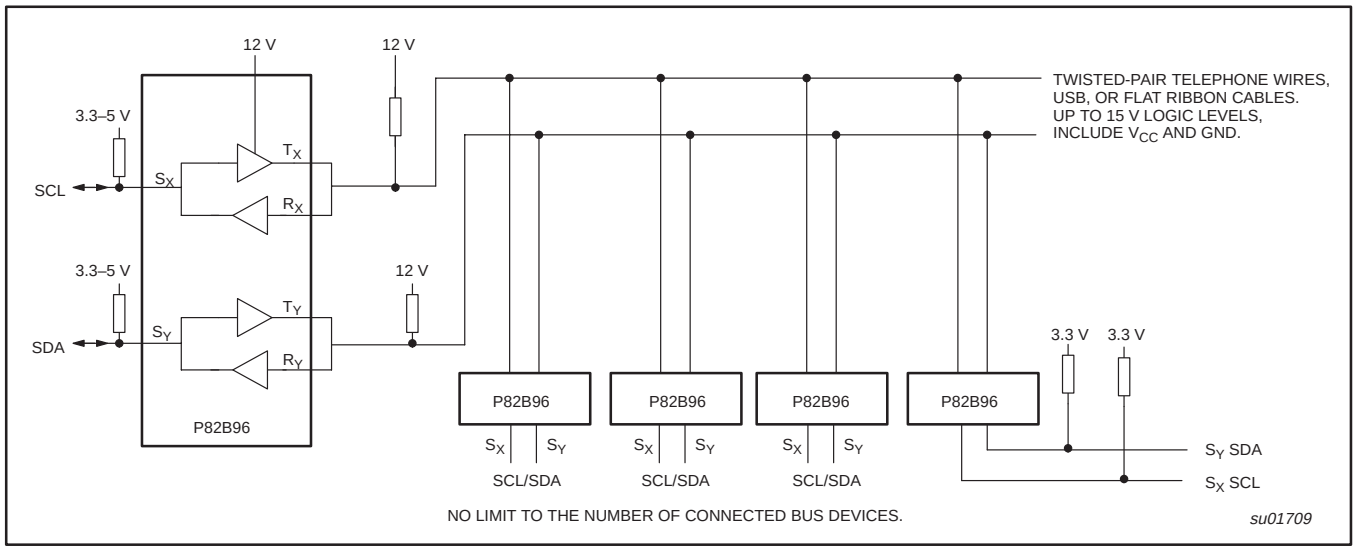


Figure 9. I²C multi-point applications

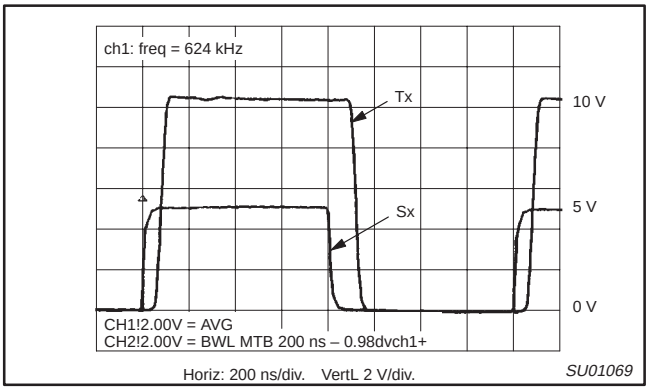


Figure 10. Propagation Sx to Tx — Sx pull-up to 5V, Tx pull-up to V_{CC} = 10 V

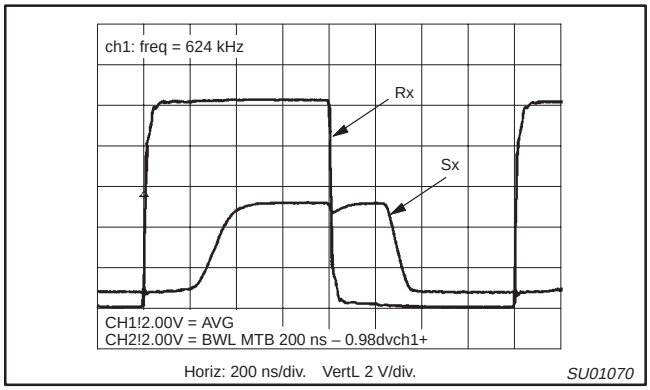
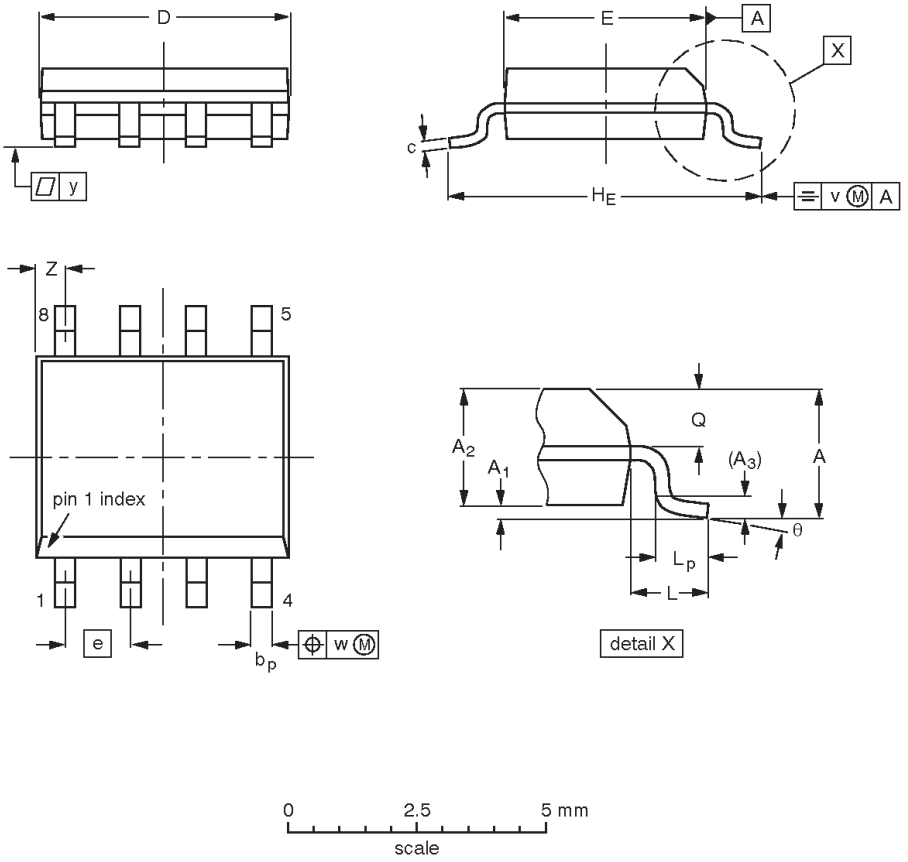


Figure 11. Propagation Rx to Sx — Sx pull-up to 5V, Rx pull-up to V_{CC} = 10 V

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

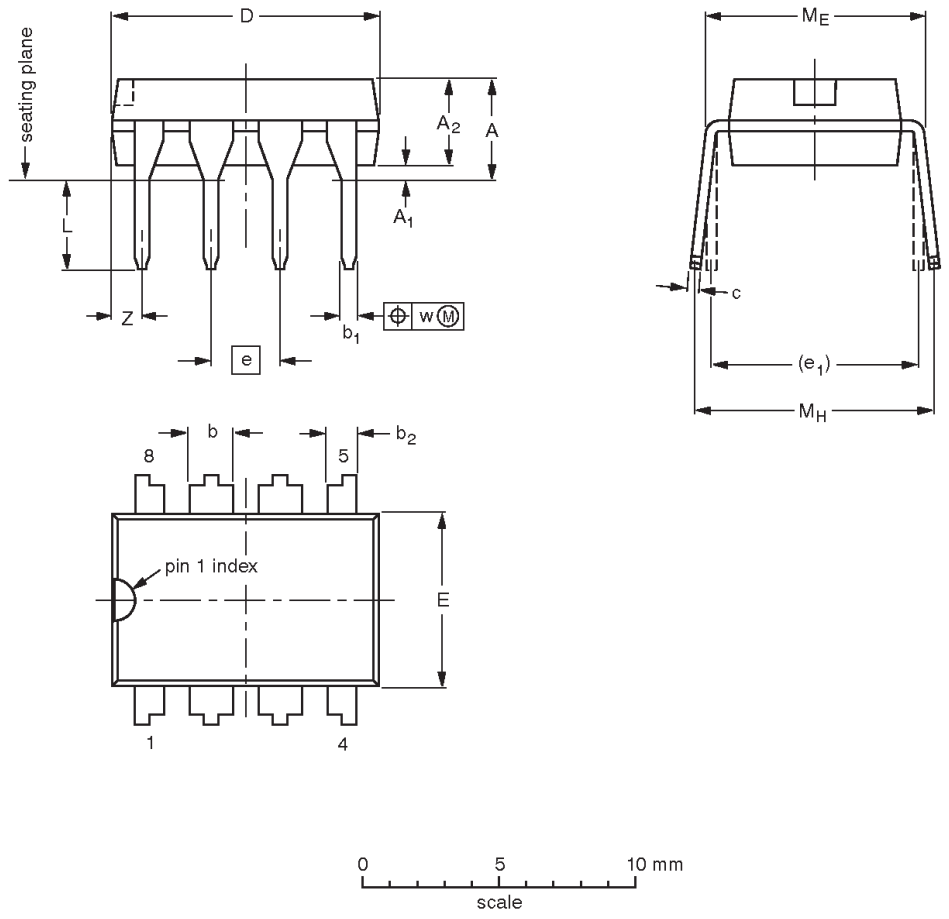
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

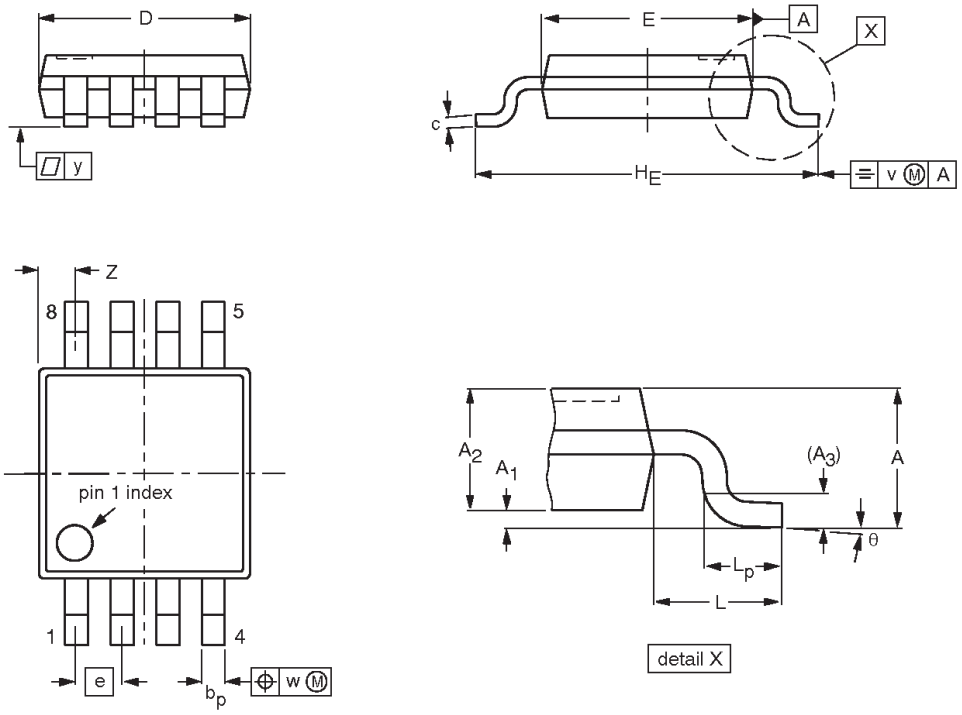
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

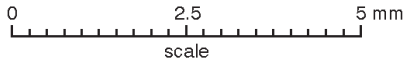
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

REVISION HISTORY

Rev	Date	Description
_4	20040326	**Product data (9397 750 12932). Supersedes data of 2003 Apr 02 (9397 750 11351).** Modifications: ● Page 2: – Features section re-written. – Add “TSSOP” to heading for pin configurations ● Page 3, Ordering information table: correct description of TSSOP8 package. ● Page 5, (continued) Characteristics table, Note 1, – third sentence: from “... the LOW from **on** S_X output ...” to “... the LOW from **one** S_X output ...” – fourth sentence: from “In any design the S_X pins of different ICs because the resulting ...” to “In any design the S_X pins of different ICs **should never be linked** because the resulting ...” ● Figure 4: Change 2 transistors to bipolar type. Add dashed line between V_{CC1} and V_{CC}, and between V_{CC2} and V_{CC} to indicate optional/allowed links. ● Figure 5: Add dashed line between V_{CC1} and V_{CC}, and between V_{CC2} and V_{CC} to indicate optional/allowed links. ● Page 8, table “Examples of bus capability”: – cable capacitance 1 nF: change LOW period from “1600 ns” to “1500 ns” change Effective bus clock speed from “380 kHz” to “390 kHz” – change cable capacitance “120 nF” to “120 pF” ● Add title “Calculating system delays and bus clock frequency for a Fast mode system” on page 9. ● Add V_{CCB} label to Figures 6, 7 and 8. ● Page 10, “Example:” paragraphs 3, 5 and 6: values corrected in equations. ● Add signal names to Figure 9. ● Add package outline drawing SOT505-1.
_3	20030402	**Product data (9397 750 11351); ECN 853-2241 29602 dated 28 February 2003. Supersedes data of 2003 Jan 22 (9397 750 11093)**
_2	20030226	**Product data (9397 750 11093); ECN 853-2241 29410 of 22 January 2003; supersedes data of 2001 Mar 06 (9397 750 08122)**
_1	20010306	**Product data (9397 750 08122); ECN 853-2241 25758 of 2001 Mar 06.**

Dual bi-directional bus buffer P82B96

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Date of release: 03-04

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