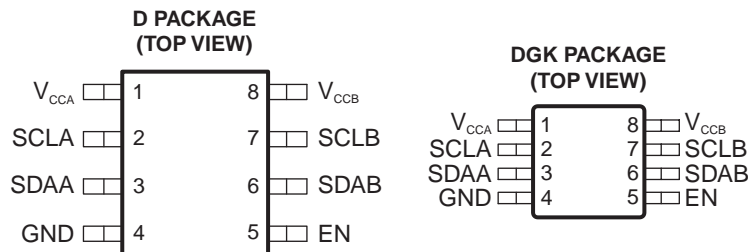


FEATURES

- Two-Channel Bidirectional Buffer
- I²C Bus and SMBus Compatible
- Operating Supply Voltage Range of 0.9 V to 5.5 V on A Side
- Operating Supply Voltage Range of 2.7 V to 5.5 V on B Side
- Voltage-Level Translation From 0.9 V to 5.5 V and 2.7 V to 5.5 V
- Footprint and Function Replacement for PCA9515A
- Active-High Repeater-Enable Input
- Open-Drain I²C I/O
- 5.5-V Tolerant I²C and Enable Input Support Mixed-Mode Signal Operation
- Lockup-Free Operation
- Accommodates Standard Mode and Fast Mode I²C Devices and Multiple Masters
- Supports Arbitration and Clock Stretching Across Repeater
- Powered-Off High-Impedance I²C Pins
- 400-kHz Fast I²C Bus
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

This dual bidirectional I²C buffer is operational at 2.7 V to 5.5 V.

The PCA9517 is a BiCMOS integrated circuit intended for I²C bus and SMBus systems. It can also provide bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables I²C and similar bus systems to be extended, without degradation of performance even during level shifting.

The PCA9517 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I²C bus, thus allowing two buses of 400-pF bus capacitance to be connected in an I²C application. This device can also be used to isolate two halves of a bus for voltage and capacitance.

The PCA9517 has two types of drivers—A-side drivers and B-side drivers. All inputs and I/Os are overvoltage tolerant to 5.5 V, even when the device is unpowered (V_{CCB} and/or V_{CCA} = 0 V).

ORDERING INFORMATION

T _A	PACKAGES ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tape and reel	PCA9517DR	PD517
	MSOP – DGK	Tape and reel	PCA9517DGKR	7EA

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The B-side drivers operate from 2.7 V to 5.5 V and behave like the drivers in the PCA9515A. This side also supports the standard low-level contention arbitration of the I²C bus and clock stretching. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released.

This type of design on the B side prevents it from being used in series with the PCA9515A and another PCA9517 (B side). This is because these devices do not recognize buffered low signals as a valid low and do not propagate it as a buffered low again.

The A-side drivers operate from 0.9 V to 5.5 V and drive more current. They do not require the buffered low feature (or the static offset voltage). This means that a low signal on the B side translates to a nearly 0-V low on the A side, which accommodates smaller voltage swings of lower-voltage logic. The output pulldown on the A side drives a hard low, and the input level is set at $0.3 V_{CCA}$ to accommodate the need for a lower low level in systems where the low-voltage-side supply voltage is as low as 0.9 V.

The A side of two or more PCA9517s can be connected together to allow a star topography, with the A side on the common bus. Also, the A side can be connected directly to any other buffer with static- or dynamic-offset voltage. Multiple PCA9517s can be connected in series, A side to B side, with no buildup in offset voltage and with only time-of-flight delays to consider.

The PCA9517 drivers are enabled when V_{CCA} is above 0.8 V and V_{CCB} is above 2.5 V.

The PCA9517 has an active-high enable (EN) input with an internal pullup to V_{CCB} , which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. It should never change state during an I²C operation, because disabling during a bus operation hangs the bus, and enabling part way through a bus cycle could confuse the I²C parts being enabled. The EN input should change state only when the global bus and repeater port are in an idle state, to prevent system failures.

The PCA9517 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. V_{CCB} and V_{CCA} can be applied in any sequence at power up. After power up and with the EN high, a low level on the A side (below $0.3 V_{CCA}$) turns the corresponding B-side driver (either SDA or SCL) on and drives the B side down to approximately 0.5 V. When the A side rises above $0.3 V_{CCA}$, the B-side pulldown driver is turned off and the external pullup resistor pulls the pin high. When the B side falls first and goes below $0.3 V_{CCB}$, the A-side driver is turned on and the A side pulls down to 0 V. The B-side pulldown is not enabled unless the B-side voltage goes below 0.4 V. If the B-side low voltage does not go below 0.5 V, the A-side driver turns off when the B-side voltage is above $0.7 V_{CCB}$. If the B-side low voltage goes below 0.4 V, the B-side pulldown driver is enabled, and the B side is able to rise to only 0.5 V until the A side rises above $0.3 V_{CCA}$. Then the B side continues to rise, being pulled up by the external pullup resistor. V_{CCA} is only used to provide the $0.3 V_{CCA}$ reference to the A-side input comparators and for the power-good-detect circuit. The PCA9517 logic and all I/Os are powered by the V_{CCB} pin.

As with the standard I²C system, pullup resistors are required to provide the logic-high levels on the buffered bus. The PCA9517 has standard open-collector configuration of the I²C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with Standard mode and Fast mode I²C devices in addition to SMBus devices. Standard mode I²C devices only specify 3 mA in a generic I²C system, where Standard mode devices and multiple masters are possible. Under certain conditions, higher termination currents can be used.

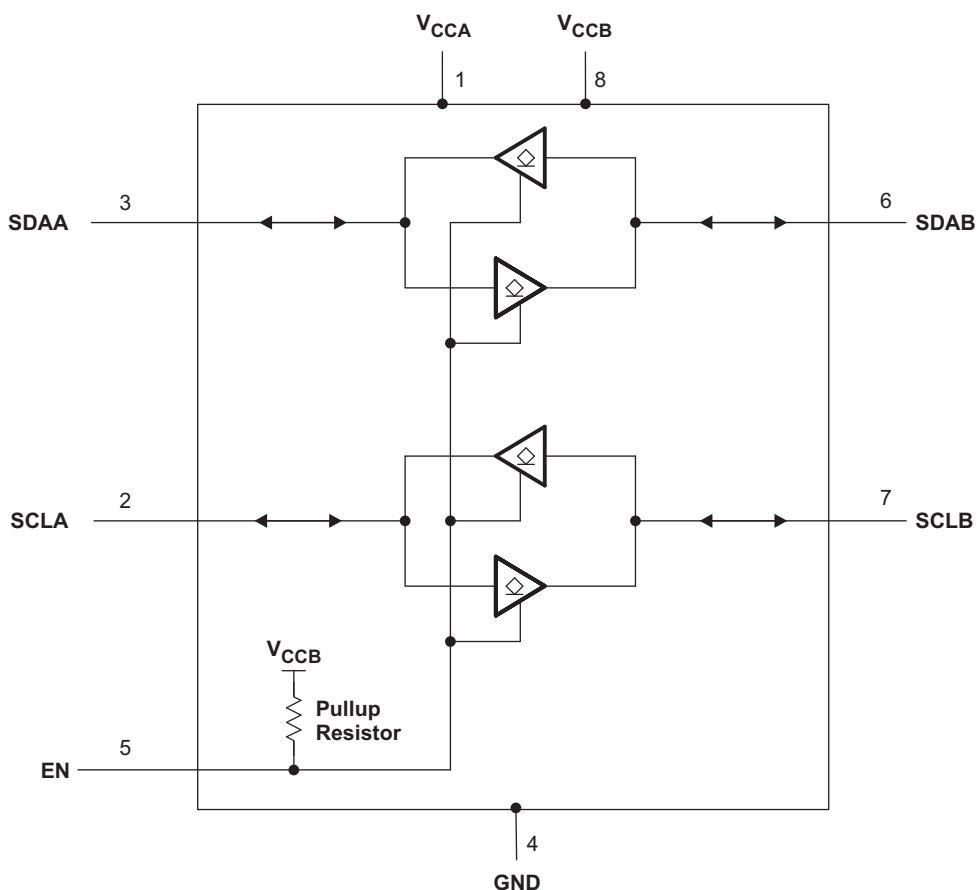
TERMINAL FUNCTIONS

NO.	NAME	DESCRIPTION
1	V _{CCA}	A-side supply voltage (0.9 V to 5.5 V)
2	SCLA	Serial clock bus, A side. Connect to V _{CCA} through a pullup resistor.
3	SDAA	Serial data bus, A side. Connect to V _{CCA} through a pullup resistor.
4	GND	Supply ground
5	EN	Active-high repeater enable input
6	SDAB	Serial data bus, B side. Connect to V _{CCB} through a pullup resistor.
7	SCLB	Serial clock bus, B side. Connect to V _{CCB} through a pullup resistor.
8	V _{CCB}	B-side and device supply voltage (2.7 V to 5.5 V)

FUNCTION TABLE

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

FUNCTIONAL BLOCK DIAGRAM



PCA9517 LEVEL-TRANSLATING I²C BUS REPEATER

SCPS157A—DECEMBER 2007—REVISED FEBRUARY 2008

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CCB}	Supply voltage range	-0.5	7	V
V _{CCA}	Supply voltage range	-0.5	7	V
V _I	Enable input voltage range ⁽²⁾	-0.5	7	V
V _{I/O}	I ² C bus voltage range ⁽²⁾	-0.5	7	V
I _{IK}	Input clamp current		-50	mA
I _{OK}	Output clamp current		-50	
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	
θ _{JA}	Package thermal impedance ⁽³⁾	D package	97	°C/W
		DGK package	172	
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JEDEC 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CCA}	Supply voltage, A-side bus	0.9 ⁽¹⁾	5.5	V
V _{CCB}	Supply voltage, B-side bus	2.7	5.5	V
V _{IH}	High-level input voltage	SDAA, SCLA	0.7 × V _{CCA}	5.5
		SDAB, SCLB	0.7 × V _{CCB}	5.5
		EN	0.7 × V _{CCB}	5.5
V _{IL}	Low-level input voltage	SDAA, SCLA	-0.5	0.28 × V _{CCA}
		SDAB, SCLB	-0.5 ⁽²⁾	0.3 × V _{CCB}
		EN	-0.5	0.3 × V _{CCB}
I _{OL}	Low-level output current	V _{CCB} = 2.7 V		6
		V _{CCB} = 3 V		6
T _A	Operating free-air temperature	-40	85	°C

- (1) Low-level supply voltage
- (2) V_{IL} specification is for the first low level seen by the SDAB and SCLB lines. V_{ILc} is for the second and subsequent low levels seen by the SDAB and SCLB lines.

Electrical Characteristics

V_{CCB} = 2.7 V to 5.5 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCB}	MIN	TYP	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = –18 mA	2.7 V to 5.5 V			–1.2	V
V _{OL}	Low-level output voltage	SDAB, SCLB I _{OL} = 100 μA or 6 mA, V _{ILA} = V _{ILB} = 0 V	2.7 V to 5.5 V	0.45	0.52	0.7	V
		SDAA, SCLA I _{OL} = 6 mA			0.1	0.2	
V _{OL} – V _{ILC}	Low-level input voltage below low-level output voltage	SDAB, SCLB	2.7 V to 5.5 V			70	mV
V _{ILC}	SDA and SCL low-level input voltage contention	SDAB, SCLB	2.7 V to 5.5 V	–0.5	0.4		V
I _{CC}	Quiescent supply current for V _{CCA}	Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND				1	mA
I _{CC}	Quiescent supply current	Both channels high, SDAA = SCLA = V _{CCA} and SDAB = SCLB = V _{CCB} and EN = V _{CCB}	5.5 V		1.5	4	mA
		Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND			1.5	5	
		In contention, SDAA = SCLA = GND and SDAB = SCLB = GND			1.5	5	
I _I	Input leakage current	SDAB, SCLB	2.7 V to 5.5 V	V _I = V _{CCB}		±1	μA
				V _I = 0.2 V		10	
		SDAA, SCLA		V _I = V _{CCB}		±1	
				V _I = 0.2 V		10	
		EN		V _I = V _{CCB}		±1	
				V _I = 0.2 V		–10 –30	
I _{OH}	High-level output leakage current	SDAB, SCLB	2.7 V to 5.5 V			10	μA
		SDAA, SCLA		V _O = 3.6 V			
C _I	Input capacitance	EN	V _I = 3 V or 0 V	3.3 V	6	7	pF
		SCLA, SCLB	V _I = 3 V or 0 V	3.3 V	6	9	
			0 V		6	8	
C _{IO}	Input/output capacitance	SDAA, SDAB	V _I = 3 V or 0 V	3.3 V	6	9	pF
			0 V		6	8	

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t _{SU}	Setup time, EN high before Start condition ⁽¹⁾	100		ns
t _H	Hold time, EN high after Stop condition ⁽¹⁾	100		ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

PCA9517 LEVEL-TRANSLATING I²C BUS REPEATER

SCPS157A–DECEMBER 2007–REVISED FEBRUARY 2008

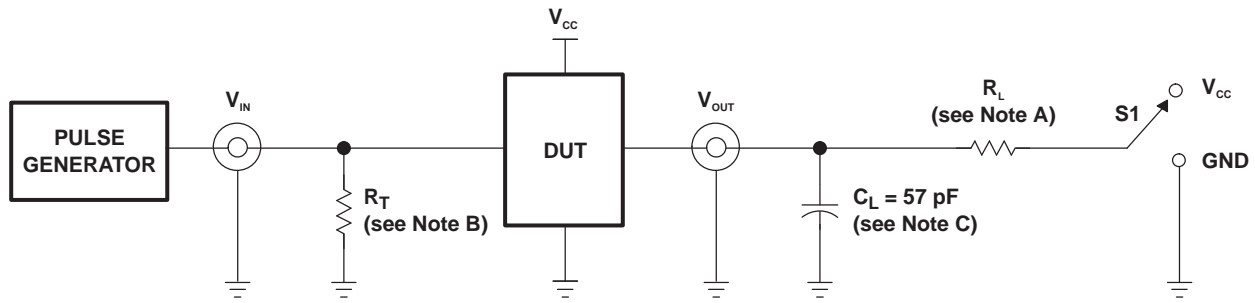
I²C Interface Timing Requirements

$V_{CCB} = 2.7\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
t _{PLZ}	Propagation delay	SDAB, SCLB ⁽²⁾ (see Figure 4)	SDAA, SCLA ⁽²⁾ (see Figure 4)		100	169	255	ns	
		SDAA, SCLA ⁽³⁾ (see Figure 3)	SDAB, SCLB ⁽³⁾ (see Figure 3)		25	67	110		
t _{PZL}	Propagation delay	SDAB, SCLB	SDAA, SCLA	$V_{CCA} \leq 2.7\text{ V}$ (see Figure 2)	15	68 ⁽⁴⁾	110	ns	
				$2.7\text{ V} \leq V_{CCA} \leq 3\text{ V}$ (see Figure 2)	20	79	130		
				$V_{CCA} \geq 3\text{ V}$ (see Figure 2)	10	103 ⁽⁵⁾	300		
		SDAA, SCLA ⁽³⁾ (see Figure 3)	SDAB, SCLB ⁽³⁾ (see Figure 3)		45	118	230		
t _{TLH}	Transition time	B side to A side (see Figure 3)	20%	80%		1	6	30	ns
		A side to B side (see Figure 2)				20	31	170	
t _{THL}	Transition time	B side to A side	80%	20%	$V_{CCA} \leq 2.7\text{ V}$ (see Figure 3)	1	3 ⁽⁴⁾	105	ns
					$2.7\text{ V} \leq V_{CCA} \leq 3\text{ V}$ (see Figure 2)	1	6	120	
					$V_{CCA} \geq 3\text{ V}$ (see Figure 3)	1	25 ⁽⁵⁾	175	
		A side to B side (see Figure 2)		1	12	90			

- (1) Typical values were measured with $V_{CCA} = V_{CCB} = 2.7\text{ V}$ at $T_A = 25^\circ\text{C}$, unless otherwise noted.
- (2) The t_{PLH} delay data from B to A side is measured at 0.5 V on the B side to 0.5 V_{CCA} on the A side when V_{CCA} is less than 2 V, and 1.5 V on the A side if V_{CCA} is greater than 2 V.
- (3) The proportional delay data from A to B side is measured at 0.3 V_{CCA} on the A side to 1.5 V on the B side.
- (4) Typical value measured with $V_{CCA} = 0.9\text{ V}$ at $T_A = 25^\circ\text{C}$
- (5) Typical value measured with $V_{CCA} = 5.5\text{ V}$ at $T_A = 25^\circ\text{C}$

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}

TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

- A. $R_L = 167 \Omega$ on the A side and $1.35 \text{ k}\Omega$ on the B side
- B. R_T termination resistance should be equal to Z_{OUT} of pulse generators.
- C. C_L includes probe and jig capacitance.
- D. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
- E. The outputs are measured one at a time, with one transition per measurement.
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- H. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 1. Test Circuit

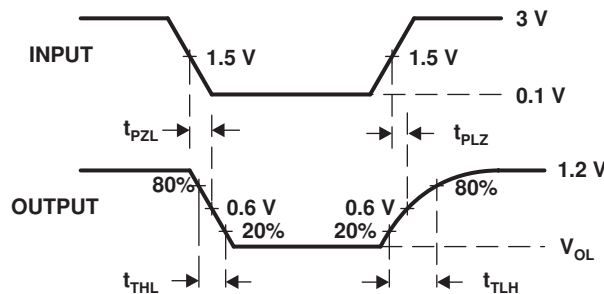


Figure 2. Waveform 1 – Propagation Delay and Transition Times for B Side to A Side

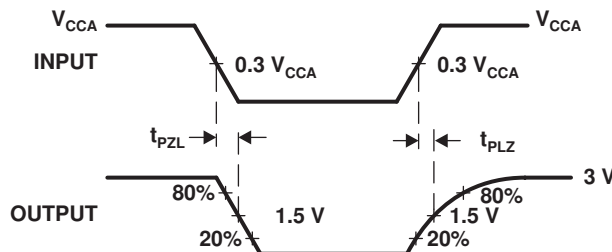


Figure 3. Waveform 2 – Propagation Delay and Transition Times for A Side to B Side

PARAMETER MEASUREMENT INFORMATION (continued)

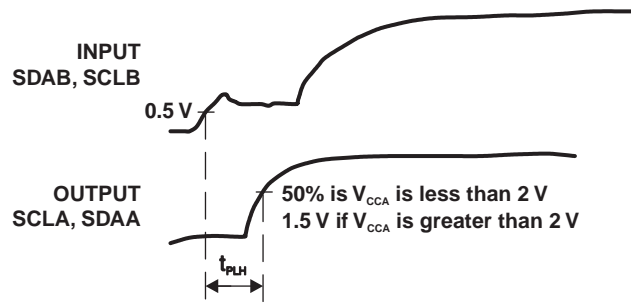


Figure 4. Waveform 3

APPLICATION INFORMATION

A typical application is shown in [Figure 5](#). In this example, the system master is running on a 3.3-V I²C bus, and the slave is connected to a 1.2-V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

The PCA9517 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9-V to 5.5-V bus voltages and 2.7-V to 5.5-V bus voltages.

When the A side of the PCA9517 is pulled low by a driver on the I²C bus, a comparator detects the falling edge when it goes below $0.3 V_{CCA}$ and causes the internal driver on the B side to turn on, causing the B side to pull down to about 0.5 V. When the B side of the PCA9517 falls, first a CMOS hysteresis-type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to [Figure 7](#) and [Figure 8](#). If the bus master in [Figure 5](#) were to write to the slave through the PCA9517, waveforms shown in [Figure 7](#) would be observed on the A bus. This looks like a normal I²C transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B-side bus of the PCA9517, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9517. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the PCA9517 for a short delay, while the A-bus side rises above $0.3 V_{CCA}$ and then continues high. It is important to note that any arbitration or clock stretching events require that the low level on the B-bus side at the input of the PCA9517 (V_{IL}) be at or below 0.4 V to be recognized by the PCA9517 and then transmitted to the A-bus side.

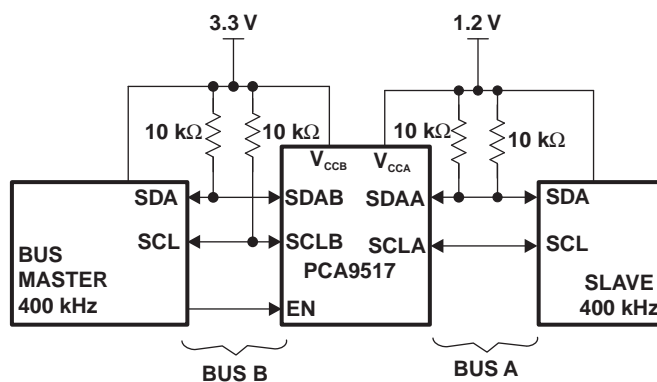


Figure 5. Typical Application

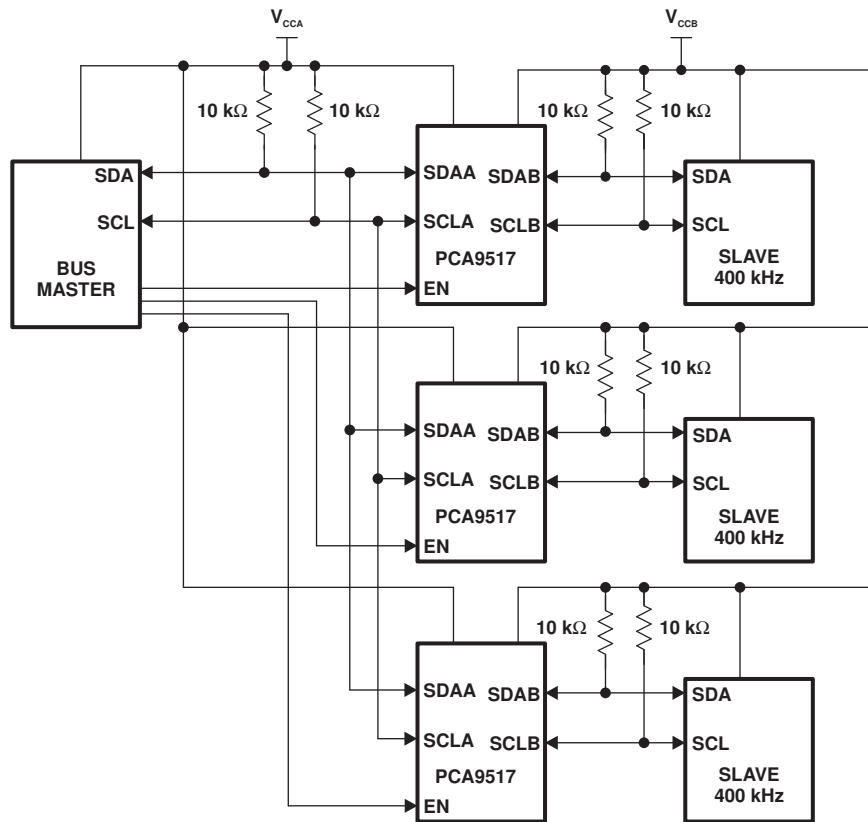


Figure 6. Typical Star Application

Multiple PCA9517 A sides can be connected in a star configuration, allowing all nodes to communicate with each other.

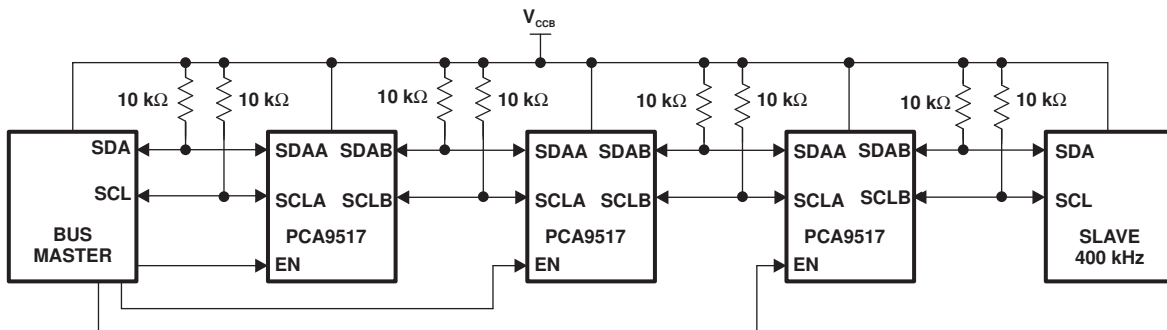


Figure 7. Typical Series Application

Multiple PCA9517s can be connected in series as long as the A side is connected to the B side. I²C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

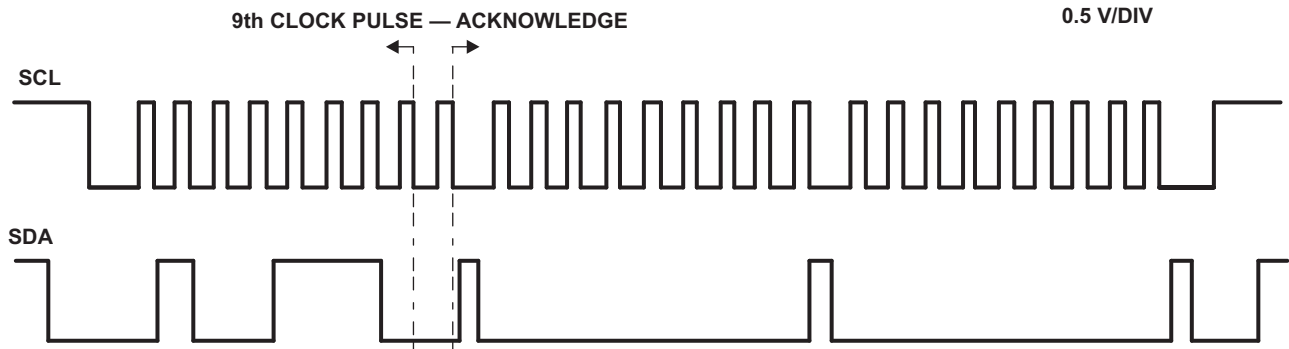


Figure 8. Bus A (0.9-V to 5.5-V Bus) Waveform

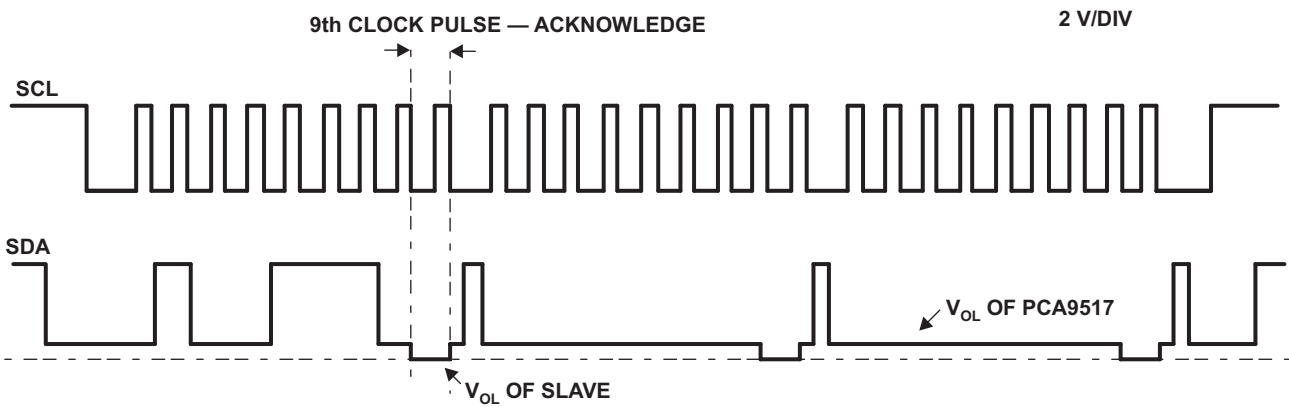


Figure 9. Bus B (2.7-V to 5.5-V Bus) Waveform

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
PCA9517D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9517DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9517DGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9517DGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9517DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9517DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9517DGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
PCA9517DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9517DGKR	MSOP	DGK	8	2500	358.0	335.0	35.0
PCA9517DR	SOIC	D	8	2500	346.0	346.0	29.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

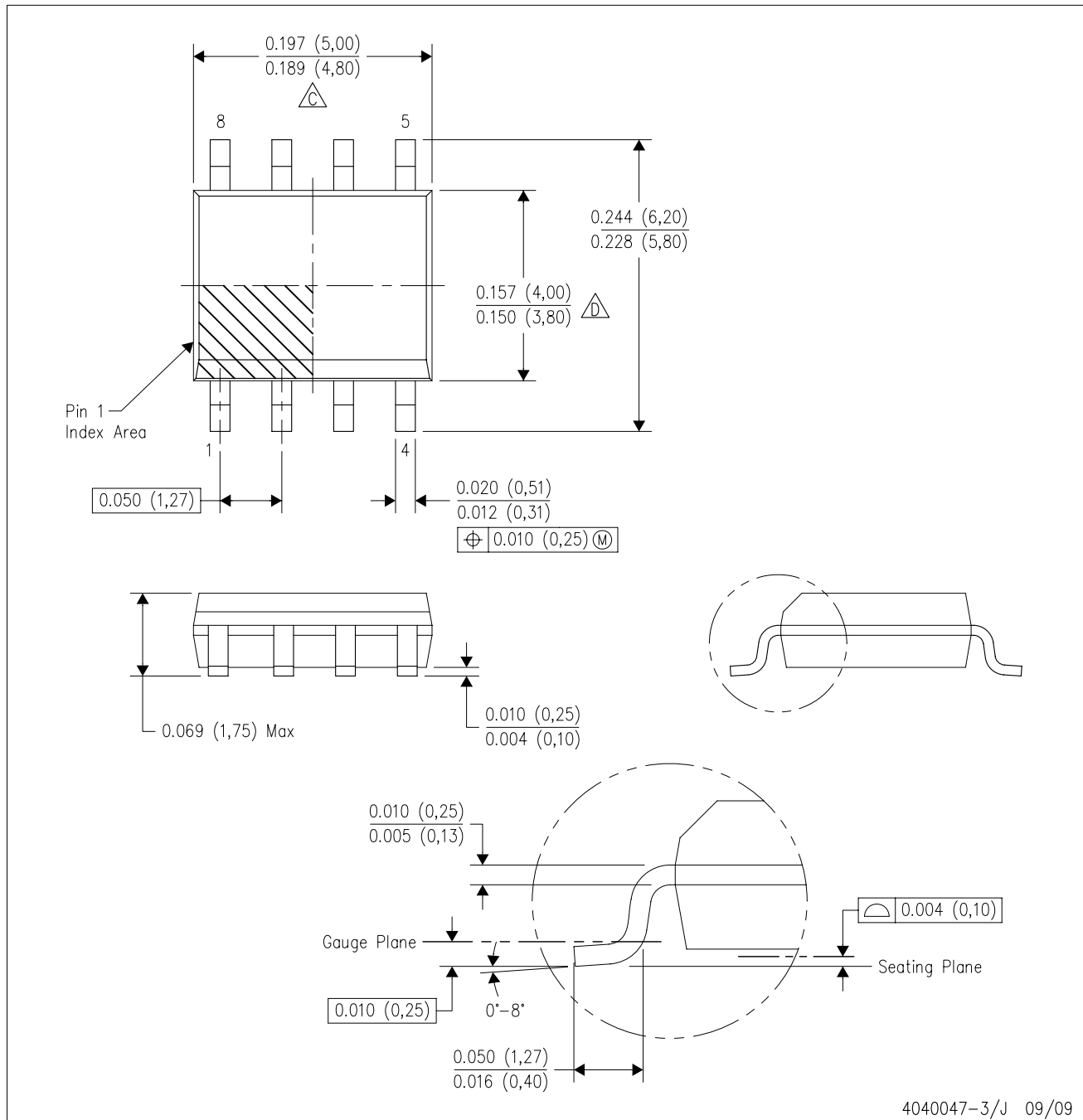


4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated