phyCORE-LPC3180

Preliminary

HARDWARE MANUAL

EDITION APRIL 2006

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Index of Figures

Index of Tables

1 Preface

This phyCORE-LPC3180 Hardware Manual describes the single board computer's design and functions. Precise specifications for the Philips LPC3180 microcontrollers can be found in the enclosed microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" preceding the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE-LPC3180

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-LPC3180 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. For more information go to:

http://www.phytec.com/services/phytec-advantage.html

1.1 Introduction

The phyCORE-LPC3180 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled Microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-LPC3180 is a subminiature (60 x 53 mm) insert-ready Single Board Computer populated with the Philips LPC3180 microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.635 mm) connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or datasheet. The descriptions in this manual are based on the Philips LPC3180. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-LPC3180.

The phyCORE-LPC3180 offers the following features:

- subminiature Single Board Computer (60 x 53 mm) achieved through modern SMD technology
- populated with the Philips LPC3180 microcontroller (LFBGA320 packaging)
- improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- controller signals and ports extend to two 100-pin high-density (0.635 mm) Molex connectors aligning two sides of the board, enabling it to be plugged like a "big chip" into target application
- max. 208 MHz core clock frequency
- 32 MByte (up to 128 MByte) on-board NAND Flash[1]
- 32 MByte (up to 64 MByte) SDRAM on-board, max. 1 MByte at 0 wait states[1]
- RS-232 transceivers supporting three UARTs at data rates of up to 460kbps
- 32KB I^2C EEPROM
- battery buffered controller based RTC with automatic battery switchover
- USB OTG transceiver
- processor independent watchdog with disable, normal, or extended modes
- one operating voltage for core & peripherals, 3.0V, typ. < 280 mA (with maximum circuitry installed at 208 MHz CPU frequency)
- controller required 0.9V, 1.2V, and 1.8V supplies generated on board
- support of ETM9 and EmbeddedICE-RT debug interface through JTAG connector
- keyboard support for up to 64 keys in a 8 * 8 matrix
- two SPI interfaces with DMA
- two PWM output channels with programmable duty cycle in 255 steps
- two I^2C interfaces
- SD card interface with DMA

1 : Please contact PHYTEC for more information about additional module configurations.

1.2 Block Diagram

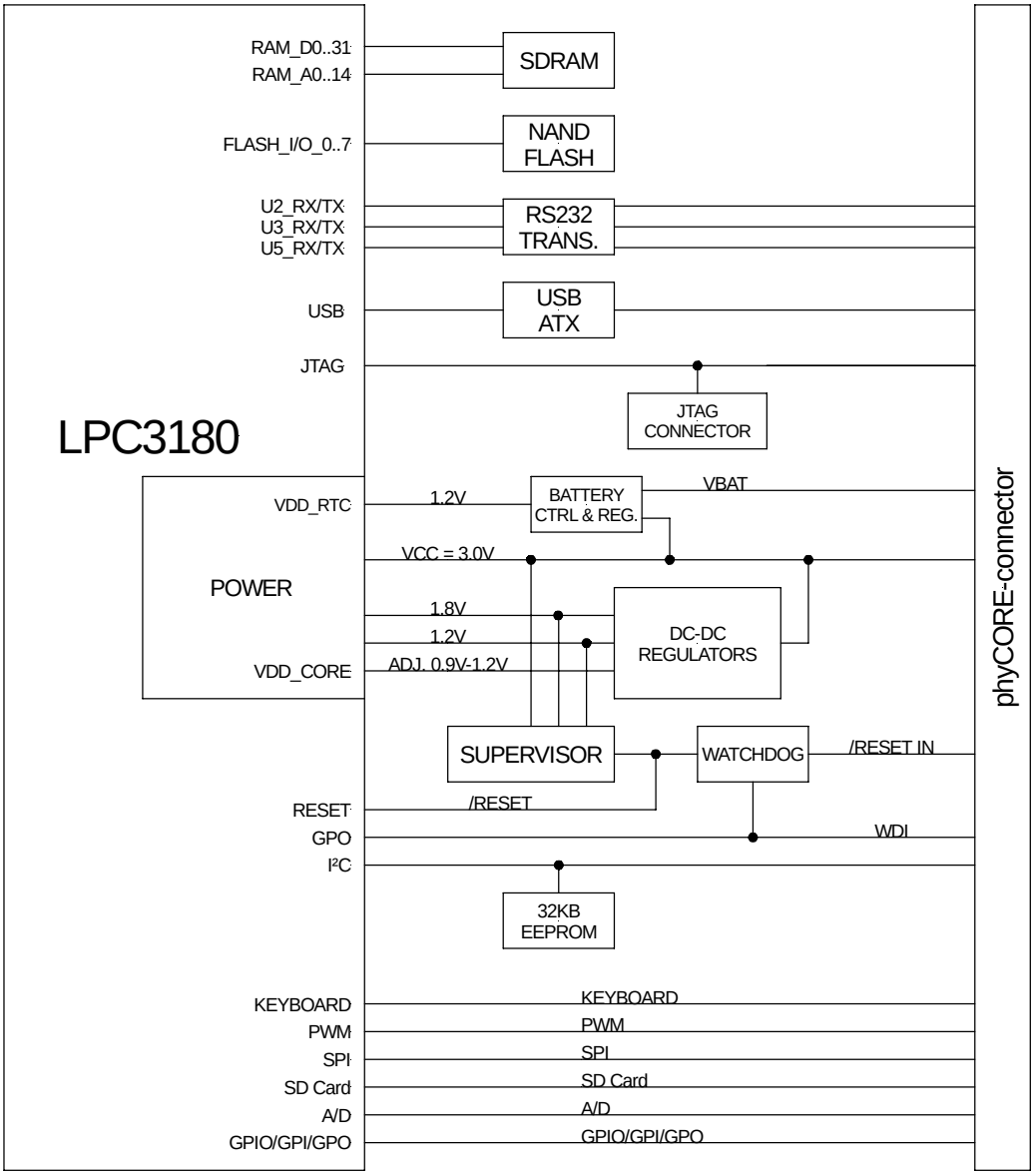

Figure 1: Block Diagram phyCORE-LPC3180

1.3 View of the phyCORE-LPC3180

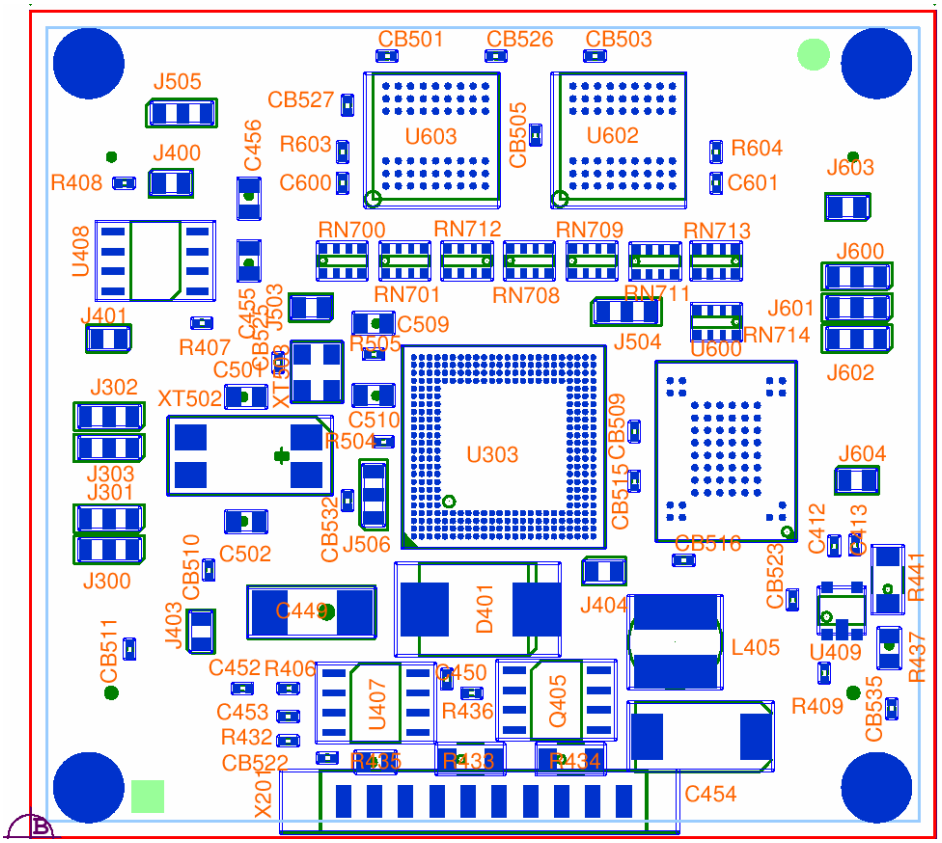

Figure 2: Top View of the phyCORE-LPC3180 (controller side)
[Generic image, not specific to phyCORE-LPC3180]

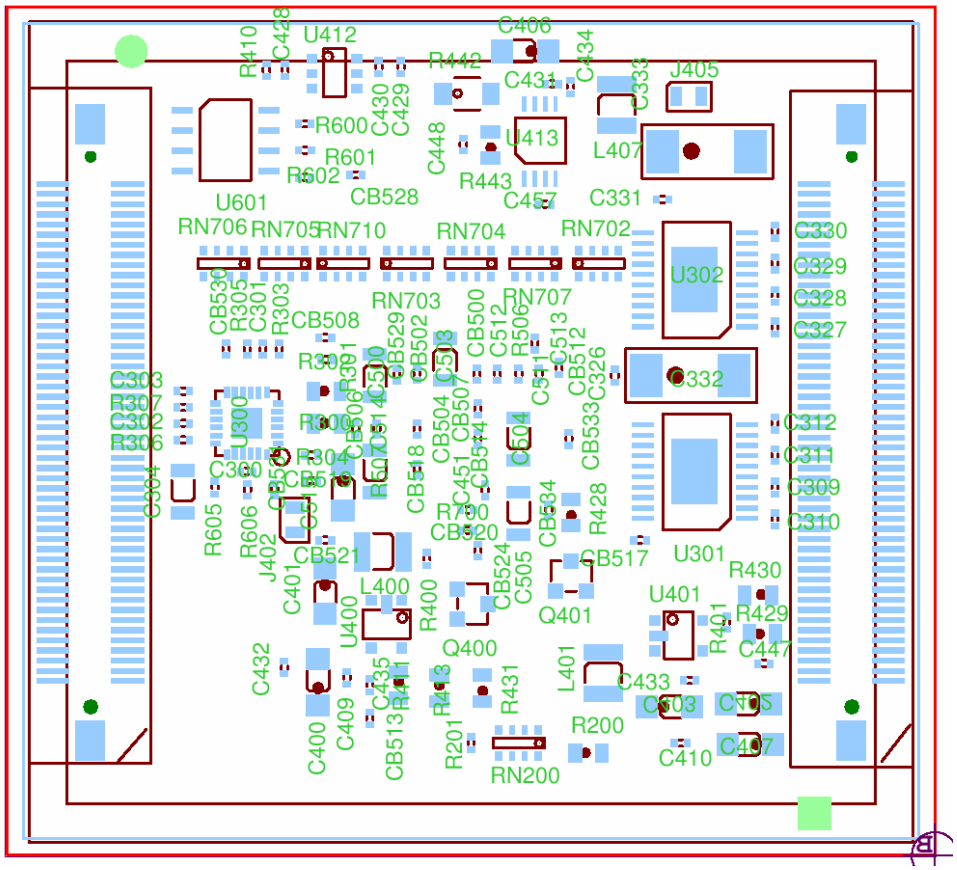

Figure 3: Bottom View of the phyCORE-LPC3180 (connector side)
[Generic image, not specific to phyCORE-LPC3180]

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector). This allows the phyCORE-LPC3180 to be plugged into any target application like a "big chip".

A new numbering scheme for the pins on the phyCORE-connector has been introduced with the phyCORE specifications. This enables quick and easy identification of desired pins and minimizes errors when matching pins on the phyCORE module with the phyCORE-connector on the appropriate PHYTEC Development Board or in user target circuitry.

The numbering scheme for the phyCORE-connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*refer to Figure 4*).

The numbered matrix can be aligned with the phyCORE-LPC3180 (viewed from above; phyCORE-connector pointing down) or with the socket of the corresponding phyCORE Development Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCORE-LPC3180 marked with a white triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module’s phyCORE-connector as well as mating connectors on the phyCORE Development Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCORE-connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector. The location of row 1 on the board is marked by a white triangle on the PCB to allow easy identification.

The following figure (*Figure 4*) illustrates the numbered matrix system. It shows a phyCORE-LPC3180 with SMT phyCORE-connectors on its underside (defined as dotted lines) mounted on a Development Board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCORE module showing these phyCORE-connectors mounted on the underside of the module’s PCB.

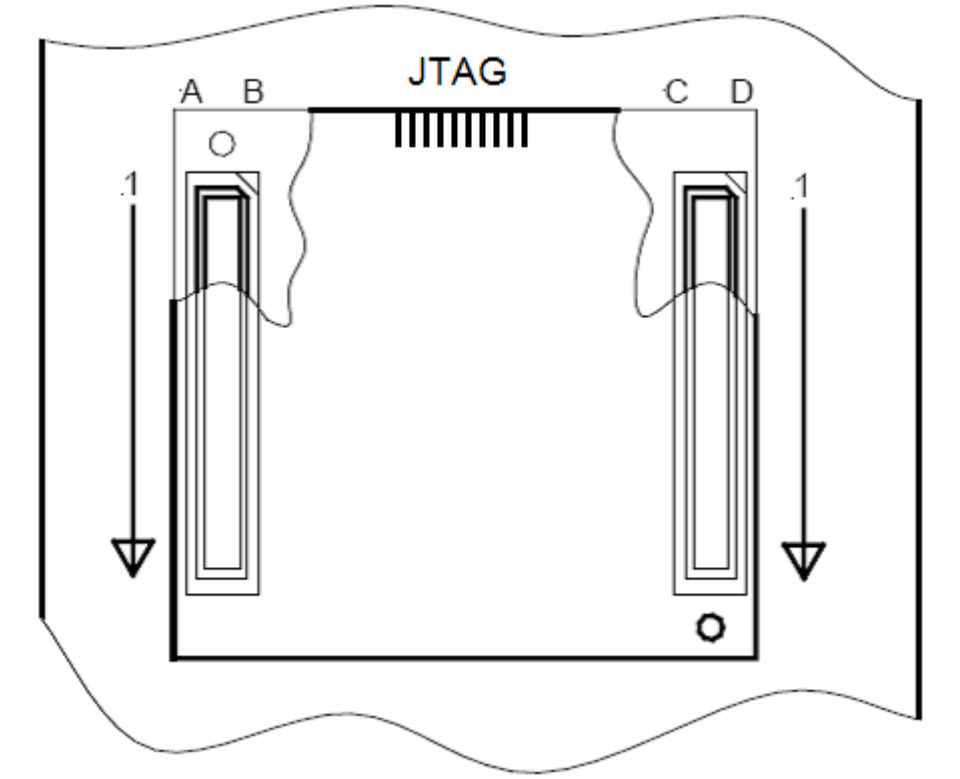

Figure 4: Pinout of the phyCORE-Connector (Top View, with Cross Section Insert)

Table 1 provides an overview of the pinout of the phyCORE-connector, as well as descriptions of possible alternative functions. Table 1 also provides the appropriate signal level interface voltages listed in the SL (**S**ignal **L**evel) column. The Philips LPC3180 is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. *Please refer to the Philips phyCORE-LPC3180 User's Manual/Data Sheet for details on the functions and features of controller signals and port pins*.

NOTE: SL is short for Signal Level (V) and is the applicable logic level to interface a given pin. Those pins marked as "N/A" have a range of applicable values that constitute proper operation.

Table 1: Pinout of the phyCORE-Connector X200

PIN ROW X200A				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1A	CLKIN	I	1.2	Optional external processor clock input[1]
2A	GND	-	0	Ground 0V
3A	KEY_COL2	I	3.0	Keyboard column 2 scan input pin of the µC
4A	KEY_COL3	I	3.0	Keyboard column 3 scan input pin of the µC
5A	KEY_COL4	I	3.0	Keyboard column 4 scan input pin of the µC
6A	GPI_8/KEY_COL6/ SPI2_BUSY	I	3.0	General purpose input 8 of the µC / keyboard column scan 6 input / SPI 2 busy input pin of the µC
7A	GND	-	0	Ground 0V
8A	KEY_ROW2	O	3.0	Keyboard row 2 scan output pin of the µC
9A	KEY_ROW3	O	3.0	Keyboard row 3 scan output pin of the µC
10A	KEY_ROW4	O	3.0	Keyboard row 4 scan output pin of the µC
11A	GPIO_2/KEY_ROW6	I/O	3.0	General purpose I/O 2 of the µC / keyboard row 6 scan output pin of the µC
12A	GND	-	0	Ground 0V
13A	GPI_3	I	1.8	General purpose input 3 pin of the µC
14A	GPI_5	I	3.0	General purpose input 5 pin of the µC
15A	GPI_6/ HSTIM_CAPTURE	I	3.0	General purpose input 6 / high-speed timer capture input pin of the µC
16A	GPI_11	I	3.0	General purpose input 11 pin of the µC
17A	GND	-	0	Ground 0V
18A	GPI_4/SPI1_BUSY	I	3.0	General purpose input 4 of the µC / SPI 1 busy input of the µC
19A	SPI2_DATIN	I	3.0	SPI 2 data input pin of the µC
20A	SPI2_CLK	I/O	3.0	SPI 2 clock pin of the µC
21A	MS_SCLK	I/O	3.0	SD card serial clock pin of the µC
22A	GND	-	0	Ground 0V
23A	MS_DIO2	I/O	3.0	SD card data I/O 2 pin of the µC
24A	MS_DIO3	I/O	3.0	SD card data I/O 3 pin of the µC
25A	USB_VBUS	I/O	5.0	VBUS I/O pin of the ISP1301 USB transceiver
26A	USB_ID	I/O	N/A	ID I/O pin of the ISP1301 USB transceiver
27A	GND	-	0	Ground 0V
28A	USB_DAT_VP/U5_RX	I/O	1.8	USB TX data / D- receive pin of the µC
29A	/USB_OE_TP	I/O	1.8	USB transmit enable for DAT / SE0 pin of the µC
30A	USB_I2C_SDA	I/O	1.8	I^2C SDA pin of the µC for ISP1301 USB transceiver

1: Optional capacitor C513 must be placed to use this input. Standard configurations do not have C513 populated.

31A	TST_CLK2	O	3.0	Test clock output pin of the µC
32A	GND	-	0	Ground 0V
33A	HIGHCORE	O	3.0	Core voltage select pin of the µC
34A	TDO	O	3.0	JTAG TDO pin of the µC
35A	TCK	I	3.0	JTAG TCK pin of the µC
36A	TDI	I	3.0	JTAG TDI pin of the µC
37A	GND	-	0	Ground 0V
38A	/PWROFF_CORE	I	3.0	VDD_CORE power control input
39A	/PWROFF_1V2	I	3.0	VDD_1V2 power control input
40A	/PWROFF_1V8	I	3.0	VDD_1V8 power control input
41A	Not connected	-	-	Unused
42A	GND	-	0	Ground 0V
43A	Not connected	-	-	Unused
44A	Not connected	-	-	Unused
45A	Not connected	-	-	Unused
46A	Not connected	-	-	Unused
47A	GND	-	0	Ground 0V
48A	Not connected	-	-	Unused
49A	Not connected	-	-	Unused
50A	Not connected	-	-	Unused

Pin Row X200B				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1B	MCKO	O	1.2	System clock output signal
2B	KEY_COL0	I	3.0	Keyboard column 0 scan input pin of the µC
3B	KEY_COL1	I	3.0	Keyboard column 1 scan input pin of the µC
4B	GND	-	0	Ground 0V
5B	KEY_COL5	I	3.0	Keyboard column 5 scan input pin of the µC
6B	GPI_9/KEY_COL7	I	3.0	General purpose input 9 / keyboard column 7 scan input pin of the µC
7B	KEY_ROW0	O	3.0	Keyboard row 0 scan output pin of the µC
8B	KEY_ROW1	O	3.0	Keyboard row 1 scan output pin of the µC
9B	GND		0	Ground 0V
10B	KEY_ROW5	O	3.0	Keyboard row 5 scan output pin of the µC
11B	GPIO_3/KEY_ROW7	I/O	0	General purpose I/O 3 / keyboard row 7 scan output pin of the µC
12B	GPI_0	I	3.0	General purpose input pin 0 of the µC
13B	GPI_2	I	3.0	General purpose input pin 2 of the µC
14B	GND	-	0	Ground 0V
15B	GPI_7	I	3.0	General purpose input pin 7 of the µC
16B	SPI1_CLK	O	3.0	SPI 1 clock pin of the µC
17B	SPI1_DATIN	I	3.0	SPI 1 data input pin of the µC
18B	SPI1_DATIO	I/O	3.0	SPI 1 data input/output pin of the µC
19B	GND	-	0	Ground 0V
20B	SPI2_DATIO	I/O	3.0	SPI 2 data input/output of the µC
21B	MS_BS	I/O	3.0	SD card serial bus state pin of the µC
22B	MS_DIO0	I/O	3.0	SD card data I/O 0 pin of the µC
23B	MS_DIO1	I/O	3.0	SD card data I/O 1 pin of the µC
24B	GND	-	0	Ground 0V
25B	USB_D-	I/O	N/A	USB D- pin of the ISP1301 USB transceiver
26B	USB_D+	I/O	N/A	USB D+ pin of the ISP1301 USB transceiver
27B	USB_SE0_VM/U5_TX	I/O	1.8	Single ended zero transmit/D- receive pin of the µC
28B	/USB_ATX_INT	I	1.8	Interrupt line of the µC for ISP1301 USB transceiver
29B	GND	-	0	Ground 0V
30B	USB_I2C_SCL	I/O	1.8	I^2C SCL pin of the µC for ISP1301 USB transceiver
31B	ONSW	O	1.2	VCCon output pin of the µC
32B	TEST	O	3.0	TEST pin of the µC
33B	SYSCLKEN	I/O	3.0	SYSCLKEN pin of the µC
34B	GND	-	0	Ground 0V
35B	RTCK	O	3.0	JTAG RTCK pin of the µC
36B	TMS	I	3.0	JTAG TMS pin of the µC
37B	/TRST		3.0	JTAG /TRST pin of the µC
38B	Not connected	-	-	Unused

39B	GND	-	0	Ground 0V
40B	Not connected	-	-	Unused
41B	Not connected	-	-	Unused
42B	Not connected	-	-	Unused
43B	Not connected	-	-	Unused
44B	GND	-	0	Ground 0V
45B	Not connected	-	-	Unused
46B	Not connected	-	-	Unused
47B	Not connected	-	-	Unused
48B	Not connected	-	-	Unused
49B	GND	-	0	Ground 0V
50B	Not connected	-	-	Unused

PIN ROW X200C				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1C	VCC	-	3.0	3.0V power input to the phyCORE-LPC3180
2C	VCC	-	3.0	3.0V power input to the phyCORE-LPC3180
3C	GND	-	0	Ground 0V
4C	Not connected	-	-	Unused
5C	Not connected	-	-	Unused
6C	VBAT	-	3.0	3.0V battery power supply input for the µC's RTC
7C	GND	-	0	Ground 0V
8C	Not connected	-	-	Unused
9C	GPI_1//SERVICE	I	3.0	General purpose input pin 1 of the µC / /SERVICE (boot) pin of the µC
10C	/RESET	O	1.2	Active low system reset signal generated by phyCORE reset circuitry
11C	/RESOUT	O	1.8	/RESOUT pin of the µC
12C	GND	-	0	Ground 0V
13C	GPIO_4	I/O	3.0	General purpose I/O pin 4 of the µC
14C	GPO_0/TST_CLK1	O	1.8	General purpose output pin 0 of the µC / TST_CLK1 pin of the µC
15C	GPO_1	O	1.8	General purpose output pin 1 of the µC
16C	GPO_3	O	3.0	General purpose output pin 3 of the µC
17C	GND	-	0	Ground 0V
18C	GPO_5	O	1.8	General purpose output pin 5 of the µC
19C	U5_RX	I	3.0	UART U5_RX pin of the µC
20C	U5_TX	O	3.0	UART U5_TX pin of the µC
21C	U5_RX_RS232	O	N/A	RS-232 level input to the MAX3380E RS-232 transceiver
22C	GND	-	0	Ground 0V
23C	U5_TX_RS232	O	N/A	RS-232 level output from the MAX3380E RS-232 transceiver
24C	U3_RX	I	3.0	UART U3_RX pin of the µC
25C	U3_TX	O	3.0	UART U3_TX pin of the µC
26C	U1_RX	I	3.0	UART U1_RX pin of the µC
27C	GND	-	0	Ground 0V
28C	U1_TX	O	3.0	UART U1_TX pin of the µC
29C	GPI_10/U4_RX	I	3.0	GPI_10 / U4_RX pin of the µC
30C	GPO_21/U4_TX	O	3.0	GPO_21 / U4_TX pin of the µC
31C	I2C1_SCL	I/O	3.0	I^2C1_SCL pin of the µC
32C	GND	-	0	Ground 0V
33C	U7_RX	I	3.0	UART U7_RX pin of the µC
34C	GPO_22/U7_HRTS	O	3.0	General purpose output pin 22 of the µC / U7_HRTS (handshake output) pin of the µC
35C	U7_HCTS	I	3.0	U7_HCTS (hardware flow control) pin of the µC
36C	PWM_OUT1	O	3.0	PWM_OUT1 pin of the µC

37C	GND	-	0	Ground 0V
38C	GPO_8	O	3.0	General purpose output pin 8 of the µC
39C	GPO_10	O	3.0	General purpose output pin 10 of the µC
40C	GPO_11	O	3.0	General purpose output pin 11 of the µC
41C	GPO_13	O	3.0	General purpose output pin 13 of the µC
42C	AGND	-	N/A	Analog Ground (floating, not connected to GND)
43C	GPO_16	O	3.0	General purpose output pin 16 of the µC
44C	GPO_18	O	3.0	General purpose output pin 18 of the µC
45C	GPO_19	O	1.8	General purpose output pin 19 of the µC
46C	Not connected	-	-	Unused
47C	AGND	-	N/A	Analog Ground (floating, not connected to GND)
48C	ADIN0	I	N/A	ADIN0 pin of the µC
49C	ADIN2	I	N/A	ADIN2 pin of the µC
50C	VSSad_ext	-	0	VSSad_ext pin of the µC

PIN ROW X200D				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1D	VCC	-	3.0	3.0V power input to the phyCORE-LPC3180
2D	VCC	-	3.0	3.0V power input to the phyCORE-LPC3180
3D	GND	-	0	Ground 0V
4D	Not connected	-	-	Unused
5D	Not connected	-	-	Unused
6D	VPD	-	1.2	Regulated battery / VCC output voltage to the µC's RTC power supply pins
7D	Not connected	-	-	Unused
8D	WDI	I	3.0	Watchdog input pin of the MAX6301 watchdog IC
9D	GND	-	0	Ground 0V
10D	/RESIN	I	3.0	Active low system reset input signal
11D	GPIO_0	I/O	3.0	General purpose I/O pin 0 of the µC
12D	GPIO_1	I/O	3.0	General purpose I/O pin 1 of the µC
13D	GPIO_5	I/O	3.0	General purpose I/O pin 5 of the µC
14D	GND	-	0	Ground 0V
15D	GPO_2	O	3.0	General purpose output pin 2 of the µC
16D	U2_RX	I	3.0	UART U2_RX pin of the µC
17D	U2_TX	O	3.0	UART U2_TX pin of the µC
18D	GPO_4	O	3.0	General purpose output pin 4 of the µC
19D	GND	-	0	Ground 0V
20D	GPO_6	O	3.0	General purpose output pin 6 of the µC
21D	GPO_7	O	3.0	General purpose output pin 7 of the µC
22D	U2_RX_RS232	I	N/A	RS-232 level input to the MAX3380E RS-232 transceiver
23D	U2_TX_RS232	O	N/A	RS-232 level output from the MAX3380E RS-232 transceiver
24D	GND	-	0	Ground 0V
25D	GPO_23/U2_HRTS	O	3.0	General purpose output pin 23 of the µC / U2_HRTS (handshake output) pin of the µC
26D	U2_HCTS	I	3.0	UART U2_HCTS (handshake input) pin of the µC
27D	U3_RX_RS232	I	N/A	RS232 level input to the MAX3380E RS232 transceiver
28D	U3_TX_RS232	O	N/A	RS232 level output from the MAX3380E RS232 transceiver
29D	GND	-	0	Ground 0V
30D	U6_IRRX	I	3.0	U6_IRRX pin of the µC
31D	U6_IRTX	O	3.0	U6_IRTX pin of the µC
32D	I2C1_SDA	I/O	3.0	I2C1_SDA pin of the µC
33D	U7_TX	O	3.0	U7_TX pin of the µC
34D	GND	-	-	Ground 0V
35D	I2C2_SCL	I/O	1.8	I2C2_SCL pin of the µC
36D	I2C2_SDA	I/O	1.8	I2C2_SDA pin of the µC
37D	PWM_OUT2	O	3.0	PWM_OUT2 pin of the µC

38D	GPO_9	O	3.0	GPO_9 pin of the µC
39D	GND	-	0	Ground 0V
40D	GPO_12	O	3.0	GPO_12 pin of the µC
41D	GPO_14	O	1.8	GPO_14 pin of the µC
42D	GPO_15	O	3.0	GPO_15 pin of the µC
43D	GPO_17	O	3.0	GPO_17 pin of the µC
44D	AGND	-	N/A	Analog Ground (not connected to GND)
45D	GPO_20	O	1.8	GPO_20 pin of the µC
46D	U2_HCTS_RS232	-	-	RS232 level output from the MAX3380E RS232 transceiver
47D	U2_HRTS_RS232	-	-	RS232 level output from the MAX3380E RS232 transceiver
48D	ADIN1	I	N/A	ADIN1 pin of the µC
49D	AGND	-	N/A	Analog Ground (not connected to GND)
50D	VDDad28_ext	-	N/A	VDDad28_ext pin of the µC

3 Jumpers

For configuration purposes, the phyCORE-LPC3180 has 19 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the solder jumper pads, while *Figure 6* and *Figure 7* indicate the location of the solder jumpers on the board. All but two solder jumpers are located on the top side of the module (opposite side of connectors). Table 2 below provides a functional summary of the solder jumpers, their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable section listed in the table.

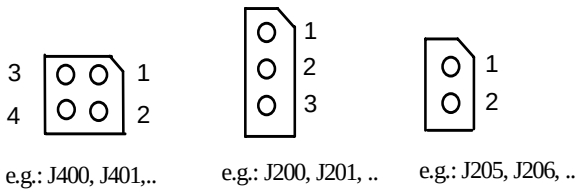

Figure 5: Numbering of the Jumper Pads

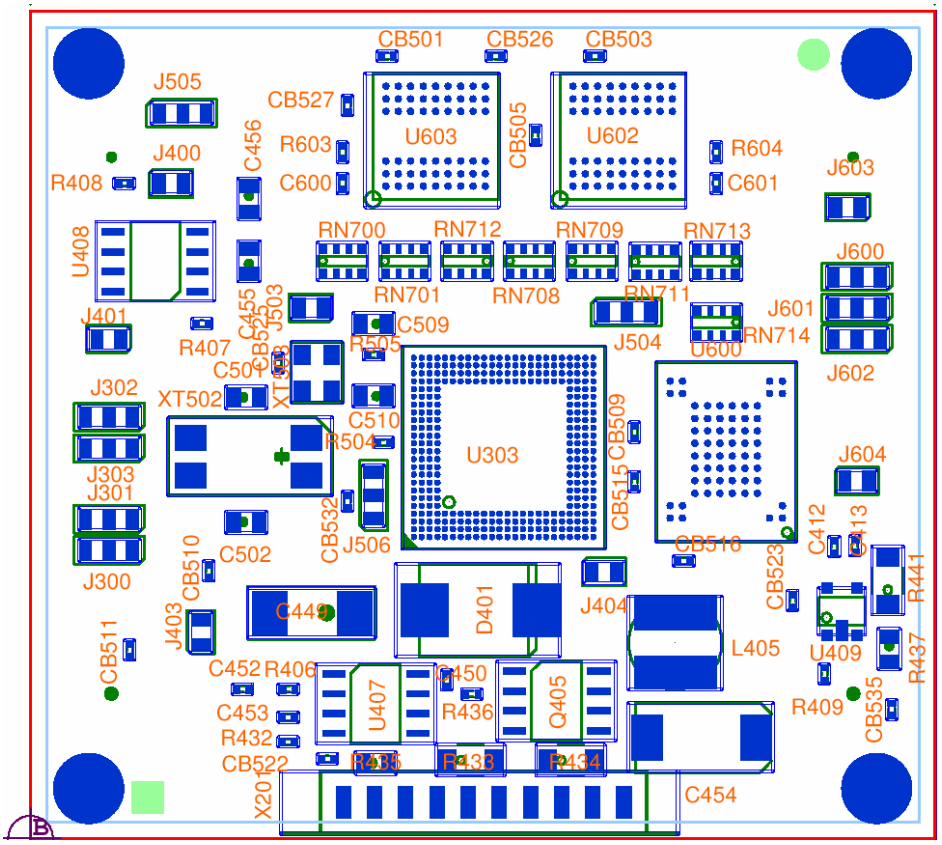

Figure 6: Location of the Jumpers (Top View)
[Generic image, not specific to phyCORE-LPC3180]

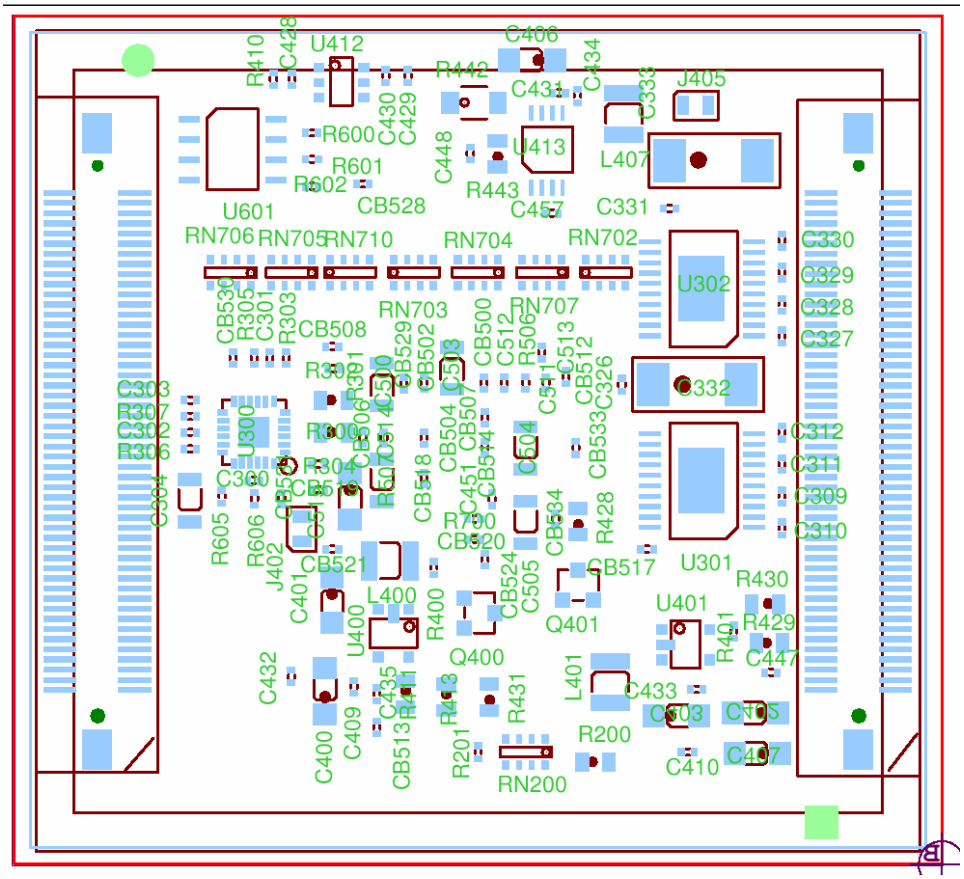

Figure 7: Location of the Jumpers (Bottom View)
[Generic image, not specific to phyCORE-LPC3180]

The jumpers (J = solder jumper) have the following functions:

Table 2: Jumper Settings

	Default Setting		Alternative Setting		See Section
J300	2 + 3	U2_RX of the µC converted to RS-0232 level and routed to X200D22	1 + 2	U2_RX of the µC left at TTL level and routed to X200D22	7.1.1
J301	2 + 3	U2_TX of the µC converted to RS-232 level and routed to X200D23	1 + 2	U2_TX of the µC left at TTL level and routed to X200D23	
J302	2 + 3	U2_HCTS of the µC converted to RS-232 level and routed to X200D46	1 + 2	U2_HCTS of the µC left at TTL level and routed to X200D46	
J303	2 + 3	U2_HRTS of the µC converted to RS-232 level and routed to X200D47	1 + 2	U2_HRTS of the µC left at TTL level and routed to X200D47	
J400	open	Selects processor independent watchdog (U408) extended mode = 6s	closed[1]	Selects processor independent watchdog (U408) normal mode = 12ms	8.1
J401	open[2]	Processor independent watchdog (U408) WDI input at pin X200D8	closed	Processor independent watchdog (U408) WDI input at X200D8 and connected to µC GPO_4	8.2
J402	closed[3]	U400 voltage regulator output connected to VDD_CORE net	open	U400 voltage regulator output disconnected from VDD_CORE net	N/A
J403	closed[3]	U401 voltage regulator output connected to VDD_1V2 net	open	U401 voltage regulator output disconnected from VDD_1V2 net	
J404	closed[3]	U407 voltage regulator output connected to VDD_1V8 net	open	U407 voltage regulator output disconnected from VDD_1V8 net	
J405	closed[3]	U413 voltage regulator output connected to VPD net	open	U413 voltage regulator output disconnected from VPD net	
J503	open	MCKO signal not routed to phyCORE-connector pin	2 + 3	MCKO signals routed to pin X200B1	3.1
J504	2 + 3	A/D supply voltage/positive reference connected to module's VCC supply	1 + 2	A/D supply voltage/positive reference routed to pin X200D50, for external supply	3.2

1 : It is not possible to disable the watchdog function with the jumper in this setting. The watchdog must be set to extended mode for disabling purposes.

2 : Leaving U408 WDI input disconnected will disable the watchdog feature when in extended mode (see J400)

3 : These jumpers are provided as a test access points to determine currents supplied by their respective voltage regulators. Removing any of these jumper will result in failed module operation.

J505	2 + 3	A/D supply GND/negative reference connected to AGND of phyCORE-connector	1 + 2	A/D supply GND/negative reference routed to pin X200C50, for external supply	3.3
J506	1 + 2[1]	µC's RTC supply pins connected to battery control and supply circuitry	2 + 3	µC's RTC supply pins connected to VDD_1V2 supply	4.1.1
J600	2 + 3	EEPROM address bit A0 connected to VCC	1 + 2	EEPROM address bit A0 connected to GND	6.4.1
J601	2 + 3	EEPROM address bit A1 connected to VCC	1 + 2	EEPROM address bit A1 connected to GND	
J602	2 + 3	EEPROM address bit A2 connected to GND	1 + 2	EEPROM address bit A2 connected to VCC	
J603	closed	EEPROM unprotected from write access	open	EEPROM write protected	6.4.2
J604	open	NAND Flash unprotected from write access	closed	NAND Flash write protected	6.3.1

3.1 J503 MCKO Signal

This jumper can be used to connect the master clock output signal (MCKO) to phyCORE-connector pin X200B1 for use in external application circuitry. The output frequency will have a nominal value of 13.000MHz.

The following configurations are possible:

Table 3: J503 MCKO Signal Configuration

SIGNAL CONFIGURATION	J503
MCKO signal not routed to phyCORE-connector	open*
MCKO signals routed to phyCORE-connector pin X200B1	closed

* = Default setting

3.2 J504 A/D Positive Supply/Reference Voltage

Jumper J504 configures the source of the microcontroller's positive supply/reference voltage for the analog to digital converter. The A/D's positive supply input and positive reference input are combined into a single pin on the LPC3180, serving a dual role purpose *(see LPC318x data sheet for further details).* J504 connects this pin to either the phyCORE-module's VCC voltage supply, or pin X200D50 on the phyCORE-connector.

The following configurations are possible:

Table 4: J504, A/D Positive Supply/Reference Voltage Selection

1 : Switchover from VCC to VBAT is automatic in this setting when the battery control and supply circuitry is populated on the module (default, but optional)

SUPPLY/REFERENCE SOURCE	J504
A/D positive supply/reference pin connected to phyCORE-module's VCC supply voltage	2 + 3*
A/D positive supply/reference pin connected to phyCORE-connector pin X200D50	1 + 2

3.3 J505 A/D Negative Supply/Reference Voltage

Jumper J505 configures the source of the microcontroller's negative supply/reference voltage for the analog to digital converter. The A/D's negative supply input and negative reference input are combined into a single pin on the LPC3180, serving a dual role purpose *(see LPC318x data sheet for further details).* J505 connects this pin to either the phyCORE-connector's AGND pins (X20042C, X20047C, X20044D, X20049D), or pin X200C50 on the phyCORE-connector.

The following configurations are possible:

Table 5: J505, A/D Negative Supply/Reference Voltage Selection

SUPPLY/REFERENCE SOURCE	J505
A/D negative supply/reference pin connected to phyCORE-connector's AGND pins	2 + 3*
A/D negative supply/reference pin connected to phyCORE-connector pin X200D50	1 + 2

4 Power Requirements

The phyCORE-LPC3180 operates off a single voltage supply with a nominal value of 3.0V. On-board switching regulators generate the 1.8V, 1.2V, and adjustable 0.9V to 1.2V voltage supplies required by the LPC3180 MCU and on-board components from the 3.0V supplied to the module.

For proper operation the phyCORE-LPC3180 must be supplied with a single voltage source of 3.0V ± 0.1V allowing a current draw of at least ***TBD*** A.

See *Table 1* from *section 2* above for applicable VCC power pins on the phyCORE-connector.

Caution:
Connect all +3.0V VCC input pins to your power supply and at least the matching number of GND pins neighboring the +3.0V pins.

As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry

4.1 Real Time Clock Battery

The connection of a battery is not essential to the functioning of the phyCORE-LPC3180. The battery, interfaced as voltage supply signal VBAT through X200C6 on the phyCORE-connector, provides power to the LPC3180's on-chip Real Time Clock (RTC). This provides a means of time keeping in the absence of power at the VCC pins while drawing minimal power from the battery.

The VBAT input operating limits are listed in Table 6 below.

Table 6: VBAT Operating Limits

	MIN	MAX	UNITS
VBAT	2.65	5.5	V

Caution:
Operation beyond $VBAT_{max}$ could cause damage to the on-board components.

If you choose not to use a battery with the phyCORE-LPC3180 then either (1) jumper J506 should be set to the 2 + 3 position to connect the LPC3180's RTC power pins to the 1.2V supply generated on the module (*see section 4.1.1 for details on setting J506*), or (2) VBAT should be connected to VCC external to the phyCORE-LPC3180.

See section 10 Technical Specifications for battery power consumption.

4.1.1 Real Time Clock Power Source (J506)

Jumper J506 allows selection between two power supplies for the microcontroller's on-chip RTC (Real Time Clock) power supply pins. The two available supplies are VDD_1V2, which is generated from the VCC voltage supplied through the phyCORE-connector, or from the output of the battery control and regulation circuitry[1]. The battery control and regulation circuitry (U412 and U413) provides the power source for the RTC from VCC when VCC is present, and from the VBAT source supplied through the phyCORE-connector pin X200C6 when VCC is lost. In this manner power is never lost to the microcontroller's on-chip Real Time Clock when the battery control and regulation circuitry and battery are present.

The following configurations are possible:

Table 7: J506 Real Time Clock Power Source

POWER SOURCE	J506
Battery control and regulation output	1 + 2*
VDD_1V2	2 + 3[2]

* = Default setting

4.2 Voltage Supervision (U409)

The phyCORE-LPC3180 comes equipped with a triple voltage supervisor IC located at U409. This voltage supervisor is responsible for monitoring the 3.0V supplied to the module through the phyCORE-connector and the 1.8V and 1.2V fixed supplies generated on the module. In the event any of these three supplies dip below permissible thresholds, the supervisor IC will hold the system /RESET line low until the supply voltages have returned to permissible operating levels and continue to hold the /RESET line low for another 200ms[3] afterwards. This ensures a typical reset duration of 200ms once the supply voltages have stabilized.

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[1] : The battery control and regulation circuitry is optional; the standard phyCORE-LPC3180 configuration includes this option.

[2] : The jumper setting 2+3 is the default configuration when the battery control and regulation circuitry are not present on the module.

[3] : Typical reset duration. See LTC1728-1.8 datasheet for specifics.

5 System Configuration

Although most features of the Philips phyCORE-LPC3180 microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

5.1 Starting the phyCORE-LPC3180 ISP Mode

In order to start the ISP command handler on the phyCORE-LPC3180, signal GPI_1/SERVICE_N of the microcontroller must be connected to a low signal level at the time the reset signal changes from its active to the inactive state. This is achieved by applying a low-level signal at pin X200C9 (BOOT) of the phyCORE-LPC3180. An on-board pull-up resistor (R700) ensures a high level at “GPI_1/SERVICE_N” if the BOOT signal is not active. This BOOT signal can be generated by a push button (temporary signal) on the phyCORE-LPC3180 Development Board *(refer to section 12.2.2 for more details)*.

6 System Memory

The phyCORE-LPC3180 provides three types of on-board memory:

- SDR SDRAM: from 16MB to 64MB
- SLC NAND Flash: from 32MB to 128MB
- EEPROM: from 1KB to 32KB

It should be noted that both the SDR SDRAM and the NAND Flash have dedicated memory buses to the LPC3180 microcontroller. The SDRAM and NAND Flash signals are therefore not made available at the phyCORE-connector X200. It is not possible to interface external memory mapped peripheral devices to the LPC3180.

6.1 Memory Model

The LPC3180 memory map is summarized in Table 8 below. For a detailed view of the memory map please consult the *Philip's LPC3180 User's Manual*.

Table 8: LPC3180 Memory Map

ADDRESS	FUNCTION
0x0000 0000 – 0x0FFF FFFF	On-chip memory on AHB matrix slave 3 0x0000 0000 – 0x03FF FFFF IROM or IRAM 0x0400 0000 – 0x07FF FFFF Dummy Space 0x0800 0000 – 0x0BFF FFFF IRAM (64k) 0x0C00 0000 – 0x0FFF FFFF IROM (16k bootstrap)
0x1000 0000 – 0x1FFF FFFF	Reserved
0x2000 0000 – 0x2FFF FFFF	Peripherals on AHB matrix slave 5 0x2000 0000 – 0x2007 FFFF AHB peripherals 0x2008 0000 – 0x2009 FFFF APB peripherals 0x200A 0000 – 0x200B FFFF AHB peripherals
0x3000 0000 – 0x3FFF FFFF	Peripherals on AHB matrix slave 6
0x4000 0000 – 0x4FFF FFFF	Peripherals on AHB matrix salve 7 0x4000 0000 – 0x4007 FFFF FAB peripherals 0x4008 0000 – 0x400F FFFF APB peripherals
0x5000 0000 – 0x7FFF FFFF	Reserved
0x8000 0000 – 0x9FFF FFFF	Off-chip SDRAM (512MB) Accessed as ARM9 instruction fetch, data fetch, and DMA controller access

An operating system or boot loader are typically responsible for initializing the LPC3180 SDRAM and peripherals. If an operating system or boot loader are not present, then it is up to the user to initialize the peripherals of interest before using the module. A basic initialization routine should include the clocking and power scheme, along with the SDRAM controller and SLC NAND Flash controller.

6.2 SDR SDRAM (U602, U603)

The phyCORE-LPC3180 comes preconfigured with 16, 32 or 64MB of 125MHz SDR SDRAM configured for 32-bit access using two 16-bit wide RAM chips at U602 and U603. Although the RAM supplied with the phyCORE-LPC3180 is capable of 125MHz operation, the LPC3180 microcontroller is only capable of a maximum of 104MHz operation to external SDR SDRAM memory.

The LPC3180 is capable of addressing a single RAM bank located at memory address 0x8000 0000 and extending to 0x9FFF FFFF. It should be noted that this is beyond what the phyCORE-LPC3180 supplies for on-board memory. *Refer to Table 9* for permissible SDRAM memory access ranges.

Table 9: Valid SDRAM Memory Address Ranges

SDRAM Size	Lower Memory Address	Upper Memory Address
16MB	0x8000 0000	0x80FF FFFF
32MB	0x8000 0000	0x81FF FFFF
64MB	0x8000 0000	0x83FF FFFF

SDRAM initialization is performed by a boot loader or the operating system following a power-on reset and must not be changed at a later point by any application code.

6.3 NAND Flash Memory (U600)

Use of Flash as non-volatile memory on the phyCORE-LPC3180 provides an easily reprogrammable means of code storage. The following Flash devices can be used on the phyCORE-LPC3180:

Table 10: Compatible NAND Flash Devices

Manufacturer	NAND Flash P/N	Density (MB)
ST Microelectronics	NAND128R3A2CZA6	16
	NAND256R3A2CZA6	32
	NAND512R3A2CZA6	64
	NAND01GR3A2CZA6	128
Samsung	K9F5608R0D-J	32
	K9F1208R0B-J	64
	K9K1G08R0B-J	128
Hynix	HY27SS0851A FPIP	32
	HY27SS08121A FPIP	64

Additionally, any parts that are footprint and functionally compatible with the NAND Flash devices listed above may also be used with the phyCORE-LPC3180.

These Flash devices are programmable with 1.8 V. No dedicated programming voltage is required.

As of the printing of this manual, these NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years.

6.3.1 NAND Flash Write Protection Control (J604)

Jumper J604 is used to control write access to the NAND Flash memory (U600) device. Closing this jumper enables write protection, while opening this jumper allows write access to the device.

The following configurations are possible:

Table 11: J604, EEPROM Write Protection States

WRITE PROTECTION STATE	J604
Write Access Allowed	open*
Write Protected	closed

* = Default setting

6.4 I²C EEPROM (U601)

The phyCORE-LPC3180 is populated with a Microchip 24FC256[1] non-volatile 32KB EEPROM (U601) with an I²C interface to store configuration data or other general purpose data. This device is accessed through I²C port 1 on the LPC3180. The serial clock signal and serial data signal for I²C port 1 are made available at the phyCORE-connector as I2C1_SDA on X200D32 and I2C1_SCL on X200C31.

Three solder jumpers are provided to set the lower address bits: J600, J601, and J602. *Refer to section 6.4.1 for details on setting these jumpers.*

Write protection to the device is accomplished via jumper J603. By default this jumper is closed, allowing write access to the EEPROM memory. Removing this jumper will cause the EEPROM to enter write protect mode, thereby disabling write access to the device. *Refer to section 6.4.2 for further details on setting this jumper.*

6.4.1 Setting the EEPROM Lower Address bits (J600, J601, J602)

The optional 32KB I²C EEPROM populating U601 on the phyCORE-module has the capability of configuring the lower address bits A0, A1, and A2. The four upper address bits of the device are fixed at '1010' (*see Microchip 24FC256 data sheet).* The remaining three lower address bits of the seven bit I²C device address are configurable using jumpers J600, J601 and J602. J600 sets address bit A0, J601 address bit A1, and J602 address bit A2. *Table 12* below shows the resulting seven bit I²C device address for the eight possible jumper configurations.

The following configurations are possible:

Table 12: J600, J601, J602 EEPROM Lower Address Bits

I²C DEVICE ADDRESS	J602	J601	J600
1010 011*	2 + 3*	2 + 3*	2 + 3*
1010 010	2 + 3	2 + 3	1 + 2
1010 001	2 + 3	1 + 2	2 + 3
1010 000	2 + 3	1 + 2	1 + 2

1: See the manufacturer's data sheet for intefacing and operation.

1010 111	1 + 2	2 + 3	2 + 3
1010 110	1 + 2	2 + 3	1 + 2
1010 101	1 + 2	1 + 2	2 + 3
1010 100	1 + 2	1 + 2	1 + 2

* = Default setting

6.4.2 EEPROM Write Protection Control (J603)

Jumper J603 controls write access to the EEPROM (U601) device. Closing this jumper allows write access to the device, while opening this jumper enables write protection.

The following configurations are possible:

Table 13: J603, EEPROM Write Protection States

EEPROM Write Protection State	J603
Write Access Allowed	closed*
Write Protected	open

* = Default setting

7 Serial Interfaces

7.1 RS-232 Transceivers (U301, U302)

Two high-speed RS-232 transceiver supporting 460kbps data rates populate the phyCORE-LPC3180 at U301 and U302. These devices convert the signal levels for:

- U5_RX/U5_TX and U3_RX/U3_TX (UART5 & UART3 on U301)
- U2_RX/U2_TX/U2_HRTS/U2_HRTS (UART2 on U302)

All RS-232 interfaces enable connection of the module to a COM port on a host-PC. In this instance the RxD line of the transceiver is connected to the TxD line of the COM port; while the TxD line is connected to the RxD line of the COM port. The Ground potential of the phyCORE-LPC3180 circuitry needs to be connected to the applicable Ground pin on the COM port as well.

UART3 and UART5 do not support handshake signals. Only Rx/Tx are available on these two UARTs. UART2, however, supports limited handshake signals with HRTS (high-speed Request To Send) and HCTS (high-speed Clear To Send). The phyCORE-LPC3180 does not convert the remaining four available UARTs (UART1, UART4, UART6, UART7) provided by the LPC3180 MCU to RS-232 levels. The TTL level signals are made available at the phyCORE-connector X200 (*see Table 1*). External RS-232 transceivers must be supplied by the user if additional UARTs require RS-232 levels.

It should be noted that although UART 2 is a “High Speed” UART its maximum baud rate (921,600bps) is only twice that of the standard UARTs (460,800) on the LPC3180. The maximum baud rate of UART2 is limited to 460,800 bps when used with the on-board MAX3380 RS-232 transceiver.

7.1.1 UART2 Routing Jumpers J300, J301, J302 and J303

Jumpers J300, J301, J302, J303 are used to route the signals of the high speed synchronous/asynchronous serial interface through the RS-232 transceiver or around the RS-232 transceiver when not populated. When placed in their default positions of 2+3 UART2 signals U2_RX, U2_TX, U2_HRTS, and U2_HCTS are routed through the RS-232 transceiver U302 and come out as U2_RX_RS232, U2_TX_RS232, U2_HRTS_RS232, and U2_HCTS_RS232 at the phyCORE-connector pins X200D22, X200D23, X200D47, U200D46. If U302 does not populate the module, these jumpers should be placed in the 1+2 position to route the TTL level signals to these same pins.

The standard phyCORE-LPC3180 module will have these jumpers placed in the 2+3 positions, thereby routing the RS-232 level signals to the phyCORE-connector. Be sure the phyCORE-LPC3180 configuration you are working with has the jumpers in the correct positions before interfacing these signals outside of the module as incorrect voltage levels will likely cause damage to on-board and off-board components.

The following configurations are possible:

Table 14: J300, J301, J302, J303 High Speed Serial Interface Configuration

SIGNAL CONFIGURATION	J300	J301	J302	J303
U2_RX_RS232, U2_TX_RS232, U2_HRTS_RS232, U2_HCTS_RS232 as RS-232 level signals at X200D22, X200D23, X200D47 and X200D46	2 + 3*	2 + 3*	2 + 3*	2 + 3*

U2_RX_RS232, U2_TX_RS232, U2_HRTS_RS232, U2_HCTS_RS232 as TTL level signals at X200D22, X200D23, X200D47 and X200D46	1 + 2	1 + 2	1 + 2	1 + 2

* = Default setting

7.2 USB Transceiver (U300)

The phyCORE-LPC3180 comes populated with a Philips ISP1301 USB On-The-Go transceiver (U300) supporting full speed, and low speed data rates. The ISP1301 functions as the transceiver between the LPC3180 Host Controller, Device Controller, and On-The-Go Controller. An external USB Standard-A (for USB host), USB Standard-B (for USB device), or USB mini-AB (for USB OTG) connector is all that is needed to interface the phyCORE-LPC3180 USB functionality. The applicable interface signals (D+/D-/VBUS/ID) can be found in the phyCORE-connector pinout *Table 1.*

Termination resistors and capacitors have already been populated on the phyCORE-LPC3180. A Vbus capacitor of 4.7uF has also been placed on the phyCORE-LPC3180. It should be noted that the maximum Vbus capacitance a USB OTG device can add to the bus is 6.5uF. Therefore, adding anything but a small capacitor value of 0.1uF external to the phyCORE-LPC3180 on Vbus is not recommended.

8 Processor Independent Watchdog (U408)

In addition to the LPC3180's on-chip watchdog, the phyCORE-LPC3180 comes equipped with a MAX6301 processor independent watchdog located at U408. This processor independent watchdog is disabled by factory default configuration. To disable the MAX6301 the WDI input must be at high impedance, and the operation mode must be set to extended mode. Both the mode, and the WDI input are controlled via jumpers J400 and J401. *See sections 8.1 and 8.2 for a detailed description of settings these jumpers and the resulting watchdog operation.*

The processor independent watchdog adds a supervisory circuit independent from the LPC3180 processor itself. Under typical operation the watchdog IC has control over the system /RESET signal. If the watchdog is not signaled within a specific timing interval, the watchdog considers there to be an unrecoverable system error and issues a system reset by holding the /RESET signal low for a specific duration of time. To make use of the watchdog feature a general purpose output (GPO) from the controller must provide a high-to-low, or low-to-high transition within the applicable watchdog timeout period to prevent the watchdog timer from issuing a system reset.

8.1 Setting the Watchdog Timeout Period (J400)

Jumper J400 connects the WDS (Watchdog Select) input of the MAX6301 watchdog controller U408 to VCC when the jumper is open, or to GND when the jumper is closed. When the jumper is open the watchdog extended mode is selected with a watchdog timeout period of approximately 6 seconds. When the jumper is closed the watchdog normal mode is selected with a watchdog timeout period of approximately 12 milliseconds. It should be noted that it is not possible to disable the watchdog timer in normal mode. To disable the watchdog timer, extended mode must be selected and the WDI input must be high impedance. The timeout period of the MAX6301 is determined by the external capacitor C456 connected to pin 4. The watchdog timeout period is determined by: $t_{wd} = 2.67 \cdot C_{456} = 2.67 \cdot 4.7nF \cong 12.5ms$ *(see MAX6301 data sheet).*

The following configurations are possible:

Table 15: J400, Processor Independent Watchdog Timeout Period Configuration

SIGNAL CONFIGURATION	J400
Watchdog extended mode selected Watchdog timeout period ~ 6s	open*
Watchdog normal mode selected Watchdog timeout period ~ 12ms	closed

* = Default setting

8.2 Interfacing the WDI Watchdog Input (J401)

Jumper J401 connects the WDI (Watchdog Input) input of the watchdog controller U408 to the MCU's GPO_4 pin when closed, or disconnects the WDI input from the MCU's GPO_4 pin when open. The WDI input is always available at the phyCORE-connector X200D8 regardless of the jumper placement. Leaving the WDI input of the watchdog controller unconnected disables the watchdog functionality when the watchdog is in extended mode (*see section 8.1*). Closing J401 effectively enables the watchdog functionality. Connecting X200D8 to a non high impedance source also enables the watchdog functionality. When enabled the WDI input must change states (high to low, or low to high) before the watchdog timeout period expires (see J400 above) to avoid a processor reset.

The following configurations are possible:

Table 16: J401 First Serial Interface Configuration

SIGNAL CONFIGURATION	J401
Processor independent watchdog U408 WDI input pin disconnected from µC's GPO_4 output pin	open*
Processor independent watchdog U408 WDI input pin connected to µC's GPO_4 output pin	closed

* = Default setting

9 Debug Interface X201

The phyCORE-LPC3180 is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM or for debugging programs currently executing. The JTAG interface also allows access to the Embedded Trace Buffer (ETB) and associated configuration registers. The ETM9 provides a means for tracing the ARM core execution while the ETB provides a means to store this information. The JTAG interface extends out to 2.0 mm pitch pin header rows X201 on the controller side of the module. *Figure 8* and *Figure 9* show the position of the debug interface (JTAG connector X201) on the phyCORE module.

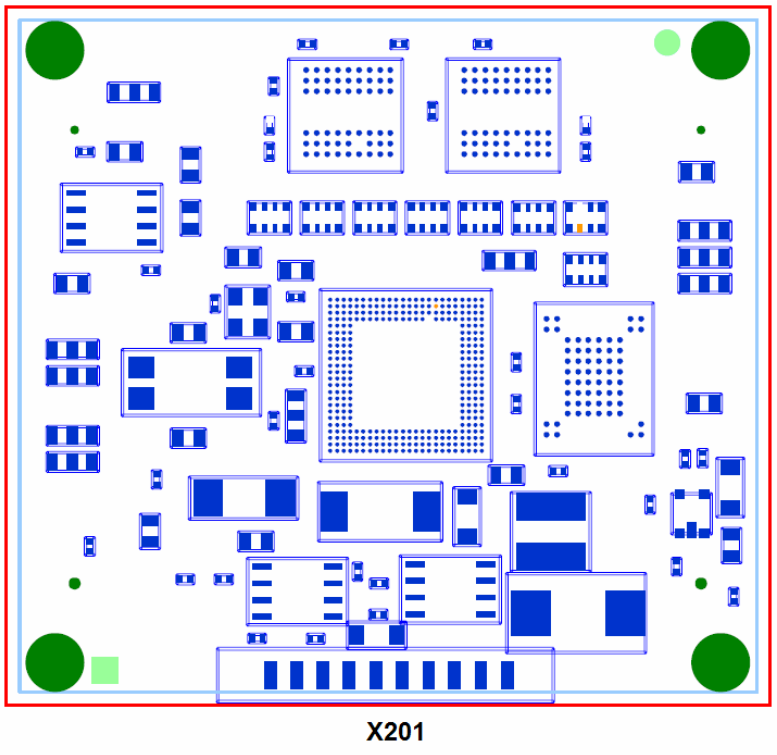

Figure 8: JTAG Interface X201 (Top View)

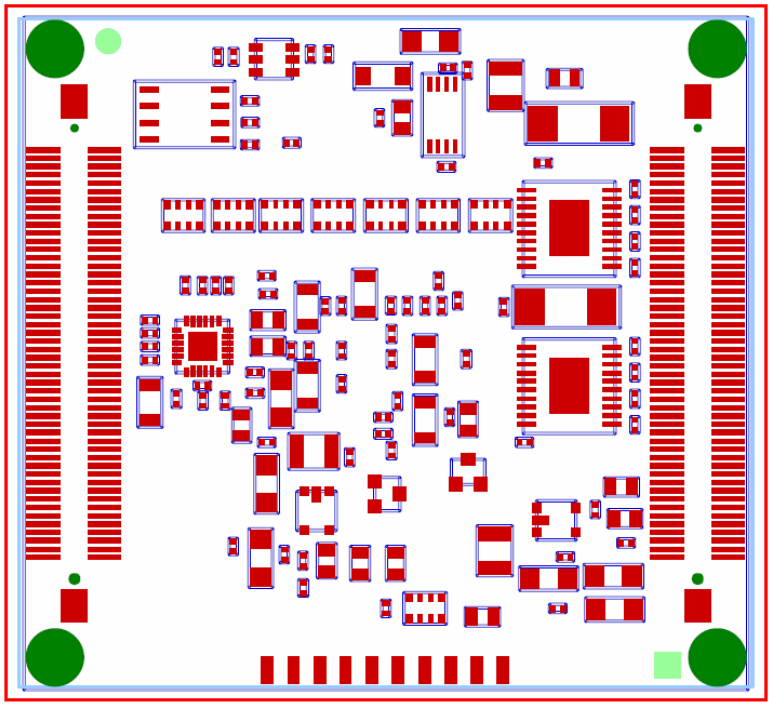

Figure 9: JTAG Interface X201 (Bottom View)

Pin 1 of the JTAG connector X201 is marked by a number one on the connector side of the module. Pin 2 of the JTAG connector is marked by a number two on the controller side of the module.

Note:
The JTAG connector X201 only populates phyCORE-LPC3180 modules with order code PCM-031-D. This version of the phyCORE module is included in all Rapid Development Kits (order code KPCM-031). JTAG connector X201 is not populated on phyCORE modules with order code PCM-031 that are intended for OEM implementation. However, all JTAG signals are also accessible at the phyCORE-connector X200 (Molex connectors). We recommend integration of a standard (2.54 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface. *See Table* 17 *for details on the JTAG signal pin assignment.*

Table 17: JTAG Connector X201 Signal Assignment

SIGNAL	PIN ROW*		SIGNAL
	A	B	
VCC	2	1	VTref
GND	4	3	/TRST
GND	6	5	TDI
GND	8	7	TMS
GND	10	9	TCK
GND	12	11	RTCK
GND	14	13	TDO
GND	16	15	/RESET
GND	18	17	NC
GND	20	19	NC

*Note: Row A is on the controller side of the module and row B is connector side of the module

PHYTEC offers a JTAG-Emulator adapter (order code JA-002) for connecting the phyCORE-LPC3180 to a standard emulator. The JTAG-Emulator adapter extends the signals of the module's JTAG connector to a standard ARM connector with 2.54 mm pin pitch. The JA-002 therefore functions as an adapter for connecting the module's non-ARM-compatible JTAG connector X201 to standard Emulator connectors.

10 Technical Specifications

The physical dimensions of the phyCORE-LPC3180 are represented in *Figure 10*. The module's profile is approximately ***7.2 mm*** thick, with a maximum component height of ***2.6 mm*** on the bottom (connector) side of the PCB and approximately ***3.0 mm*** on the top (microcontroller) side. The board itself is approximately ***1.6 mm*** thick. [Values in ***Bold Italic*** are ***TBD***!]

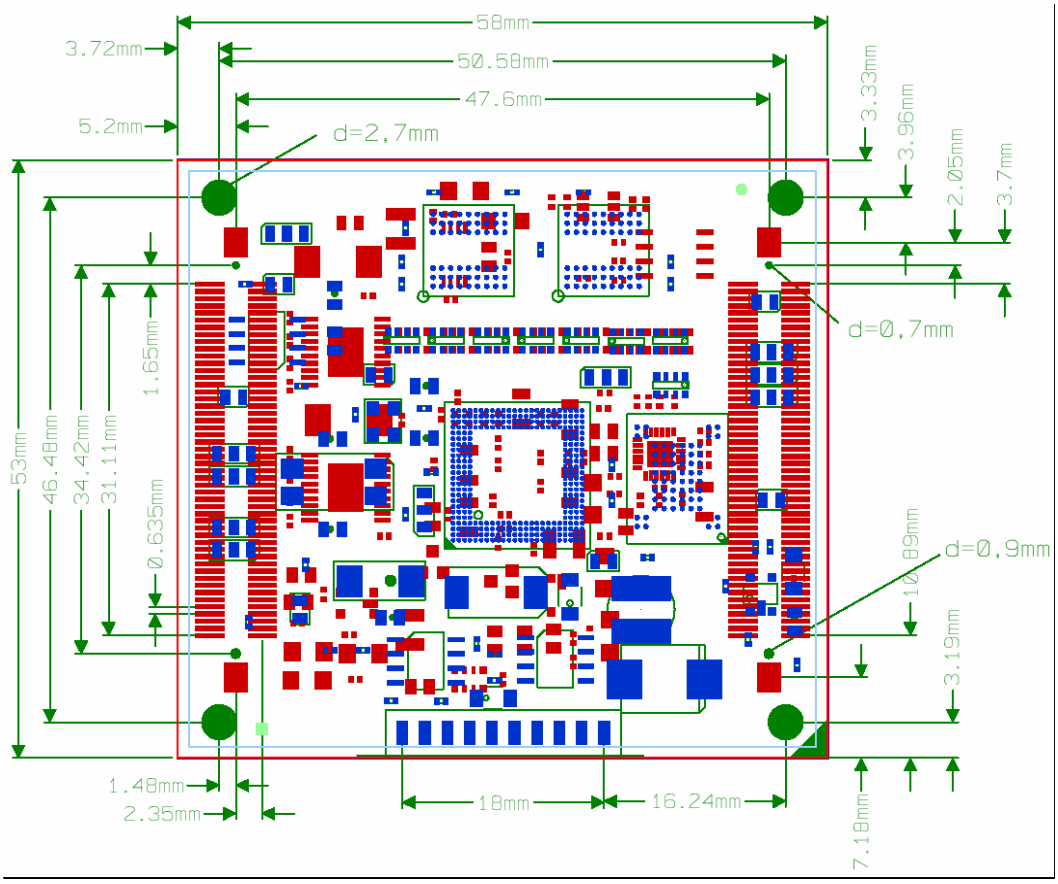

Figure 10: Physical Dimensions

Additional specifications (***all TBD***):

• *Dimensions:*	*60 mm x 53 mm*
• *Weight:*	*approximately 25 g with all optional components mounted on the circuit board*
• *Storage temperature:*	*-40°C to +90°C*
• *Operating temperature:*	*-40°C to +85°C*
• *Humidity:*	*95 % r.F. not condensed*
• *Operating voltage:*	*VCC 2.9V to 3.1V* *VBAT 2.65V to 5.5V*
• *Power consumption:* *VCC 3.0 V/000mA typical*	*Conditions:* ***VCC = 3.0 V, VBAT = 0 V***, *2 MByte fast SRAM, 4 MByte Flash, 10 MHz quartz, 60 Mhz CPU frequency at 20°C*

These specifications describe the standard configuration of the phyCORE-LPC3180 as of the printing of this manual.

11 Hints for Handling the phyCORE-LPC3180

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

12 The phyCORE-LPC3180 on the phyCORE-LPC3180 Development Board

PHYTEC Development Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. Development Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in laboratory environments prior to their use in customer designed applications.

12.1 phyCORE-LPC3180 Development Board Peripherals

The phyCORE-LPC3180 Development Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-LPC3180 Single Board Computer module. The Development Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.
This modular development platform concept is depicted in Figure 11 and includes the following components and peripherals listed in Table 18, Table 19, Table 20, and Table 21. For a more detailed description of each peripheral refer to the appropriate section listed in the applicable table.

Table 18: Development Board Connectors

CONNECTORS		
REF DES	DESCRIPTION	SEE SECTION
X200	phyCORE-connector enabling mounting of the phyCORE-LPC3180	12.2.14
X201	mating receptacle for GPIO expansion board connectivity	
X202	2.54mm pitch 20 pin connector for JTAG debugging interface	9
X203	2.54mm pitch 16 pin connector for LPC3180 keyboard interface	12.2.12
X300	SD Card connector for compatible SD Card devices	12.2.5
X301	USB Standard A connector for USB host operation	12.2.8
X302	USB Standard B connector for USB device operation	
X303	USB MiniAB connector for USB OTG operation	
X304	low-voltage socket for 5.0V power supply connectivity	12.2.1
X305	GND connector (for connection of GND signal of measuring devices such as an oscilliscope)	N/A
X306	3.0V voltage supply for external devices and subassemblies	12.2.11
X307	5.0V voltage supply for external devices and subassemblies	
P300	dual DB-9 sockets for serial RS-232 interface connectivity	12.2.3 12.2.4
BAT300	receptacle for an optional battery to support the LPC3180 on-chip RTC	12.2.10

Table 19: Development Board Buttons

BUTTONS		
REF DES	DESCRIPTION	SEE SECTION
S300	System reset button	12.2.2
S301	System boot button	
S302	User button #1	12.2.6
S303	User button #2	

Table 20: Development Board LEDs

LEDS		
REF DES	DESCRIPTION	SEE SECTION
D307	5V power LED indicator	N/A
D305	User LED #1 (red)	12.2.7
D306	User LED #2 (red)	
D309	User LED #3 (green)	
D310	User LED #4 (green)	

Table 21: Development Board Potentiometers

POTENTIOMETERS		
REF DES	DESCRIPTION	SEE SECTION
R313	A/D optional input	12.2.9

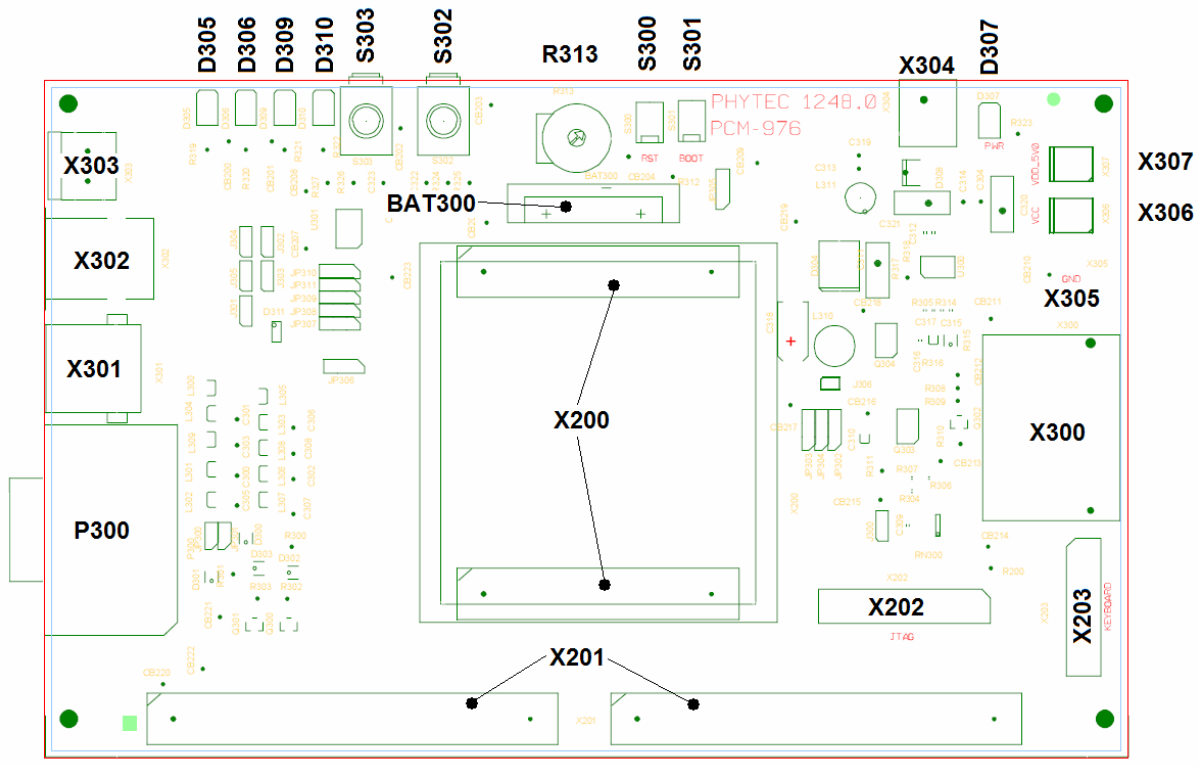

Figure 11: Component Locations on the phyCOR-LPC3180 Development Board

The GPIO expansion port connector X201 provides a 1:1 mapping of the phyCORE-LPC3180 connector X200 signals. Addditional signals generated on the development board are also routed to the GPIO expansion port connector X201. As an accessory a GPIO expansion board is made available through PHYTEC to mates with the X201 connector on the phyCORE-LPC3180 Development Board. This expansion board provides a patch field for easy access to all signals, and additional board space for testing and prototyping. A summary of the signal mappings between X200, X201, and the patch field on the GPIO expansion board is provided in section **Fehler! Verweisquelle konnte nicht gefunden werden.**.

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

12.1.1 Jumpers on the PHYCORE-LPC3180 Development Board

The phyCORE-LPC3180 Development Board comes preconfigured with 7 solder jumpers and 12 solderless jumpers. The jumpers allow the user flexibility of rerouting a limited amount of signals for development constraint purposes. Table 22 below lists the 7 solder jumpers and 12 solderless jumpers, their default positions, and their functions in each position. Figure 12 depicts the jumper pad numbering scheme for reference when altering jumper settings on the development board.

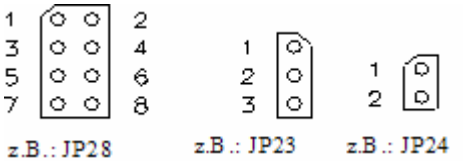

Figure 12: Typical Jumper Pad Numbering Scheme (solderless jumpers)

The jumpers (J = solder jumper, JP = solderless jumper) have the following functions:

Table 22: phyCORE-LPC3180 Development Board Jumper Settings

	Default Setting		Alternative Setting		See Section
J300	2 + 3	VMMC signal routed to SD Card connector as power input	1 + 2	VCC signal routed to SD card connector as power input	12.2.5
J301	2 + 3	USB_VBUS signal routed to X303 (USB OTG connector)	1 + 2	USB_VBUS signal routed to X301 (USB Host connector)	12.2.8
J302	2 + 3	USB_D- signal routed to J304	1 + 2	USB_D- signal route to X301 (USB Host connector)	
J303	2 + 3	USB_D+ signal routed to J304	1 + 2	USB_D+ signal route to X301 (USB Host connector)	
J304	2 + 3[1]	USB_D- signal routed to X303 (USB OTG connector)	1 + 2	USB_D- signal route to X302 (USB Device connector)	
J305	2 + 3[2]	USB_D+ signal routed to X303 (USB OTG connector)	1 + 2	USB_D+ signal route to X302 (USB Device connector)	
J306	closed[3]	U300 voltage regulator output connected to VCC net	open	U300 voltage regulator output disconnected from VCC net	N/A
JP300	open	Allow P300A-7 signal to initiate a reset via /RESIN signal	closed	Disallow P300A-7 signal to initiate a reset via /RESIN signal	12.2.3

1: When J302 is in the 1+2 position then J304 is a don't care. J304 is only important when the USB_D- signal has first been routed to it by setting J302 to the 2+3 position (default).

2: When J303 is in the 1+2 position then J305 is a don't care. J305 is only important when the USB_D+ signal has first been routed to it by setting J303 to the 2+3 position (default).

3: This jumper is provided as a test access points to determine the current supplied by the 3.0V voltage regulator U300. Removing this jumper will result in failed module operation.

JP301	open	Allow P300A-4 signal to control boot mode via GPI_1//SERVICE signal of the µC	closed	Disallow P300A-4 signal to control boot mode via GPI_1//SERVICE signal of the µC	
JP302	1 + 2	xMMC_DETECT signal routed to GPI_0 of the µC	2 + 3	xMMC_DETECT signal routed to pin X201B38 of the GPIO expansion board connector	12.2.5
JP303	1 + 2	xMMC_WP signal routed to GPI_2 of the µC	2 + 3	xMMC_WP signal routed to pin X201A41 of the GPIO expansion board connector	
JP304	1 + 2[1]	GPO_1 of the µC routed to MMC power control circuitry	2 + 3	MMC_PWR signal routed to MMC power control circuitry and available at pin X201B40 GPIO of the expansion board connector	
JP305	1 + 2	ADIN0 of the µC routed to wiper of R313 1k potentiometer	2 + 3	R313 1k potentiometer wiper routed to pin X201C46 of the GPIO expansion board connector	12.2.9
JP306	2 + 3	LED1 (D305) routed to GPO_2 of the µC	1 + 2	LED1 (D305) routed to pin X201B41 of the GPIO expansion board connector	12.2.7
JP307	2 + 3	LED2 (D306) routed to GPO_3 of the µC	1 + 2	LED2 (D306) routed to pin X201B42 of the GPIO expansion board connector	
JP308	2 + 3	LED3 (D309) routed to GPO_5 of the µC	1 + 2	LED3 (D309) routed to pin X201A43 of the GPIO expansion board connector	
JP309	2 + 3	LED4 (D310) routed to GPO_6 of the µC	1 + 2	LED4 (D310) routed to pin X201B43 of the GPIO expansion board connector	
JP310	2 + 3	BUTTON1 output routed to GPI_3 of the µC	1 + 2	BUTTON1 output routed to pin X201A44 of the GPIO expansion board connector	12.2.6
JP311	2 + 3	BUTTON2 output routed to GPI_5 of the µC	1 + 2	BUTTON2 output routed to pin X201B45 of the GPIO expansion board connector	12.2.6

1 : If J300 is not in its default position of 2 + 3 then JP304's position becomes a don't care.

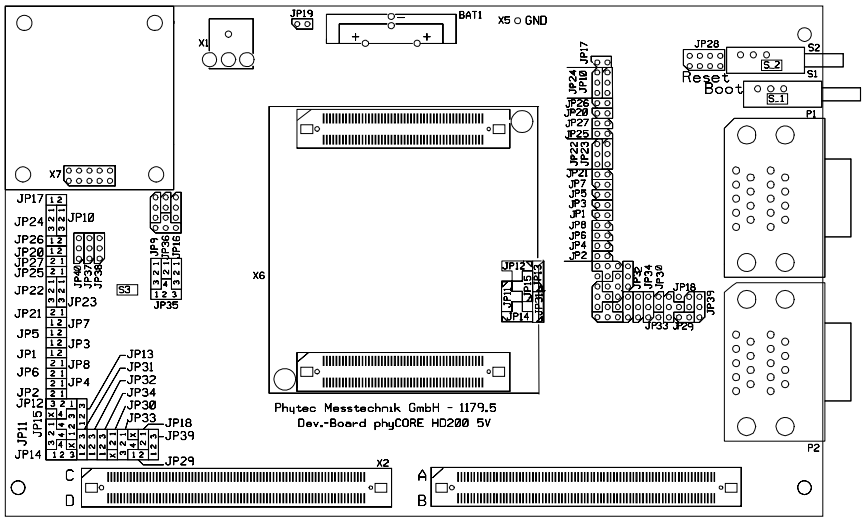

Figure 13: Location of the Jumpers (View of the Component Side)

Figure 14 shows the factory default jumper settings for operation of the phyCORE-LPC3180 Development Board with the standard phyCORE-LPC3180. Jumper settings for other functional configurations of the phyCORE-LPC3180 module mounted on the Development Board are described in detail in *section 12.2*.

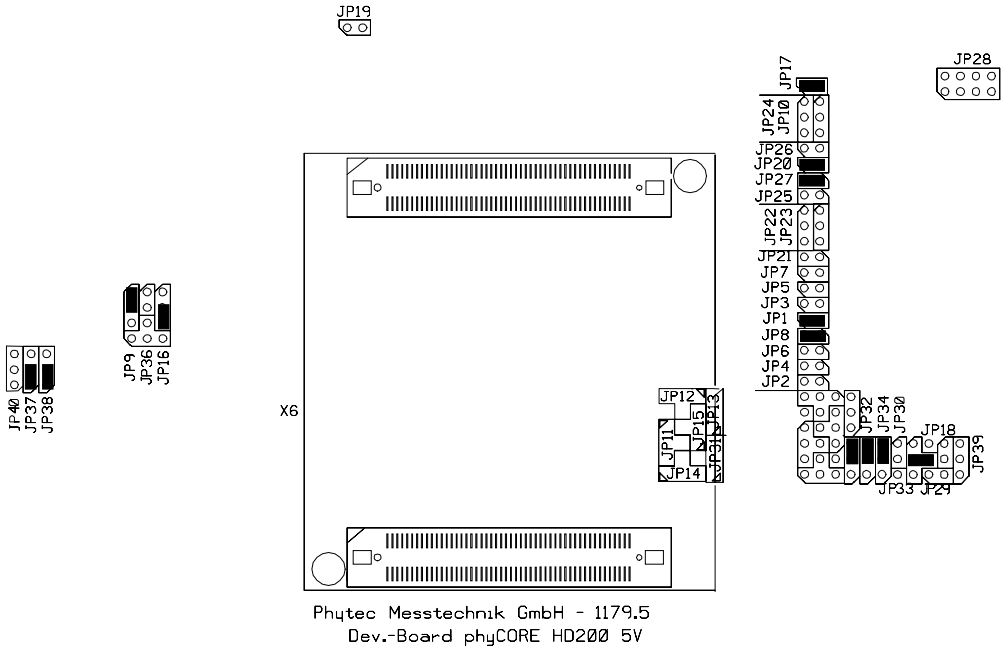

Figure 14: Default Jumper Settings of the phyCORE-LPC3180 Development Board with the phyCORE-LPC3180

12.2 Functional Components on the phyCORE-LPC3180 Development Board

This section describes the functional components of the phyCORE-LPC3180 Development Board supported by the phyCORE-LPC3180 and appropriate jumper settings to activate these components. Depending on the specific configuration of the phyCORE-LPC3180 module, alternative jumper settings can be used. These jumper settings are different from the factory default settings as shown in *Figure 14* and enable alternative or additional functions on the phyCORE Development Board HD200 depending on user needs.

12.2.1 Power Supply at X304

Caution:
Do not use a laboratory adapter to supply power to the Development Board! Power spikes during power-on could destroy the phyCORE module mounted on the Development Board! Do not change modules or jumper settings while the Development Board is supplied with power!

Permissible input voltage: +5 VDC regulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCORE-LPC3180 mounted on the Development Board as well as whether an optional expansion board is connected to the Development Board. An adapter with a minimum supply of 500 mA is recommended.

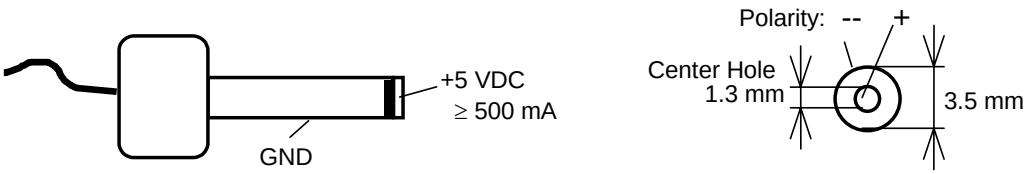

Figure 15: Connecting the Supply Voltage at X304

12.2.2 Starting the LPC3180 Bootstrap Software

The Philips LPC3180 microcontroller contain on-chip bootstrap software that provides an In-System Programming (ISP) interface to on-chip IRAM and also handles booting from external NAND flash. The bootstrap software allows a secondary bootloader to be downloaded into IRAM for NAND flash programming.

The combination of this ISP handler and the corresponding LPC3180 Flash Utility software installed on the PC allows for on-chip Flash programming with application code via an RS-232 interface.

In order to start the bootstrap software to download external user code into on-chip IRAM the GPI_1//SERVICE pin of the microcontroller must be at a low signal level at the time the /RESET signal changes from its active to inactive state. This is achieved by holding down the BOOT switch (S301), pressing the RST switch (S300), releasing the RST switch, and then releasing the BOOT switch. This will cause a system reset and the value of the GPI_1//SERVICE (boot) pin to be latched at a low signal level. The on-chip bootstrap software will then wait for user code via UART5. When the BOOT switch is not used a pull-up resistor on the GPI_1//SERVICE pin ensures a high value at the time of boot to start booting from external NAND flash. *Refer to the Philips LPC3180 User Manual section 26 “BOOT PROCESS” for an indepth explanation of the booting procedure and bootstrap software.*

12.2.3 Accessing UART5 through Socket P300A

UART5 of the LPC3180 is accessed via socket P300A. Socket P300A is the lower socket of the double DB-9 connector at P300. P300A provides connections to the following UART5 interfaces:

- UART5 RX at RS232 compatible levels on pin 3
- UART5 TX at RS232 compatible levels on pin 2
- RESET control on pin 7 via jumper JP300
- BOOT control on pin 4 via jumper JP301

See section 7.1 RS-232 Transceivers (U301, U302) for applicable UART datarates.

The RESET and BOOT inputs at pins 7 and 4 respectively provide a means of reseting and rebooting the LPC3180 over the UART5 interface. Unlike their switch (S300, S301) activated counterparts discussed in section 12.2.2, the RESET and BOOT signals through P300A are active high. The recommended operating limits are:

Table 23: P300A BOOT/RESET Signal Operating Limits

	MIN	MAX	UNITS
Vih	2.5	15	V
Vil	-15	1.0	V

Both inputs perform the identical functions as their switched counterparts in section 12.2.2. Jumpers JP300 and JP301 control connection of P300A pin 7 and pin 4 to the control and boot circuitry. By factory default these jumpers are unplaced. To use these signals JP300 and JP301 must be placed.

12.2.4 Accessing UART2 through Socket P300B

UART2 of the LPC3180 is accessed via socket P300B. Socket P300B is the upper socket of the double DB-9 connector at P300. P300B provides connections to the following UART2 interfaces:

- UART2 RX at RS232 compatible levels on pin 3
- UART2 TX at RS232 compatible levels on pin 2
- UART2 HRTS at RS232 compatible levels on pin 8
- UART2 HCTS at RS232 compatible levels on pin 7

See section 7.1 RS-232 Transceivers (U301, U302) for applicable UART datarates.

12.2.5 SD Card Interface at Connector X300

Connector X300 provides an interface for a compatible SD card. The phyCORE-LPC3180 Development Board supplies additional card detection and power control circuitry to the SD card interface.

Four configuration jumpers are supplied for card detection, write protect detection, SD card power source, and SD card power control. The four jumpers have the following functions:

J300 Controls the SD card power source. By factory default this jumpers is set to the 2 + 3 position which connects the controllable SD card power source VMMC to the SD card power input connector pins. Alternately this jumper can be set to the 1 + 2 position and provide power to the SD card as long as the development board has power via X304.

JP302 Controls the routing of the MMC_DETECT signal. By factory default this jumper is set to the 1 + 2 position which connects this signal to GPI_0 of the LPC3180. Alternatively this jumper can be set to the 2 + 3 position which routes the MMC_DETECT signal to the GPIO expansion port connector X201B38. The MMC_DETECT signal can be used for detection of the SD card by application software.

JP303 Controls routing of the MMC_WP signal. By factory default this jumper is set to the 1 + 2 position which connects this signal to GPI_2 of the LPC3180. Alternatively this jumper can be set to the 2 + 3 position which routes the MMC_WP signal to the GPIO expansion port connector X201A41. The MMC_WP signal can be used for write protect detection of the SD card by application software.

JP304 Controls routing of the MMC_PWR signal. By factory default this jumper is set to the 1 + 2 position which connects this signal to the GPO_1 of the LPC3180. Alternatively this jumper can be set to the 2 + 3 position which routes the MMC_PWR signal to the GPIO expansion port connector X201B40. The MMC_PWR signal can be used to control the VMMC power source by application software.

Jumpers J300 and JP304 combined provide a means for controlling power to the SD Card interface. When jumper J300 (see above) is set in its factory default position of 2 + 3 the MMC_PWR signal has control over VMMC. By default MMC_PWR is connected the GPO_1 of the LPC3180. An active HIGH at this general purpose output will turn on 3.0V power to the VMMC power source and an active LOW will turn off 3.0V power to the VMMC power source. Presumably the MMC_DETECT signal would be used in conjunction with the MMC_PWR signal. Typically the user application would detect the presense of the card by reading the GPI_0 input connected to the MMC_DETECT signal and then turn power on to the SD card by providing an active HIGH at GPO_1 output.

12.2.6 User Buttons S301 and S302

User buttons S301 and S302 are provided on the phyCORE-LPC3180 development board as general purpose buttons for testing purposes. Two jumpers provide routing control over button output. The two jumpers have the following functions:

JP310 Controls routing S301 debounced button output. By factory default this jumper is placed in the 2 + 3 position which routes the debounced output of S301 to GPI_3 of the LPC3180. Alternatively, this jumper can be set to the 1 + 2 position which routes the debounced output to GPIO expansion port connector X201A44 as signal BUTTON1. The inverse signal /BUTTON1 is always available at X201A45 regarldess of JP310 settings.

JP311 Controls routing S302 debounced button output. By factory default this jumper is placed in the 2 + 3 position which routes the debounced output of S302 to GPI_5 of the LPC3180. Alternatively, this jumper can be set to the 1 + 2 position which routes the debounced output to GPIO expansion port connector X201B45 as signal BUTTON2. The inverse signal /BUTTON2 is always available at X201A46 regarldess of JP311 settings.

12.2.7 User LEDs D305, D306, D309, and D310

User LEDs D305, D306, D309, and D310 are provided on the phyCORE-LPC3180 development board as general purpose LEDs for testing purposes. Four jumpers provide routing control over LED control source. The four jumpers have the following functions:

JP306 Controls routing D305 control source. By factory default this jumper is placed in the 2 + 3 position which routes GPO_2 of the LPC3180 as the control source. Alternatively, this jumper can be set to the 1 + 2 position which routes the control source to GPIO expansion port connector X201B41 as signal LED1_C. A LOW signal illuminates the LED while a HIGH signal extinguishes the LED.

JP307 Controls routing D306 control source. By factory default this jumper is placed in the 2 + 3 position which routes GPO_3 of the LPC3180 as the control source. Alternatively, this jumper can be set to the 1 + 2 position which routes the control source to GPIO expansion port connector X201B42 as signal LED2_C. A LOW signal illuminates the LED while a HIGH signal extinguishes the LED.

JP308 Controls routing D309 control source. By factory default this jumper is placed in the 2 + 3 position which routes GPO_5 of the LPC3180 as the control source. Alternatively, this jumper can be set to the 1 + 2 position which routes the control source to GPIO expansion port connector X201A43 as signal LED3_C. A LOW signal illuminates the LED while a HIGH signal extinguishes the LED.

JP309 Controls routing D310 control source. By factory default this jumper is placed in the 2 + 3 position which routes GPO_6 of the LPC3180 as the control source. Alternatively, this jumper can be set to the 1 + 2 position which routes the control source to GPIO expansion port connector X201B43 as signal LED4_C. A LOW signal illuminates the LED while a HIGH signal extinguishes the LED.

12.2.8 Accessing the USB through Connectors X301, X302, and X303

The phyCORE-LPC3180 Development Board provides three USB receptacles for USB operation: a USB standard A receptacle for Embedded USB Host connectivity (X301), a USB standard B receptacle for USB device connectivity (X302), and a USB miniAB receptacle for USB On-The-Go connectivity (X303). Note that only one of these may be used at any time. Five solder jumpers are provided for USB signal routing control to one of the three USB connectors. The five jumpers have the following functions:

J301 Controls routing of the USB_VBUS signal. By factory default this jumper is placed in the 2 + 3 position which routes the USB_VBUS signal to the VBUS pin of the USB miniAB receptacle. Alternatively, this jumper can be set to the 1 + 2 position which routes the USB_VBUS signal to the VBUS pin of the USB standard A receptacle. Note that there is no option to route the USB_VBUS signal to the USB standard B connector. When used as a device, the phyCORE-LPC3180 derives its power from the power provided through the power supply connector X304.

J302 Controls routing the USB_D- signal. By factory default this jumper is placed in the 2 + 3 position which routes the USB_D- signal to jumper J304. Alternatively, this jumper can be set to the 1 + 2 position which routes the USB_D- signal to the D- pin of the USB standard A receptacle.

J303 Controls routing the USB_D+ signal. By factory default this jumper is placed in the 2 + 3 position which routes the USB_D+ signal to jumper J305. Alternatively, this jumper can be set to the 1 + 2 position which routes the USB_D+ signal to the D+ pin of the USB standard A receptacle.

J304 Controls routing the USB_D- signal in conjunction with J302. By factory default this jumper is placed in the 2 + 3 position which routes the USB_D- signal originating from J302 to the D- pin of the USB miniAB connector. Alternatively, this jumper can be set to the 1 + 2 position which routes the USB_D- signal originating from J302 to the D- pin of the USB standard B receptacle.

J305 Controls routing the USB_D+ signal in conjunction with J303. By factory default this jumper is placed in the 2 + 3 position which routes the USB_D+ signal originating from J303 to the D+ pin of the USB miniAB connector. Alternatively, this jumper can be set to the 1 + 2 position which routes the USB_D+ signal originating from J303 to the D+ pin of the USB standard B receptacle.

To better understand the routing of the USB signals through the solder jumpers, Figure 16 is provided below. The signals to the left of the jumpers in Figure 16 are routed to the phyCORE-LPC3180 (and in turn are connected to the Philips ISP1301 OTG transceiver), while the signals on the right are routed to their respective USB connectors. By factory default the USB jumpers are configured for a USB OTG connectivity using the USB miniAB receptacle X303.

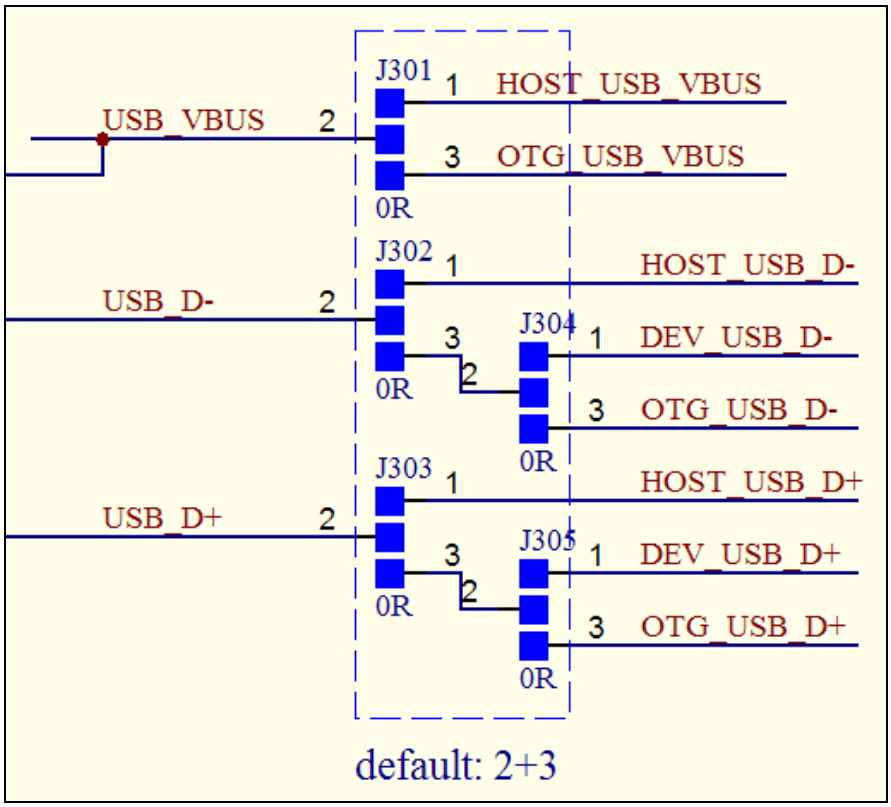

Figure 16: USB Signal Routing Solder Jumpers

To configure the phyCORE-LPC3180 Development Board for connectivity other than the factory default of USB OTG, please refer to Table 24 below.

Table 24: USB Jumper Configurations for Host/Device/OTG Operation

CONFIGURATION	J301	J302	J303	J304	J305	APPLICABLE CONNECTOR
USB Host	1+2	1+2	1+2	X	X	X301 – Standard A
USB Device	X	2+3	2+3	1+2	1+2	X302 – Standard B
USB OTG*	2+3	2+3	2+3	2+3	2+3	X303 – miniAB

* = Default setting

12.2.9 A/D Potentiometer R313

To provide a means of testing the A/D inputs of the LPC3180, the phyCORE-LPC3180 Development Board provides a 1k potentiometer as a voltage divider for the VCC = 3.0V module supply voltage. A single jumper JP305 controls routing the output of the wiper on the 1k potentiometer R313. The routing options are:

Table 25: A/D Potentiometer Output Routing Options

R313 WIPER ROUTING	JP305
Routed to LPC3180 A/D input pin ADIN0	1 + 2*
Routed to GPIO expansion port connector X201C46 as signal ADC_VADJ	2 + 3

* = Default setting

It should be noted that solder jumpers J504 and J505 on the phyCORE-LPC3180 module control the A/D's positive and negative supply reference. By default these jumpers are set to VCC (3.0V) as the positive A/D supply reference and AGND as the negative A/D supply reference. Further, the AGND is floating with respect to the development board and module GND. It is up to the user to supply a connection external to the development board by accessing the AGND pins available at the GPIO expansion port connector X201D44, D49, C42, and C47. *Refer to the Philips LPC3180 electrical data sheet for permissible voltage levels on the VSS_ad pin.*

12.2.10 Battery Connector BAT300

The mounting space BAT300 (*see PCB stencil*) is provided for connection of a battery that buffers the RTC on the phyCORE-LPC3180. In the event of a VCC operating voltage failure the RTC is automatically supplied with power from the connected battery. The optional battery required for the RTC buffering (*refer to section 4.1)* is available through PHYTEC (order code BL-011).

12.2.11 Power Connectors X306 and X307

Connector X306 and X307 provide convenient connection points for access to the module's 5.0V supply voltage and 3.0V supply voltage. The GND pin of X306 and X307 is marked on the PCB with a dot next to the applicable pin. The maximum current draw from these connectors is dependent upon the loading conditions during module operation. The 5.0V wall adapter supplied with the phyCORE-LPC3180 Development Board is rated for a maximum of 1.5A of continous current. Further more, the DC-DC regulator providing the 3.0V supply from the 5.0V wall adapter output is designed to support 2.1A of continous current. This regulator not only supplies the 3.0V required by the development board, but also the 3.0V required by the phyCORE-LPC3180 module. It is recommended not to exceed XmA of continous current from the 5.0V supply at X306 and YmA of current from the 3.0V supply at X307.

12.2.12 Keyboard Connector at X203

Connector X203 provides a convenient connection interface to the keyboard scan function of the LPC3180 microcontroller. Pin 1 on the development board is marked with a clipped corner as depicted in Figure 17 below.

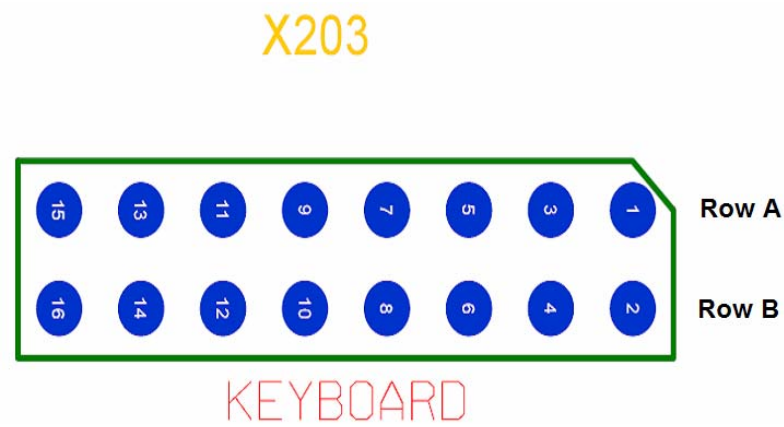

Figure 17: Development Board Keyboard Connector X203

Table 26 below describes the signal assignment scheme at connector X203. *Please refer to the Philip's LPC3180 User's Manual for a detailed explanation of interfacing the keyboard port.*

Table 26: Keyboard Connector X203 Signal Assignment

Signal	Pin Row		Signal
	A	B	
KEY_COL0	1	2	KEY_COL1
KEY_COL2	3	4	KEY_COL3
KEY_COL4	5	6	KEY_COL5
GPI_8/COL6/BUSY	7	8	GPI_9/KEY_COL7
KEY_ROW0	9	10	KEY_ROW1
KEY_ROW2	11	12	KEY_ROW3
KEY_ROW4	13	14	KEY_ROW5
GPIO_2/KEY_ROW6	15	16	GPIO_3/KEY_ROW7

12.2.13 Debug Interface X202

In addition to the JTAG debug connector available on the phyCORE-LPC3180, the phyCORE-LPC3180 Development Board also extends these signals to a 20 pin, 2.54mm pitch industry standard connection interface at X202. Pin 1 on the development board is marked with a clipped corner as depicted in Figure 18 below. *Please refer to section 9 for details on the debug interface.*

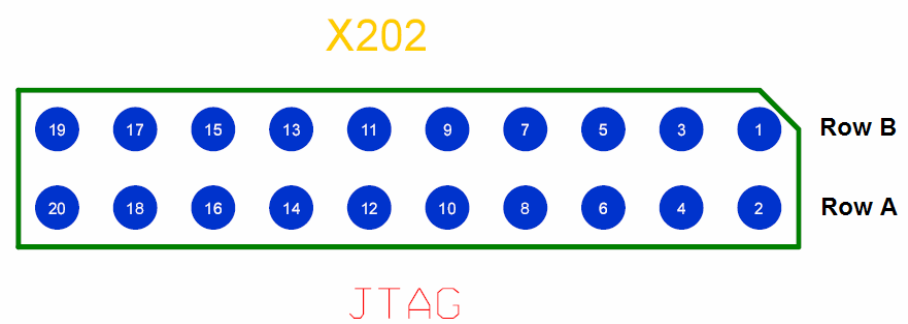

Figure 18: Development Board JTAG Connector X202

Table 27 below describes the signal assignment scheme at connector X202.

Table 27: JTAG Connector X202 Signal Assignment

SIGNAL	PIN ROW		SIGNAL
	A	B	
VCC	2	1	VTref
GND	4	3	/TRST
GND	6	5	TDI
GND	8	7	TMS
GND	10	9	TCK
GND	12	11	RTCK
GND	14	13	TDO
GND	16	15	/RESET
GND	18	17	NC
GND	20	19	NC

12.2.14 Pin Assignment Summary of the PHYCORE, the Expansion Bus and the Patch Field

As described in *sec*tion 12.1 all signals from the phyCORE-LPC3180 extend in a strict 1:1 assignment to the Expansion Bus connector X201 on the Development Board. These signals, in turn, are routed in a similar manner to the patch field on an optional GPIO expansion board that mounts to the Development Board at X201. This patch field provides easy access to all phyCORE-LPC3180 signals, in addition to signals generated on the Development Board.

Please note that, depending on the design and size of the expansion board, only a portion of the entire patch field is utilized under certain circumstances. When this is the case, certain signals described in the following section will not be available on the expansion board. However, the pin assignment scheme remains consistent.

A two dimensional numbering matrix similar to the one used for the pin layout of the phyCORE-connector is provided to identify signals on the Expansion Bus connector (X201 on the Development Board) as well as the patch field.

However, the numbering scheme for Expansion Bus connector and patch field matrices differs from that of the phyCORE-connector, as shown in the following two figures:

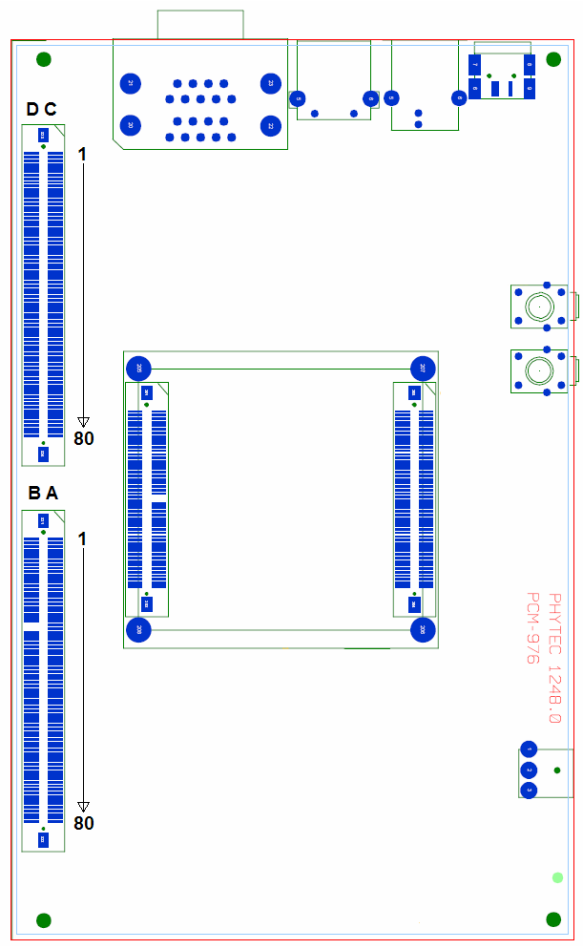

Figure 19: Pin Assignment Scheme of the Expansion Bus X201

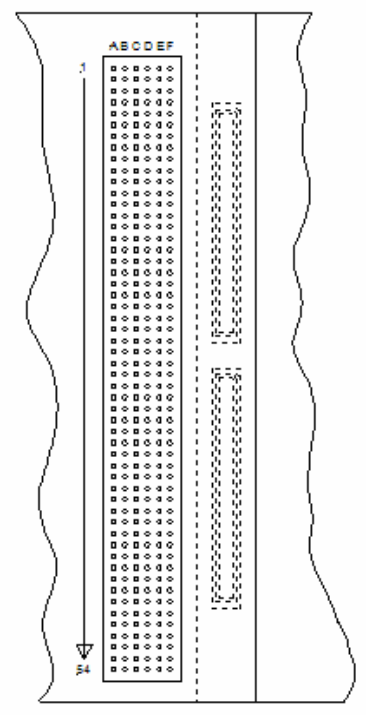

Figure 20: Pin Assignment Scheme of the Patch Field on the Optional GPIO Expansion Board

The pin assignment on the phyCORE-LPC3180, in conjunction with the Expansion Bus (X201) on the Development Board and the patch field on the optional GPIO expansion board is detailed in the tables to follow. Please note that the tables are arranged in functional groupings. Because there are a number of multiplex pins on the Philip's LPC3180 microcontroller, a particular pin may fall in multiple groups, and hence will be repeated in several tables.

Table 28: GPI Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

GPI			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
GPI_0	12B	12B	31F
GPI_1//SERVICE	9C	9C	3B
GPI_2	13B	13B	32C
GPI_3	13A	13A	32A
GPI_4/SPI1_BUSY	18A	18A	33B
GPI_5	14A	14A	32E
GPI_6/HSTIM_CAPTURE	15A	15A	32B
GPI_7	15B	15B	32F
GPI_8/KEY_COL6/SPI2_BUSY	6A	6A	29D
GPI_9/KEY_COL7	6B	6B	29F
GPI_10/U4_RX	29C	29C	10C
GPI_11	16A	16A	33A

Table 29: GPO Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

GPO			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
GPO_0/TST_CLK1	14C	14C	5C
GPO_1	15C	15C	5E
GPO_2	15D	15D	5B
GPO_3	16C	16C	5F
GPO_4	18D	18D	6B
GPO_5	18C	18C	6E
GPO_6	20D	20D	7E
GPO_7	21D	21D	7D
GPO_8	38C	38C	13A
GPO_9	38D	38D	12E
GPO_10	39C	39C	13B
GPO_11	40C	40C	13D
GPO_12	40D	40D	13F
GPO_13	41C	41C	14A

GPO_14	41D	41D	14E
GPO_15	42D	42D	14B
GPO_16	43C	43C	14F
GPO_17	43D	43D	15A
GPO_18	44C	44C	15C
GPO_19	45C	45C	15E
GPO_20	45D	45D	15B
GPO_21/U4_TX	30C	30C	10E
GPO_22/U7_HRTS	34C	34C	11F
GPO_23/U2_HRTS	25D	25D	8F

Table 30: GPIO Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

GPIO			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
GPIO_0	11D	11D	4A
GPIO_1	12D	12D	4B
GPIO_2/KEY_ROW6	11A	11A	31E
GPIO_3/KEY_ROW7	11B	11B	31B
GPIO_4	13C	13C	4F
GPIO_5	13D	13D	5A

Table 31: SPI Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

SPI			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
SPI1_CLK	16B	16B	33C
SPI1_DATIN	17B	17B	33E
SPI1_DATIO	18B	18B	33F
SPI2_CLK	20A	20A	34E
SPI2_DATIN	19A	19A	34A
SPI2_DATIO	20B	20B	34B

Table 32: SD Card Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

SD CARD

SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
MS_CLK	21A	21A	34D
MS_BS	21B	21B	34F
MS_DIO0	22B	22B	35A
MS_DIO1	23B	23B	35B
MS_DIO2	23A	23A	35E
MS_DIO3	24A	24A	35D

Table 33: USB Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

USB			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
USB_VBUS	25A	25A	35F
USB_ID	26A	26A	36E
USB_D-	25B	25B	36A
USB_D+	26B	26B	36B
USB_SE0_VM/U5_TX	27B	27B	36F
/USB_ATX_INT	28B	28B	37C
USB_I2C_SCL	30B	30B	37F
USB_I2C_SDA	30A	30A	37B
USB_DAT_VP/U5_RX	28A	28A	37A
/USB_OE_TP	29A	29A	37E

Table 34: JTAG/DEBUG Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

JTAG/DEBUG			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
RTCK	35B	35B	39B
TMS	36B	36B	39F
/TRST	37B	37B	40A
TDO	34A	34A	39A
TCK	35A	35A	39E
TDI	36A	36A	39D

Table 35: System Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

SYSTEM			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD

CLKIN	1A	1A	28A
MCKO	1B	1B	28C
GPI_1//SERVICE	9C	9C	3B
GPO_0/TST_CLK1	14C	14C	5C
TST_CLK2	31A	31A	38A
HIGHCORE	33A	33A	38B
ONSW	31B	31B	38C
TEST	32B	32B	38E
SYSCLKEN	33B	33B	38F
/RESET	10C	10C	3D
/RESOUT	11C	11C	4E
/RESIN	10D	10D	3F
WDI	8D	8D	3A
/PWROFF_CORE	38A	38A	40E
/PWROFF_1V2	39A	39A	40D
/PWROFF_1V8	40A	40A	40F

Table 36: A/D Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

A/D			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
ADIN0	48C	48C	16E
ADIN1	48D	48D	16B
ADIN2	49C	49C	16F
VSSad_ext	50C	50C	17A
VDDad_ext	50D	50D	17E

Table 37: PWM Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

PWM			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
PWM_OUT1	36C	36C	12B
PWM_OUT2	37D	37D	12F

Table 38: I²C Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

I²C			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
I2C1_SCL	31C	31C	10F
I2C1_SDA	32D	32D	11C
I2C2_SCL	35D	35D	12E
I2C2_SDA	36D	36D	12D

Table 39: UART Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

UART			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
U1_TX	28C	28C	9F
U1_RX	26C	26C	9A
U2_TX	17D	17D	6C
U2_RX	16D	16D	6A
U2_HCTS	26D	26D	9E
GPO_23/U2_HRTS	25D	25D	8F
U2_TX_RS232	23D	23D	8E
U2_RX_RS232	22D	22D	7F
U2_HCTS_RS232	46D	46D	16A
U2_HRTS_RS232	47D	47D	16C
U3_TX	25C	25C	8D
U3_RX	24C	24C	8B
U3_TX_RS232	28D	28D	10A
U3_RX_RS232	27D	27D	9B
GPO_21/U4_TX	30C	30C	10E
GPI_10/U4_RX	29C	29C	10C
U5_TX	20C	20C	7A
U5_RX	19C	19C	6F
U5_TX_RS232	23C	23C	8A
U5_RX_RS232	21C	21C	7B
U6_IRTX	31D	31D	11A
U6_IRRX	30D	30D	10B
U7_TX	33D	33D	11B
U7_RX	33C	33C	11E

GPO_22/U7_HRTS	34C	34C	11F
U7_HCTS	35C	35C	12A

Table 40: Keyboard Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

KEYBOARD			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
KEY_COL0	2B	2B	28E
KEY_COL1	3B	3B	28F
KEY_COL2	3A	3A	28B
KEY_COL3	4A	4A	29A
KEY_COL4	5A	5A	29E
KEY_COL5	5B	5B	29B
GPI_8/KEY_COL6/SPI2_BUSY	6A	6A	29D
GPI_9/KEY_COL7	6B	6B	29F
KEY_ROW0	7B	7B	30A
KEY_ROW1	8B	8B	30B
KEY_ROW2	8A	8A	30E
KEY_ROW3	9A	9A	30D
KEY_ROW4	10A	10A	30F
KEY_ROW5	10B	10B	31A
GPIO_2/KEY_ROW6	11A	11A	31E
GPIO_3/KEY_ROW7	11B	11B	31B

Table 41: Power Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

POWER			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
VCC	1C, 2C, 1D, 2D	1C, 2C, 1D, 2D	1A, 1C
VBAT	6C	6C	2B
VPD	6D	6D	2D
AGND	42C, 47C, 44D, 49D	42C, 47C, 44D, 49D	Connected to GND
GND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 3D, 9D, 14D, 19D,	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A,42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 4B, 9B, 14B, 19B, 24B, 29B, 34B,	3C, 4C, 7C, 8C, 9C, 12C, 13C, 14C, 17C, 18C, 19C, 22C, 23C, 24C, 27C, 29C, 30C, 31C, 34C, 35C, 36C, 39C, 40C,

	24D, 29D, 34D, 39D	39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 42D, 47D, 52D, 57D, 62D, 67D, 72D, 77D	41C, 44C, 45C, 46C, 49C, 50C, 51C, 54C, 4D, 5D, 6D, 9D, 10D, 11D, 14D, 15D, 16D, 9D, 20D, 21D, 24D, 25D, 26D, 28D, 31D, 32D, 33D, 36D, 37D, 38D, 41D, 42D, 43D, 46D, 47D, 48D, 51D, 52D, 53D, 1E, 2E, 1F

Table 42 below lists additional signals that are generated on the development board. Since these signals originate on the development board, they have no applicable connection to the phyCORE-module.

Table 42: Development Board Generated Signal Pin Assignment for the phyCORE-LPC3180 / Development Board / Expansion Board

DEVELOPMENT BOARD GENERATED SIGNALS			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
MMC_DETECT	N/A	38B	40B
MMC_PWR	N/A	40B	41A
MMC_WP	N/A	41A	41E
LED1_C	N/A	41B	41B
LED2_C	N/A	42B	41F
LED3_C	N/A	43A	42A
LED4_C	N/A	43B	42C
ADC_VADJ	N/A	46C	15F
BUTTON1	N/A	44A	42E
/BUTTON1	N/A	45A	42B
BUTTON2	N/A	45B	42F
/BUTTON2	N/A	46A	43A

Table 43: Unused Pins on the phyCORE-LPC3180 / Development Board / Expansion Board

UNUSED PINS			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
NC	4D, 5D,7D, 4C, 5C, 8C, 38B, 40B, 41B, 42B, 43B, 45B, 46B, 47B, 48B, 50B, 41A, 43A, 44A, 45A, 46A, 48A, 49A, 50A	4D, 5D, 7D, 4C, 5C, 8C, 51D, 52D, 53D, 54D, 55D, 56D, 57D, 58D, 59D, 60, 61D, 62D, 63D, 64D, 65D, 66D, 67D, 68D, 69D, 70D, 71D, 72D, 73D, 74D, 75D, 76D, 77D, 78D, 79D, 80D, 51C, 52C, 53C, 54C, 55C, 56C, 57C,	1B, 1D 2A, 2C, 2F 3E 13E 17B, 17D, 17F 18A, 18B, 18D, 18E, 18F 19A, 19B, 19D, 19E, 19F

		58C, 59C, 60C, 61C, 62C, 63C, 64C, 65C, 66C, 67C, 68C, 69C, 70C, 71C, 72C, 73C, 74C, 75C, 76C, 77C, 78C, 79C, 80C, 46B, 47B, 48B, 50B, 51B, 52B, 53B, 54B, 55B, 56B, 57B, 58B, 59B, 60B, 61B, 62B, 63B, 64B, 65B, 66B, 67B, 68B, 69B, 70B, 71B, 72B, 73B, 74B, 75B, 76B, 77B, 78B, 79B, 80B,48A, 49A, 50A, 51A, 52A, 53A, 54A, 55A, 56A, 57A, 58A, 59A, 60A, 61A, 62A, 63A, 64A, 65A, 66A, 67A, 68A, 69A, 70A, 71A, 72A, 73A, 74A, 75A, 76A, 77A, 78A, 79A, 80A	20A, 20B, 20C, 20E, 20F 21A, 21B, 21C, 21E, 21F 22A, 22B, 22D, 22E, 22F 23A, 23B, 23D, 23E, 23F 24A, 24B, 24E, 24F 25A, 25B, 25C, 25E, 25F 26A, 26B, 26C, 26E, 26F 27A, 27B, 27D, 27E, 27F 43B, 43C, 43E, 43F 44A, 44B, 44D, 44E, 44F 45A, 45B, 45D, 45E, 45F 46A, 46B, 46E, 46F 47A, 47B, 47C, 47E, 47F 48A, 48B, 48C, 48E, 48F 49A, 49B, 49D, 49E, 49F 50A, 50B, 50D, 50E, 50F 51A, 51B, 51E, 51F 52A, 52B, 52C, 52E, 52F 53A, 53B, 53C, 53E, 53F 54A, 54B, 54D, 54E, 54F

13 Revision History

Date	Version numbers	Changes in this manual
11-Apr-2006	Manual L-681e_1 PCM-031 PCB# 1247.0 PCM-967 PCB# 1248.0	First draft, Preliminary documentation. Describes the phyCORE-LPC3180 only

14 Component Placement Diagram

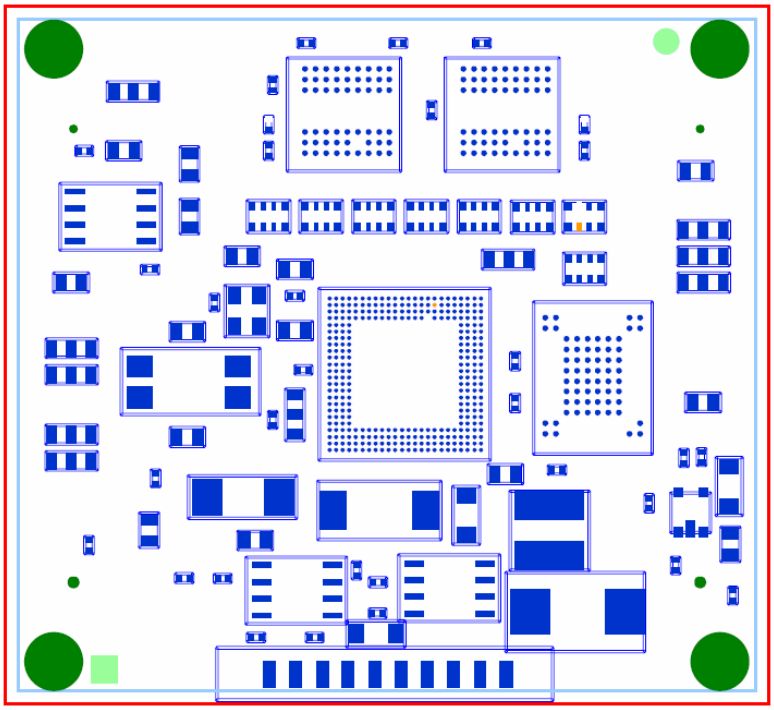

Figure 21: phyCORE-LPC3180 Component Placement, Top View

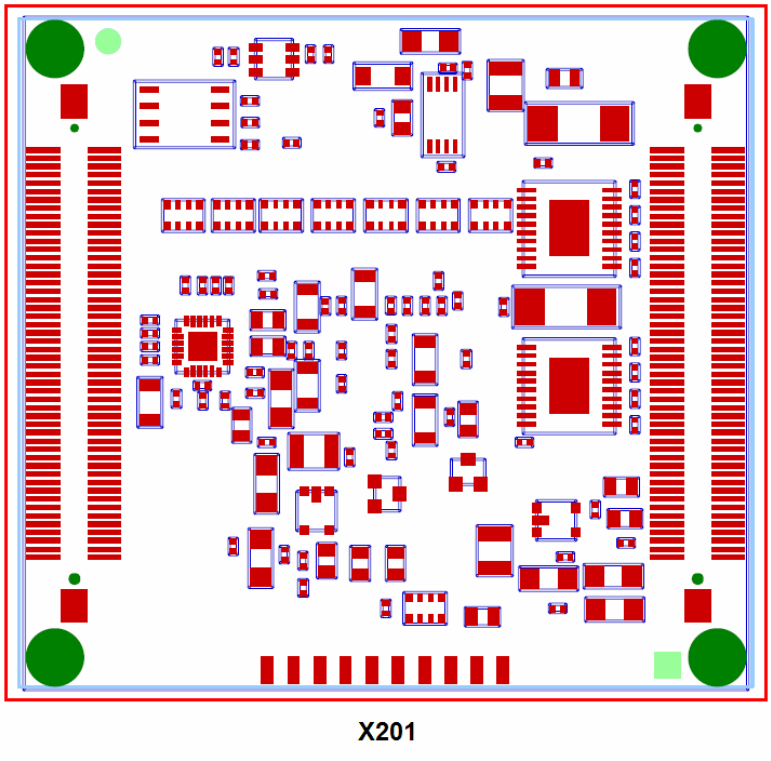

Figure 22: phyCORE-LPC3180 Component Placement, Bottom View

Index

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X

Document:	**phyCORE-LPC3180**
Document number:	**L-681e_0, Preliminary Version, April 2006**

How would you improve this manual?

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