

## SEMIDRIVER®

### High Power IGBT Driver SKHI 10<sup>5)</sup> SKHI 10/17<sup>6)</sup>



Absolute Maximum Ratings (Ta=25 °C)			
Symbol	Term	Values	Unit
V <sub>S</sub>	Supply voltage primary	18	V
V <sub>iH</sub>	Input signal voltage (HIGH) (for 15 V and 5 V input level)	V <sub>S</sub> + 0,3	V
I <sub>outPEAK</sub>	Output peak current	± 8	A
I <sub>outAVmax</sub>	Output average current (max.)	± 100	mA
V <sub>CE</sub>	Collector-emitter voltage sense	1200 <sup>5)</sup> / 1700 <sup>6)</sup>	V
dv/dt	Rate of rise and fall of voltage (secondary to primary side)		kV/μs
V <sub>isol IO</sub>	Isolation test volt. IN-OUT (2 sec. AC)	4000	V
R <sub>gon min</sub>	minimal R <sub>gon</sub>	2,7	Ω
R <sub>goff min</sub>	minimal R <sub>goff</sub>	2,7	Ω
Q <sub>out/pulse</sub>	charge per pulse	9,6	μC
T <sub>op</sub>	Operating temperature	- 25 ... + 85	°C
T <sub>stg</sub>	Storage temperature	- 25 ... + 85	°C

Electrical Characteristics (Ta=25 °C)					
Symbol	Term	Values			Unit
		min	typ	max	
V <sub>S</sub>	Supply voltage primary	14,4	15,0	15,6	V
I <sub>S</sub>	Supply current (max.)		0,3 <sup>1)</sup>		A
I <sub>SO</sub>	Supply current primary side (no load)		90		mA
V <sub>iT+</sub>	Input threshold voltage (HIGH) for 15 V input level		12,5		V
			2,4		V
V <sub>iT-</sub>	Input threshold voltage (LOW) for 15 V input level			3,6	V
				0,50	V
V <sub>G(on)</sub>	Turn-on output gate voltage		+ 15		V
V <sub>G(off)</sub>	Turn-off output gate voltage		- 8		V
f	Maximum operating frequency		see fig. 15		
td(on) <sub>IO</sub>	Input-output turn-on propagation time		1,4 <sup>2)</sup>		μs
td(off) <sub>IO</sub>	Input-output turn-off propagation time		1,4 <sup>2)</sup>		μs
t <sub>d(err)</sub>	Error input-output propagation time		1,0 <sup>3)</sup>		μs
V <sub>CEstat</sub>	Reference voltage for V <sub>CE</sub> monitoring		5,2 <sup>5)</sup> / 6,3 <sup>6)</sup>		V
R <sub>IN</sub>	Input resistance		10		kΩ
R <sub>gon</sub>	Internal gate resistor for ON signal		22 <sup>4)</sup>		Ω
R <sub>goff</sub>	Internal gate resistor for OFF signal		22 <sup>4)</sup>		Ω
C <sub>ps</sub>	Primary to secondary capacitance		12		pF

#### Features

- Single driver circuit for high power IGBTs
- SKHI 10 drives all SEMIKRON IGBTs with V<sub>CEs</sub> up to 1200 V (factory adjustment of V<sub>CEs</sub>-monitoring for 1200 V-IGBT)
- SKHI 10/17 drives all SEMIKRON IGBTs with V<sub>CE</sub> up to 1700 V (factory adjustment of V<sub>CE</sub>-monitoring for 1700 V-IGBT)
- CMOS/TTL (HCMOS) compatible input buffers
- Short circuit protection by V<sub>CE</sub> monitoring
- Soft short circuit turn-off
- Isolation due to transformers (no opto couplers)
- Supply undervoltage monitoring (< 13 V)
- Error memory / output signal (LOW or HIGH logic)
- Internal isolated power supply

#### Typical Applications

- High frequency SMPS
- Braking choppers
- Asymmetrical bridges
- High power UPS

<sup>1)</sup> This current value is a function of the output load condition

<sup>2)</sup> Typical value

<sup>3)</sup> This value does not consider t<sub>ON</sub> of IGBT and t<sub>MIN</sub> adjusted by R<sub>CE</sub> and C<sub>CE</sub>

<sup>4)</sup> Matched to be used with IGBTs < 100 A; for higher currents, see table 2

<sup>5)</sup> With R<sub>CE</sub> = 18 kΩ, C<sub>CE</sub> = 330 pF; see fig. 6 (SKHI 10; for IGBT up to 1200 V)

<sup>6)</sup> With R<sub>CE</sub> = 36 kΩ, C<sub>CE</sub> = 470 pF; (SKHI 10/17; for IGBT up to 1700 V)

# Block diagram SKHI10

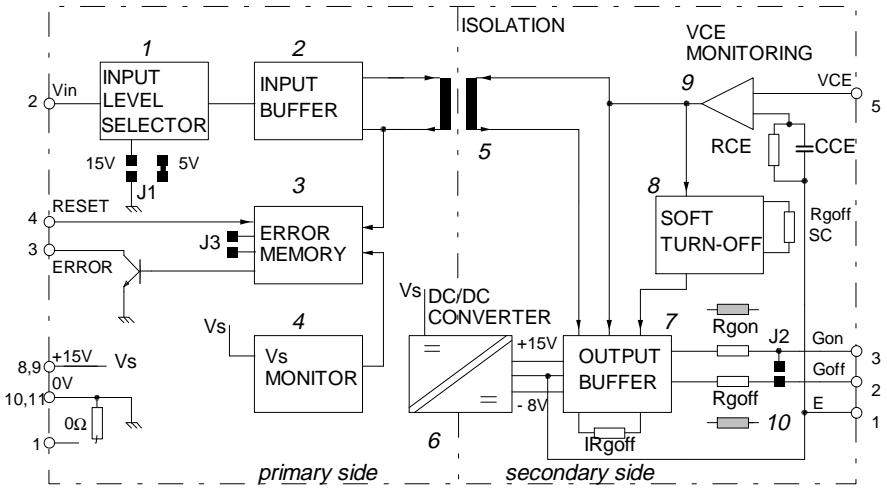
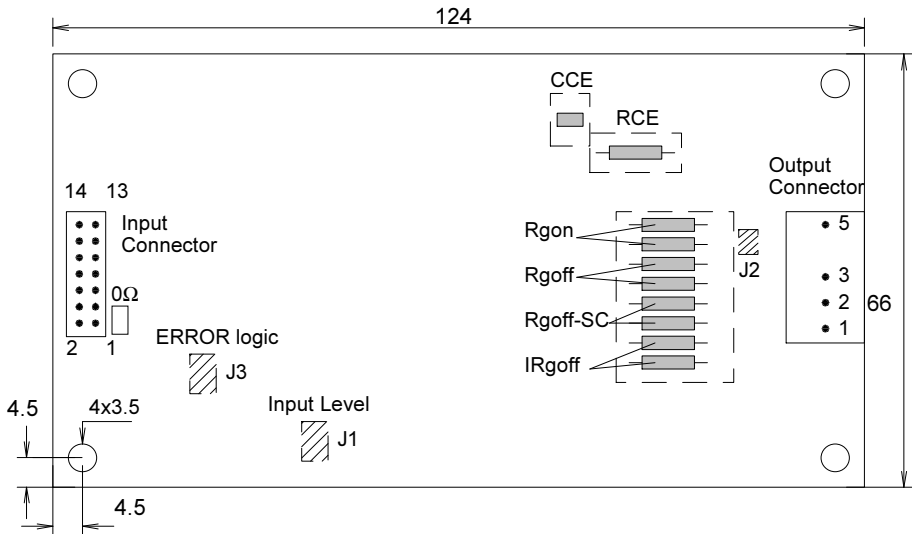


Fig.1 The numbers refer to the description on page 4, section B.



Input connector = 14 pin flat cable according to DIN 41651  
Output connector = MOLEX 41791 Series (mates with 41695 crimp terminal housing and crimp terminals 7258)

Fig.2 Dimensions (in mm) and connections of the SKHI 10

## SEMIDRIVER® SKHI 10

### SEMIDRIVER® SKHI 10/17

#### High Power Single IGBT Driver

##### General

The intelligent single IGBT driver, SKHI10 respectively SKHI 10/17 is a standard driver for all power IGBTs on the market.

The high power output capability was designed to switch high current modules or several paralleled IGBTs even for high frequency applications. The output buffer has been improved to make it possible to switch up to 400A IGBT modules at frequencies up to 20kHz.

A new function has been added to the short circuit protection circuitry (Soft Turn Off), this automatically increases the IGBT turn off time and hence reduces the DC voltage overvoltage spikes, enabling the use of higher DC-bus voltages. This means an increase in the final output power. An integrated DC/DC converter with high galvanic isolation (4 kV) ensures that the user is protected from the high voltage (secondary side).

The power supplies for the driver may be the same as used in the control board (0/+15V) without the requirement of isolation. All information that is transmitted between input and output uses ferrite transformers, resulting in high dv/dt immunity (75kV/μs).

The driver input stage is connected directly to the control board output and due to different control board operating voltages the SKHI10's input circuit includes a user voltage level selector (+15V or +5V).

In the following only the designation SKHI 10 is used. This is valid for both driver versions. If something is to be explained special to SKHI 10/17 it will be described by marking SKHI 10/17.

##### A. Features and Configuration of the Driver

A short description is given below. For detailed information, please refer to section B.

- a) The SKHI10 has an INPUT LEVEL SELECTOR circuit which is adjusted by J1 for two different levels. It is present for CMOS (15V) level, but can be changed by the user to HCMOS (5V) level by solder bridging the pads marked J1 together. For long input cables, we do not recommend the 5V level due to possible disturbances emitted by the power side.
- b) The ERROR MEMORY blocks the transmission of all turn-on signals to the IGBT if either a short circuit or malfunction of  $V_S$  is detected, and sends a signal to the external control board through an open collector transistor.
- c) With a FERRITE TRANSFORMER the information between primary and secondary may flow in both directions and high levels of dv/dt and isolation are obtained.
- d) A high frequency DC/DC CONVERTER avoids the requirement of external isolated power supplies to obtain the necessary gate voltage. An isolated ferrite transformer in half-bridge configuration supplies the

necessary power to the gate of the IGBT. With this feature, we can use the same power supply used in the external control circuit, even if we are using more than one SKHI10, e.g. in H-bridge configurations.

- e) Short circuit protection is provided by measuring the collector-emitter voltage with a  $V_{CE}$  MONITORING circuit. An additional circuit detects the short circuit after a delay (determined by  $R_{CE,CCE}$ ) and decreases the turn off speed (adjusted by  $R_{goff-SC}$ ) of the IGBT. SOFT TURN-OFF under fault conditions is necessary as it reduces the voltage overshoot and allows for a faster turn off during normal operation.
- f) The OUTPUT BUFFER is responsible for providing the correct current to the gate of the IGBT. If these signals do not have sufficient power, the IGBT will not switch properly, and additional losses or even the destruction of the IGBT may occur. According to the application (switching frequency and gate charge of the IGBT) the equivalent value of  $R_{gon}$  and the  $R_{goff}$  must be matched to the optimum value. This can be done by putting additional parallel resistors  $R_{gon}$ ,  $R_{goff}$  with those already on the board. If only one IGBT is to be used, (instead of parallel connection) only one cable could be connected between driver and gate by soldering the two J2 areas together.

Fig.1 shows a simplified block diagram of the SKHI10 driver. Some preliminary remarks will help the understanding:

- Regulated +15V must be present between pins 8,9 ( $V_S$ ) and 10,11 ( $\bar{L}$ ); an input signal (ON or OFF command to the IGBTs) from the control system is supplied to pin 2 ( $V_{in}$ ) where HIGH=ON and LOW=OFF.
- Pin 5 ( $V_{CE}$ ) at secondary side is normally connected to the collector of the IGBT to monitor  $V_{CE}$ , but for initial tests without connecting the IGBT it must be connected to pin 1 (E) to avoid ERROR signal and enable the output signals to be measured.
- The RESET input must be connected to 0V to enable the  $V_{in}$  signal. If it is left opened, the driver will be blocked.
- To monitor the error signal, a pull-up resistor must be provided between pin 3 (ERROR) and  $V_S$ .

##### B. Description of the Circuit Block Diagram (Fig. 1)

The circuit in Fig. 1 shows the input on the left and output on the right (primary/secondary).

###### 1. Input level circuit

This circuit was designed to accept two different logic voltage levels. The standard level is +15V (factory adjusted) intended for noisy environments or when long connections ( $l > 50$  cm) between the external control circuit and SKHI10 are used, where noise immunity must be considerable. For

lower power, and short connections between control and driver, the TTL-HCMOS level (+5V) can be selected by carefully soldering the small areas of J1 together, specially useful for signals coming from  $\mu P$  based controllers.

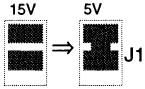


Fig.3 Selecting J1 for 5V level (TTL)

When connecting the SKHI10 to a control board using short connections no special attention needs to be taken (Fig. 4a).

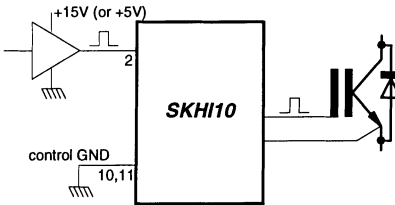


Fig.4a Connecting the SKHI10 with short cable

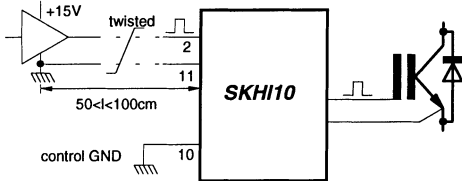


Fig.4b Connecting the SKHI10 with long cable

Otherwise, if the length is 50cm or more (we suggest to limit the cable length to about 1 meter), some care must be taken. The TTL level should be avoided and CMOS/15V is to be used instead; flat cable must have the pairs of conductors twisted or be shielded to reduce EMI/RFI susceptibility (Fig. 4b). If a shielded cable is used, it can be connected to pin 1. It is coupled to 0V through a resistor ( $0 \Omega$ ).

As the input impedance of the INPUT LEVEL SELECTOR circuit is very high, an internal pull-down resistor keeps the IGBT in OFF state in case the  $V_{in}$  connection is interrupted or left non connected.

## 2. Input buffer

This circuit enables and amplifies the input signal  $V_{in}$  to be transferred to the pulse transformer when RESET (pin 4) is LOW and also prevents spurious signals being transmitted to the secondary side.

The following overview is showing the input threshold voltages

$V_{IT+}$ (High)	min	typ	max
15 V	9,5 V	11,0 V	12,5 V
5 V	1,8 V	2,0 V	2,4 V

$V_{IT-}$ (Low)	min	typ	max
15 V	3,6 V	4,2 V	4,8 V
5 V	0,50 V	0,65 V	0,80 V

## 3. Error memory and reset signal

The ERROR memory is triggered only by following events:

- short circuit of IGBTs
- $V_S$ -undervoltage

In case of short circuit, the  $V_{CE}$  monitor sends a trigger signal (fault signal) through the impulse transformer to a FLIP-FLOP on the primary side giving the information to an open-collector transistor (pin 3), which may be connected to the external control circuit as ERROR message in HIGH logic (or LOW if J3 is short-circuited). If  $V_S$  power supply falls below 13V for more than 0,5ms, the same FLIP-FLOP is set and pin 3 is activated. For HIGH logic (default), an external  $R_C$  must be connected preferentially in the control main board. In this way the connection between main board and driver is also checked.

If low-logic version is used (J3 short-circuited), an internal pull-up resistor (internally connected to  $V_S$ ) is provided, and the signal from more SKHI10s can be connected together to perform an wired-or-circuit.

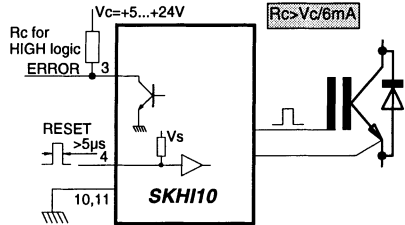


Fig.5 Driver status information ERROR, and RESET

The ERROR signal may be disabled either by RESET=HIGH (pin4) or by switching the power supply ( $V_S$ ) off. The width of the RESET pulse must be more than 5 $\mu$ s, and in case of interrupted connection an internal pull-up resistor will act.

FAULT	RESET	ERROR <sup>1)</sup>	$V_{in}$
no	0	0	enable
no	1	0	disable
yes	0	1	disable
yes	1	0	disable

1) default logic (HIGH); for LOW logic the signals are complementary

Table 1 ERROR signal truth table

The open-collector transistor (pin 3) may be connected through a pull-up resistor to an external (internal  $V_S$ ) for the "low-logic" version) voltage supply +5V...+24V, limiting the current to  $I_{sink} \leq 6mA$ .

## 4. Power supply ( $V_S$ ) monitor

The supply voltage  $V_S$  is monitored. If it falls below 13V an ERROR signal is generated and the turn-on pulses for the IGBT's gate are blocked.

## 5. Pulse transformer

It transmits the turn-on and turn-off signals to the IGBT. In the reverse direction the ERROR signal from the  $V_{CE}$  monitoring is transmitted via the same transformer. The isolation is 4 kV.

## 6. DC/DC converter

In the primary side of the converter, a half-bridge inverter transfers the necessary energy from  $V_s$  to the secondary of a ferrite transformer. In the secondary side, a full bridge and filters convert the high frequency signal coming from the primary to DC levels (+15V/- 8V) that are stabilised by a voltage regulator circuit.

## 7. Output buffer

The output buffer is supplied by the +15V/- 8V from the DC/DC converter. If the operation proceeds normally (no fault), the on- and off-signal is transmitted to the gate of an IGBT through  $R_{gon}$  and  $R_{goff}$ . The output stage has a MOSFET pair that is able to source/sink up to 8A peak current to/from the gate improving the turn-on/off time of the IGBT. Additionally, we can select  $I_{Rgoff}$  (see Fig. 2) either to discharge the gate capacitance with a voltage source (standard) or with a current source, specially design for the 1700V IGBT series (it speeds up the turn-off time of the IGBT). The present factory setting is voltage source ( $I_{Rgoff} = 0\Omega$ ). Using the current source  $I_{Rgoff}$ ,  $R_{goff}$  must be 0  $\Omega$ .

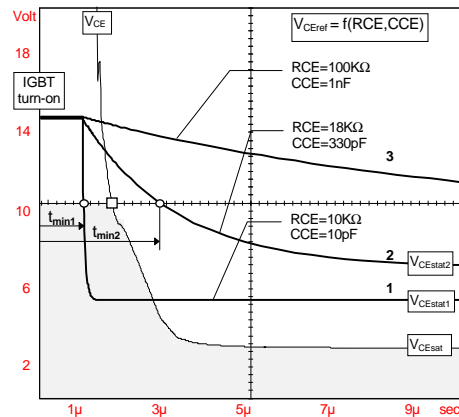


Fig.6  $V_{CEref}$  waveform with parameters  $R_{CE}$ ,  $C_{CE}$

## 8. Soft turn-off

In case of short-circuit, a further circuit (SOFT TURN-OFF) increases the resistance in series with  $R_{goff}$  and turns-off the IGBT at a lower speed. This produces a smaller voltage spike (due  $LSTRAY \times di/dt$ ) above the DC link by reducing the  $di/dt$  value. Because in short-circuit conditions the Homogeneous IGBT's peak current increases up to 8 times the nominal current (up to 10 times with Epitaxial IGBT structures), and some stray inductance is ever present in power circuits, it must fall to zero in a longer time than at normal operation. This "soft turn-off time" can be reduced by connecting a parallel resistor  $R_{goff-SC}$  (see Fig. 2) with those already on the printed circuit board.

## 9. $V_{CE}$ monitoring

This circuit is responsible for short-circuit sensing. Due to the direct measurement of  $V_{CEstat}$  on the IGBT's collector, it blocks the output buffer (through the soft turn-off circuit) in case of short-circuit and sends a signal to the ERROR memory on the primary side. The recognition of which  $V_{CE}$  level must be considered as a short circuit event, is adjusted by  $R_{CE}$  and  $C_{CE}$  (see Fig. 2), and it depends of the IGBT used. Typical values  $R_{CE} = 18k\Omega$  and  $C_{CE} = 330 pF$  for SKHI 10 are delivered from factory (Fig. 6, curve 2). Using SKHI 10/17 the driver will be delivered with  $R_{CE} = 36 k\Omega$  and  $C_{CE} = 470 pF$  from factory.

The  $V_{CEref}$  is not static but a dynamic reference which has an exponential shape starting at about 15V and decreases to  $V_{CEstat}$  ( $5V \leq V_{CEstat} \leq 10V$  determined by  $R_{CE}$ ), with a time constant  $\tau$  ( $0.5 \mu s \leq \tau \leq 1 ms$  controlled by  $C_{CE}$ ). The  $V_{CEstat}$  must be adjusted to remain above  $V_{CEsat}$  in normal operation (the IGBT is already in full saturation).

To avoid a false failure indication when the IGBT just starts to conduct ( $V_{CEsat}$  value is still too high) some decay time must be provided for the  $V_{CEref}$ . As the  $V_{CE}$  signal is internally limited at 10V, the decay time of  $V_{CEref}$  must reach this level after  $V_{CE}$  or a failure indication will occur (see Fig.6, curve 1). A  $t_{min}$  is defined as function of  $V_{CEstat}$  and  $\tau$  to find out the best choice for  $R_{CE}$  and  $V_{CE}$  (see Fig.6, curve 2). The time the IGBT come to the 10V (represented by a „□“ in Fig. 6) depends on the IGBT itself and  $R_{gon}$  used.

The  $R_{CE}$  and  $C_{CE}$  values can be found from Fig. 7 by taking the  $V_{CEstat}$  and  $t_{min}$  as input values with following remarks:

- $R_{CE} > 10K\Omega$
- $C_{CE} < 2,7nF$

**Attention!** If this function is not used, for example during the experimental phase, the  $V_{CE}$  MONITORING must be connected with the EMITTER output to avoid possible fault indication and consequent gate signal blocking.

## 10. $R_{gon}$ , $R_{goff}$

These two resistors are responsible for the switching speed of each IGBT. As an IGBT has input capacitance (varying during the switching time) which must be charged and discharged, both resistors will dictate what time must be taken to do this. The final value of resistance is difficult to predict, because it depends on many parameters, as follows:

- DC-link voltage
- stray inductance of the circuit
- switching frequency
- type of IGBT

## C. Operating Procedure

### 1. One IGBT connection

To realize the correct switching and short-circuit monitoring of one IGBT some additional external components must be used (Fig.8).

The driver is delivered with four  $R_g$  resistors (43 $\Omega$ ). This value can be reduced to use the driver with bigger modules or higher frequencies/lower voltages, by putting additional resistors in parallel to the existing ones.

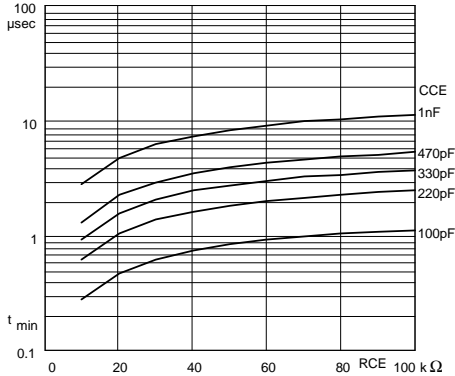


Fig.7a  $t_{min}$  as function of  $R_{CE}$  and  $C_{CE}$

The outputs  $G_{on}$  and  $G_{off}$  were previewed to connect the driver with more than one IGBT (paralleling). In that case we need both signals ON/OFF separately to connect additional external resistors  $R_{gon}$  and  $R_{goff}$  for each IGBT. If only one IGBT is to be used, we suggest to connect both points together through J2 (see Fig. 1 and 2). This can be done by soldering the two small pads together, which saves one external connection.

Typical component values: \*)

SK-IGBT-Module	$R_{Gon}$ $\Omega$	$R_{Goff}$ $\Omega$	$C_{CE}$ pF	$R_{CE}$ k $\Omega$	$I_{Rgoff}$ $\Omega$
SKM 75GAL123D	22	22	330	18	0
SKM 100GAL(R)123D	15	15	330	18	0
SKM 150GAL(R)123D	12	12	330	18	0
SKM 200GA(L/R)123D	10	10	330	18	0
SKM 300GA(L/R)123D	8,2	8,2	330	18	0
SKM 400GA123D	6,8	6,8	330	18	0
SKM 500GA123D	5,6	5,6	330	18	0

Table 2a 1200V IGBT @ DC-link < 700V

SK-IGBT-Module	$R_{Gon}$ $\Omega$	$R_{Goff}$ $\Omega$	$C_{CE}$ pF	$R_{CE}$ k $\Omega$	$I_{Rgoff}$ $\Omega$
SKM 200GAL173D	8,2	8,2	470	36	0
SKM 300GA173D	6,8	6,8	470	36	0
SKM 400GA173	5,6	5,6	470	36	0

Table 2b 1700V IGBT @ DC-link < 1000V

\*) Only starting values, for final optimization.

The adjustment of  $R_{goffSC}$  (factory adjusted  $R_{goffSC} = 22 \Omega$ ) should be done observing the overvoltages at the module in case of short circuit. When having a low inductive DC-link the module can be switched off faster.

**The values shown should be considered as standard values for a mechanical/electrical assembly, with ac-**

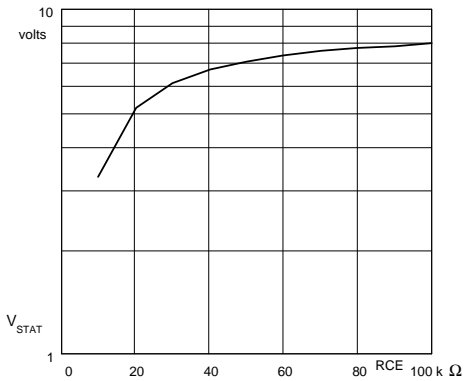


Fig. 7b  $V_{CEstat}$  as function of  $R_{CE}$

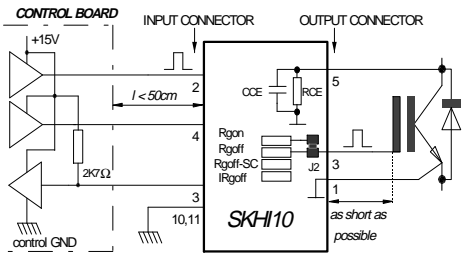


Fig. 8 Preferred standard circuit

**ceptable stray inductance level, using only one IGBT per SKH10 driver. The final optimized value can be found only by measuring.**

## 2. Paralleling IGBTs

The parallel connection is recommended only by using IGBTs with homogeneous structure (IGHT), that have a positive temperature coefficient resulting in a perfect current sharing without any external auxiliary element. After all some care must be considered to reach an optimized circuit and to obtain the total performance of the IGBT (Fig. 9). The IGBTs must have independent values of  $R_{gon}$  and  $R_{goff}$ . An auxiliary emitter resistor  $R_e$  as well as an auxiliary collector resistor  $R_c$  must also be used.

The external resistors  $R_{gonx}$ ,  $R_{goffx}$ ,  $R_{ex}$  and  $R_{cx}$  should be mounted on an additional circuit board near the paralleled modules, and the  $R_{gon}/R_{goff}$  on the driver should be changed to zero ohms.

The  $R_{ex}$  assumes a value of 0,5 $\Omega$  and its function is to compensate the wiring resistance in the auxiliary emitters what could make the emitter voltage against ground unbalanced.

The  $R_{cx}$  assumes a value of 47  $\Omega$  and its function is to create an average value of  $V_{CEsat}$  in case of short circuit for  $V_{CE}$

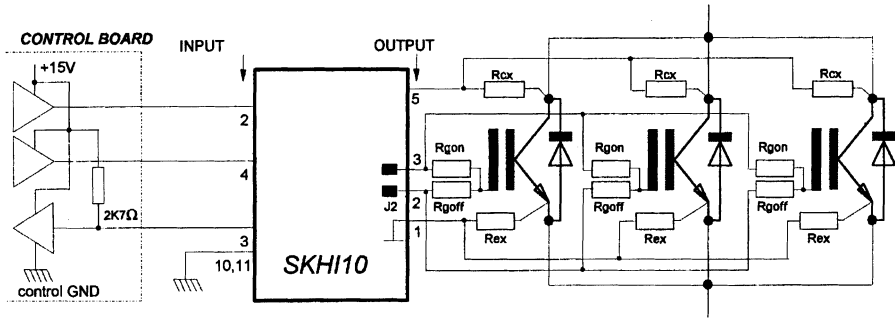


Fig.9 Preferred circuit for paralleled IGBTs

monitoring.

The mechanical assembly of the power circuit must be symmetrical and low inductive.

The maximum recommended gate charge is  $9,6\mu\text{C}$ .  
See also Fig.14.

#### D. Signal Waveforms

The following signal waveforms were measured under the conditions below:

- $V_S = 15\text{V}$
- $T_{\text{amb}} = 25^\circ\text{C}$
- load = SKM150GAL161D
- $R_{\text{CE}} = 18\text{k}\Omega$
- $C_{\text{CE}} = 330\text{pF}$
- $U_{\text{DC}} = 1200\text{V}$
- $I_C = 100\text{A}$

All results are typical values if not otherwise specified.

The limit frequency of SKH110 depends on the gate charge connected in its output pins.

If small IGBT modules are used, the frequency could theo-

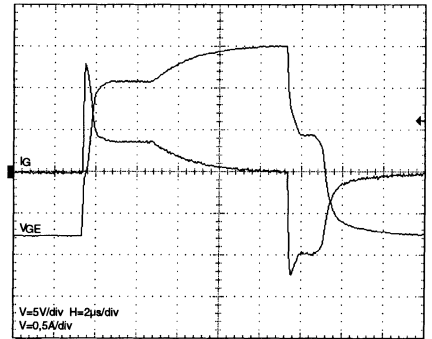


Fig.11 Output voltage ( $V_{\text{GE}}$ ) and output current ( $I_{\text{G}}$ )

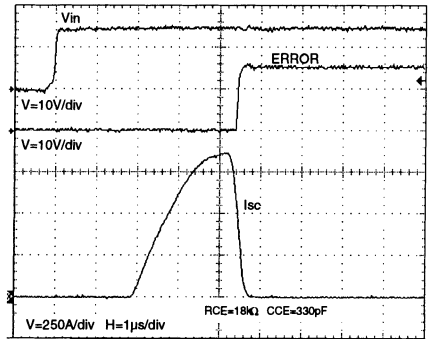


Fig.12 Short-circuit and ERROR propagation time worst-case ( $V_{\text{in}}$  with SC already present)

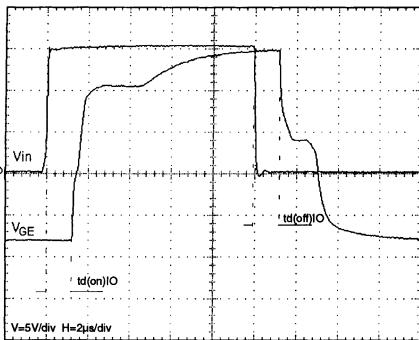


Fig.10 Input and output voltage propagation time

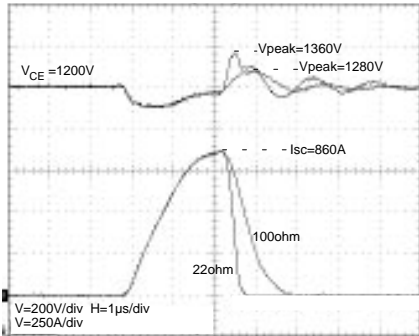


Fig.13 Effect of  $R_{goff-SC}$  in short - circuit

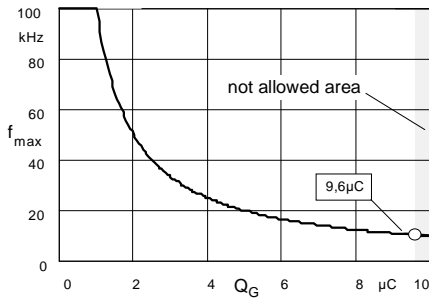


Fig.14 Maximum operating frequency x gate charge

retically reach 100kHz. For bigger modules or even paralleled modules, the maximum frequency must be determined (Fig. 14).  $Q_G$  is the total equivalent gate charge connected to the output of the driver. The maximum allowed value is limited ( $9,6\mu C$ ), and depends on the output internal capacitance connected to the power supply (energy storage capacitance).

## E. Application / Handling

1. The CMOS inputs of the driver are extremely sensitive to overvoltage. Voltages higher than ( $V_S + 0,3 V$ ) or under  $- 0,3 V$  may destroy these inputs.

Therefore the following safety requirements are to be observed:

- To make sure that the control signals do not comprise overvoltages exceeding the above values.
- Protection against static discharges during handling. As long as the hybrid driver is not completely assembled the input terminals must be short circuited. Persons working with CMOS devices should wear a grounded bracelet. Any floor coverings must not be chargeable. For transportation the input terminals must be short circuited using, for example, conductive rubber. Places of work must be grounded. The same foam requirements apply to the IGBTs.

2. The connecting leads between the driver and the power module must be as short as possible, and should be twisted.

3. Any parasitic inductance should be minimized. Overvoltages may be damped by C or RCD snubber networks between the main terminals [3] = C1 (+) and [2] = E2 (-) of the power module.

4. When first operating a newly developed circuit, low collector voltage and load current should be used in the beginning. These values should be increased gradually, observing the turn-off behavior of the free-wheeling diodes and the turn-off voltage spikes across the IGBT by means of an oscilloscope. Also the case temperature of the power module should be monitored. When the circuit works correctly, short circuit tests can be made, starting again with low collector voltage.

5. It is important to feed any ERROR back to the control circuit to switch the equipment off immediately in such events. Repeated turn-on of the IGBT into a short circuit, with a frequency of several kHz, may destroy the device.

For further details ask SEMIKRON

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