

# SN65LVDS048A LVDS QUAD DIFFERENTIAL LINE RECEIVER

SLLS451B– SEPTEMBER 2000 – REVISED SEPTEMBER 2002

- >400 Mbps (200 MHz) Signaling Rates
- Flow-Through Pinout Simplifies PCB Layout
- 50 ps Channel-to-Channel Skew (Typ)
- 200 ps Differential Skew (Typ)
- Propagation Delay Times 2.7 ns (Typ)
- 3.3-V Power Supply Design
- High Impedance LVDS Inputs on Power Down
- Low-Power Dissipation (40 mW at 3.3 V Static)
- Accepts Small Swing (350 mV) Differential Signal Levels
- Supports Open, Short, and Terminated Input Fail-Safe
- Industrial Operating Temperature Range (–40°C to 85°C)
- Conforms to TIA/EIA-644 LVDS Standard
- Available in SOIC and TSSOP Packages
- Pin-Compatible With DS90LV048A From National

## description

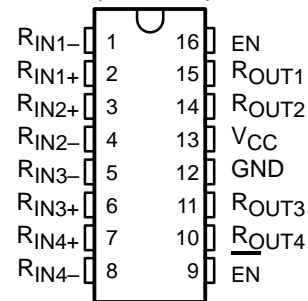
The SN65LVDS048A is a quad differential line receiver that implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the quad differential receivers will provide a valid logical output state with a  $\pm 100$ -mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100  $\Omega$ . The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.

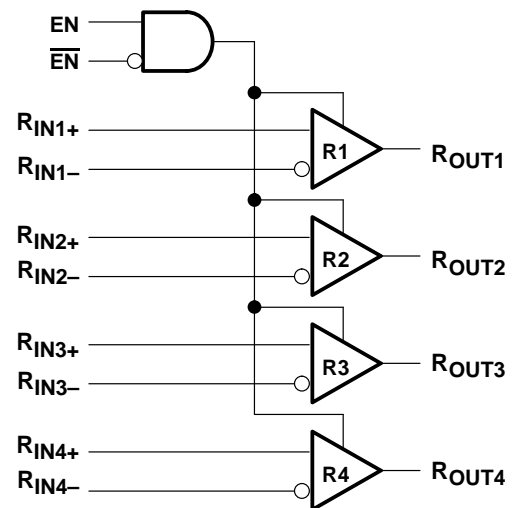
The SN65LVDS048A is characterized for operation from –40°C to 85°C.

SN65LVDS048AD (Marked as LVDS048A)  
SN65LVDS048APW (Marked as DL048A)

(TOP VIEW)



## functional diagram



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN65LVDS048A

## LVDS QUAD DIFFERENTIAL LINE RECEIVER

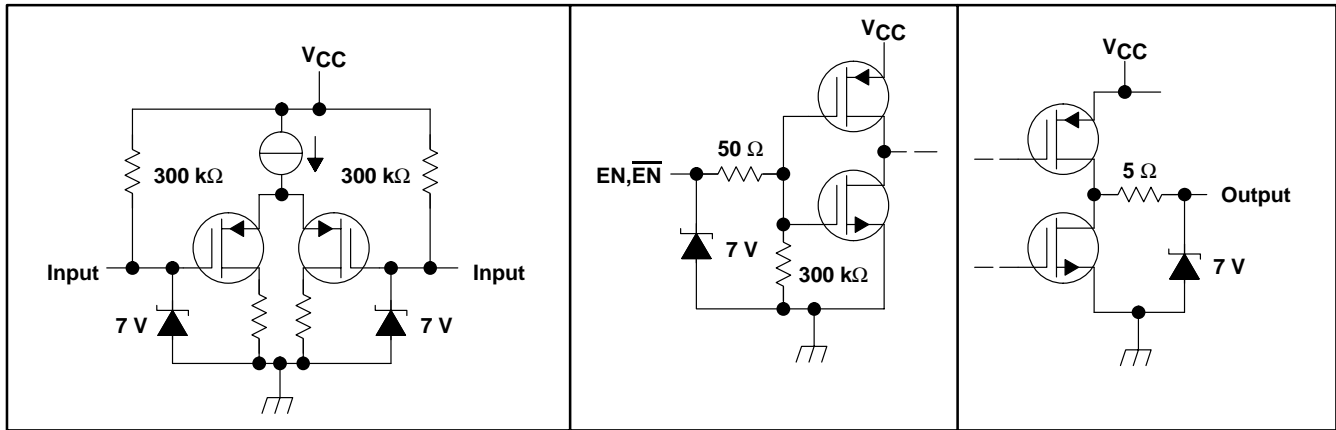
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TRUTH TABLE

| DIFFERENTIAL INPUT                   | ENABLES              |                        | OUTPUT |
|--------------------------------------|----------------------|------------------------|--------|
|                                      | EN                   | $\overline{\text{EN}}$ |        |
| $R_{\text{IN}+} - R_{\text{IN}-}$    | H                    | L or OPEN              | H      |
| $V_{\text{ID}} \geq 100 \text{ mV}$  |                      |                        | L      |
| $V_{\text{ID}} \leq -100 \text{ mV}$ |                      |                        | H      |
| Open/short or terminated             | All other conditions |                        | Z      |
| X                                    | All other conditions |                        | Z      |

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

### equivalent input and output schematic diagrams



### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

|   |   |
|---|---|
| Supply voltage range ( $V_{\text{CC}}$ )  | –0.3 V to 4 V                                 |
| Input voltage range, $V_{\text{I}}(R_{\text{IN}+}, R_{\text{IN}-})$               | –0.3 V to 4 V                                 |
| Enable input voltage ( $\text{EN}, \overline{\text{EN}}$ )                        | –0.3 V to ( $V_{\text{CC}} + 0.3 \text{ V}$ ) |
| Output voltage, $V_{\text{O}}(R_{\text{OUT}})$                                    | –0.3 V to ( $V_{\text{CC}} + 0.3 \text{ V}$ ) |
| Bus-pin ( $R_{\text{IN}+}, R_{\text{IN}-}$ ) Electrostatic discharge (see Note 2) | > 10 kV                                       |
| Continuous power dissipation  | See Dissipation Rating Table                  |
| Storage temperature range   | –65°C to 150°C                                |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds                      | 260°C   |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.  
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

| PACKAGE | $T_{\text{A}} \leq 25^{\circ}\text{C}$<br>POWER RATING | OPERATING FACTOR‡<br>ABOVE $T_{\text{A}} = 25^{\circ}\text{C}$ | $T_{\text{A}} = 85^{\circ}\text{C}$<br>POWER RATING |
|---------|--|--|---|
| D       | 950 mW   | 7.6 mW/°C  | 494 mW  |
| PW      | 774 mW   | 6.2 mW/°C  | 402 mW  |

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

# SN65LVDS048A

## LVDS QUAD DIFFERENTIAL LINE RECEIVER

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### recommended operating conditions

|                                       | MIN                  | NOM | MAX                        | UNIT |
|---------------------------------------|----------------------|-----|----------------------------|------|
| Supply voltage, $V_{CC}$              | 3                    | 3.3 | 3.6                        | V    |
| Receiver input voltage                | GND                  |     | 3                          | V    |
| Common-mode input voltage, $V_{IC}$   | $\frac{ V_{ID} }{2}$ |     | $2.4 - \frac{ V_{ID} }{2}$ | V    |
|                                       |                      |     | $V_{CC} - 0.8$             |      |
| Operating free-air temperature, $T_A$ | -40                  | 25  | 85                         | °C   |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

| PARAMETER  | TEST CONDITIONS   | MIN                                   | TYP†                  | MAX      | UNIT          |               |
|--|---|---------------------------------------|-----------------------|----------|---------------|---------------|
| $V_{IT+}$ Differential input high threshold voltage    | $V_{CM} = 1.2\text{ V}, 0.05\text{ V}, 2.35\text{ V}$<br>(see Note 4) |                                       |                       | 100      | mV            |               |
| $V_{IT-}$ Differential input low threshold voltage     |   | -100                                  |                       |          |               |               |
| $V_{(CMR)}$ Common mode voltage range                  | $V_{ID} = 200\text{ mV pk to pk}$ (see Note 5)                        | 0.1                                   |                       | 2.3      | V             |               |
| $I_{IN}$ Input current                                 | $V_{IN} = 2.8\text{ V}$   | $V_{CC} = 3.6\text{ V or }0\text{ V}$ | -20                   | $\pm 1$  | 20            | $\mu\text{A}$ |
|  | $V_{IN} = 0\text{ V}$   |                                       | -20                   | $\pm 1$  | 20            | $\mu\text{A}$ |
|  | $V_{IN} = 3.6\text{ V}$   |                                       | $V_{CC} = 0\text{ V}$ | -20      | $\pm 1$       | 20            |
| $V_{OH}$ Output high voltage                           | $I_{OH} = -0.4\text{ mA}, V_{ID} = 200\text{ mV}$                     | 2.7                                   | 3.2                   |          | V             |               |
|  | $I_{OH} = -0.4\text{ mA},$ input terminated                           | 2.7                                   | 3.2                   |          | V             |               |
|  | $I_{OH} = -0.4\text{ mA},$ input shorted                              | 2.7                                   | 3.2                   |          | V             |               |
| $V_{OL}$ Output low voltage                            | $I_{OL} = 2\text{ mA}, V_{ID} = -200\text{ mV}$                       |                                       | 0.05                  | 0.25     | V             |               |
| $I_{OS}$ Output short circuit current                  | Enabled, $V_{OUT} = 0\text{ V}$ (see Note 6)                          |                                       | -65                   | -100     | mA            |               |
| $I_{O(Z)}$ Output 3-state current                      | Disabled, $V_{OUT} = 0\text{ V or }V_{CC}$                            | -1                                    |                       | 1        | $\mu\text{A}$ |               |
| $V_{IH}$ Input high voltage                            |   | 2.0                                   |                       | $V_{CC}$ | V             |               |
| $V_{IL}$ Input low voltage                             |   | GND                                   |                       | 0.8      | V             |               |
| $I_I$ Input current (enables)                          | $V_{IN} = 0\text{ V or }V_{CC},$<br>Other input = $V_{CC}$ or GND     | -10                                   |                       | 10       | $\mu\text{A}$ |               |
| $V_{IK}$ Input clamp voltage                           | $I_{CL} = -18\text{ mA}$  | -1.5                                  | -0.8                  |          | V             |               |
| $I_{CC}$ No load supply current, receivers enabled     | $EN = V_{CC},$ Inputs open  |                                       | 8                     | 15       | mA            |               |
| $I_{CC(Z)}$ No load supply current, receivers disabled | $EN = GND,$ Inputs open   |                                       | 0.6                   | 1.5      | mA            |               |

† All typical values are at 25°C and with a 3.3-V supply.

- NOTES:
- Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.
  - $V_{CC}$  is always higher than  $R_{IN+}$  and  $R_{IN-}$  voltage,  $R_{IN-}$  and  $R_{IN+}$  have a voltage range of  $-0.2\text{ V to }V_{CC}-V_{ID}/2$ . To be compliant with ac specifications the common voltage range is 0.1 V to 2.3 V.
  - The VCMR range is reduced for larger  $V_{ID}$ . Example: If  $V_{ID} = 400\text{ mV}$ , the VCMR is 0.2 V to 2.2 V. The fail-safe condition with inputs shorted is not supported over the common-mode range of 0 V to 2.4 V, but is supported only with inputs shorted and no external common-mode voltage applied. A  $V_{ID}$  up to  $V_{CC}-0\text{ V}$  may be applied to the  $R_{IN+}$  and  $R_{IN-}$  inputs with the common-mode voltage set to  $V_{CC}/2$ . Propagation delay and differential pulse skew decrease when  $V_{ID}$  is increased from 200 mV to 400 mV. Skew specifications apply for  $200\text{ mV} < V_{ID} < 800\text{ mV}$  over the common-mode range.
  - Output short circuit current ( $I_{OS}$ ) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time. Do not exceed maximum junction temperature specification.



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**switching characteristics over recommended operating conditions (unless otherwise noted) (see Notes 7)**

| PARAMETER            |   | TEST CONDITIONS   | MIN | TYP† | MAX | UNIT |
|----------------------|---|---|-----|------|-----|------|
| t <sub>PHL</sub>     | Differential propagation delay, high-to-low                                   | C <sub>L</sub> = 15 pF<br>V <sub>ID</sub> = 200 mV<br>(see Figure 1 and 2 ) | 1.9 | 2.7  | 3.7 | ns   |
| t <sub>PLH</sub>     | Differential propagation delay, low-to-high                                   |   | 1.9 | 2.9  | 3.7 | ns   |
| t <sub>SK(p)</sub>   | Differential pulse skew (t <sub>PHLD</sub> – t <sub>PLHD</sub> ) (see Note 8) |   | 200 | 450  |     | ps   |
| t <sub>SK(o)</sub>   | Differential channel-to-channel skew; same device (see Note 8)                |   | 50  | 500  |     | ps   |
| t <sub>SK(pp)</sub>  | Differential part-to-part skew (see Note 10)                                  |   |     |      | 1   | ns   |
| t <sub>SK(lim)</sub> | Differential part-to-part skew (see Note 11)                                  |   |     |      | 1.5 | ns   |
| t <sub>r</sub>       | Rise time   |   |     | 0.5  | 1   | ns   |
| t <sub>f</sub>       | Fall time   |   |     | 0.5  | 1   | ns   |
| t <sub>PHZ</sub>     | Disable time high to Z  | R <sub>L</sub> = 2 K Ω<br>C <sub>L</sub> = 15 pF<br>(see Figure 3 and 4 )   |     | 8    | 9   | ns   |
| t <sub>PLZ</sub>     | Disable time low to Z   |   |     | 6    | 8   | ns   |
| t <sub>PZH</sub>     | Enable time Z to high   |   |     | 8    | 10  | ns   |
| t <sub>PZL</sub>     | Enable time Z to low  |   |     | 7    | 8   | ns   |
| f <sub>(MAX)</sub>   | Maximum operating frequency (see Note 12)                                     | All channels switching  | 200 | 250  |     | MHz  |

† All typical values are at 25°C and with a 3.3-V supply.

- NOTES:
- Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> and t<sub>f</sub> (0% – 100%) ≤ 3 ns for R<sub>IN</sub>.
  - t<sub>SK(p)</sub>|t<sub>PLH</sub> – t<sub>PHL</sub>| is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
  - t<sub>SK(o)</sub> is the differential channel-to-channel skew of any event on the same device.
  - t<sub>SK(pp)</sub> is the differential part-to-part skew, and is defined as the difference between the minimum and the maximum specified differential propagation delays. This specification applies to devices at the same VCC and within 5°C of each other within the operating temperature range.
  - t<sub>sk(lim)</sub> part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t<sub>sk(lim)</sub> is defined as |Min – Max| differential propagation delay.
  - f<sub>(MAX)</sub> generator input conditions: t<sub>r</sub> = t<sub>f</sub> < 1 ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% to 55%, V<sub>OD</sub> > 250 mV, all channels switching



PARAMETER MEASUREMENT INFORMATION

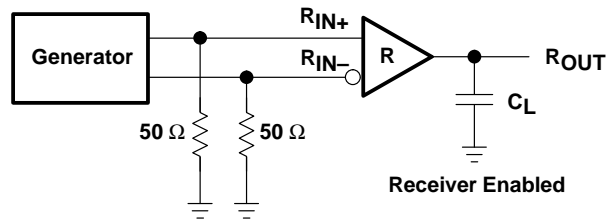


Figure 1. Receiver Propagation Delay and Transition Time Test Circuit

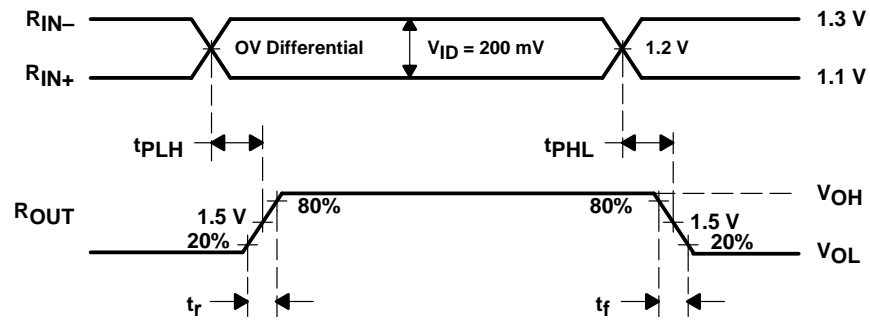
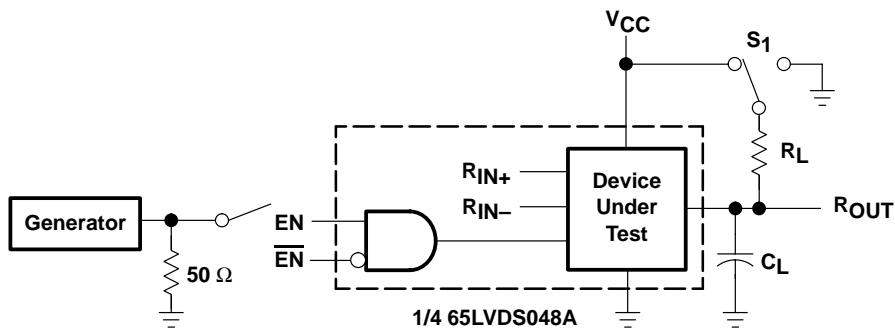


Figure 2. Receiver Propagation Delay and Transition Time Waveforms

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## PARAMETER MEASUREMENT INFORMATION



$C_L$  Includes Load and Test Jig Capacitance.  
 $S_1 = V_{CC}$  for  $t_{pZL}$  and  $t_{pLZ}$  Measurements.  
 $S_1 = GND$  for  $t_{pZH}$  and  $t_{pHZ}$  Measurements.

Figure 3. Receiver 3-State Delay Test Circuit

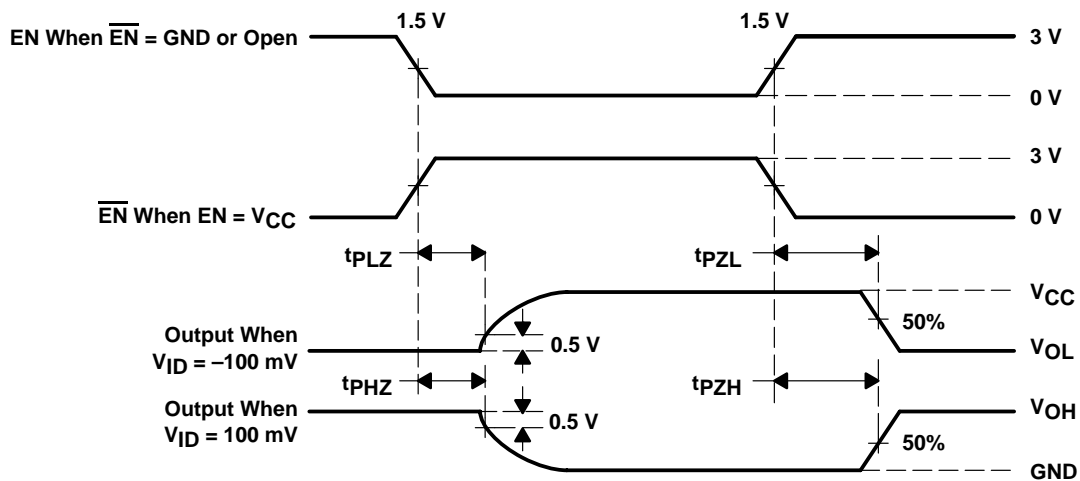


Figure 4. Receiver 3-State Delay Waveforms

TYPICAL CHARACTERISTICS

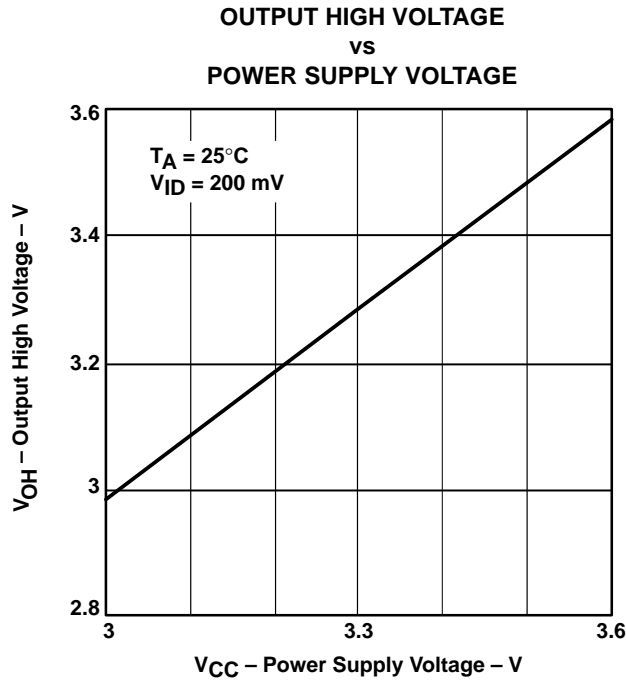


Figure 5

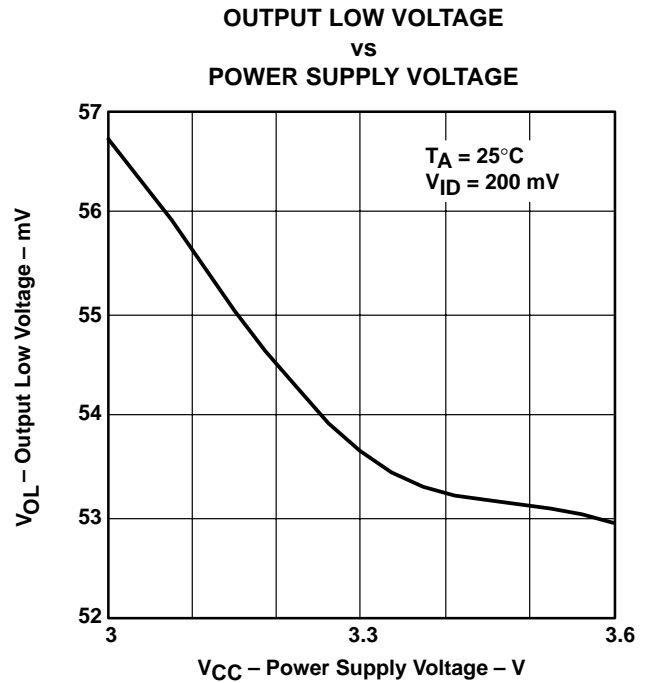


Figure 6

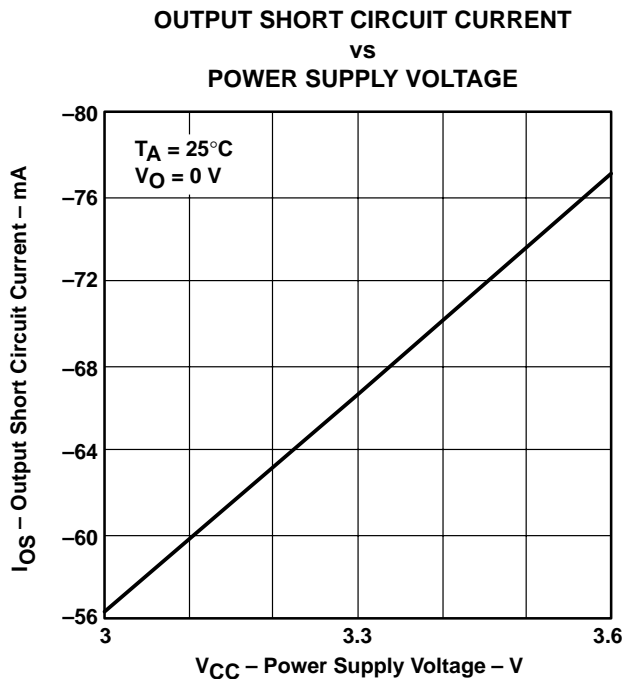


Figure 7

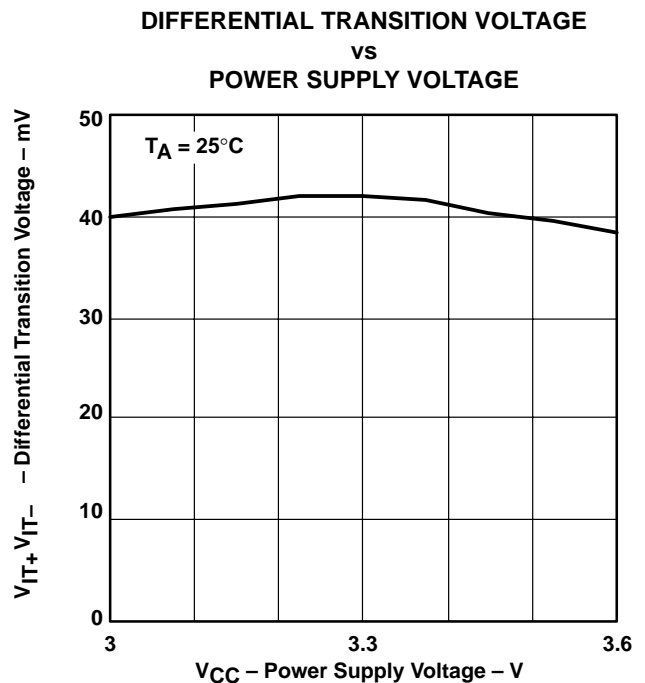
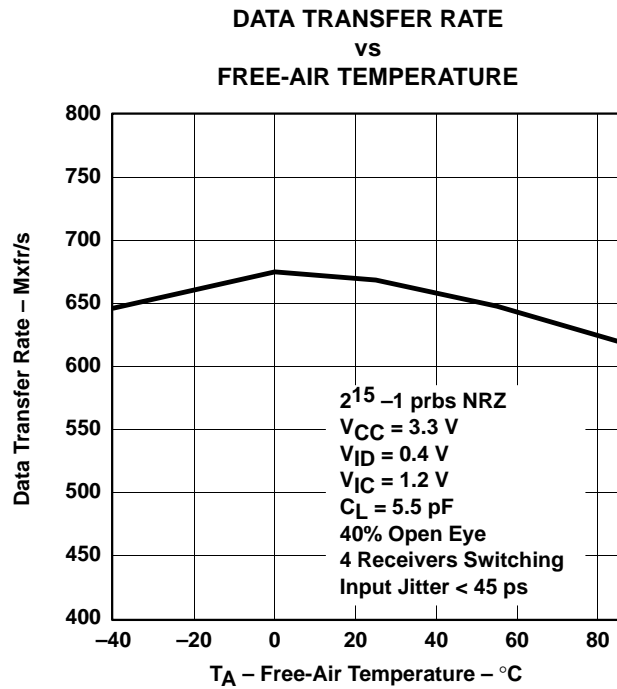
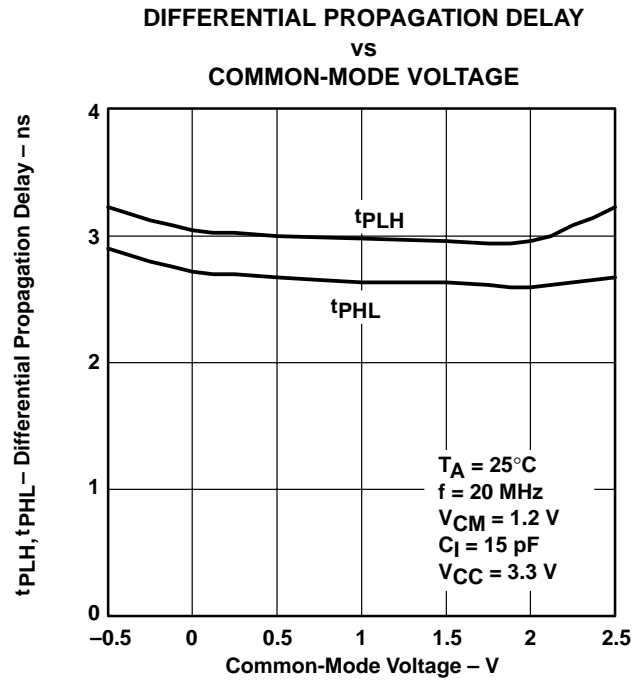
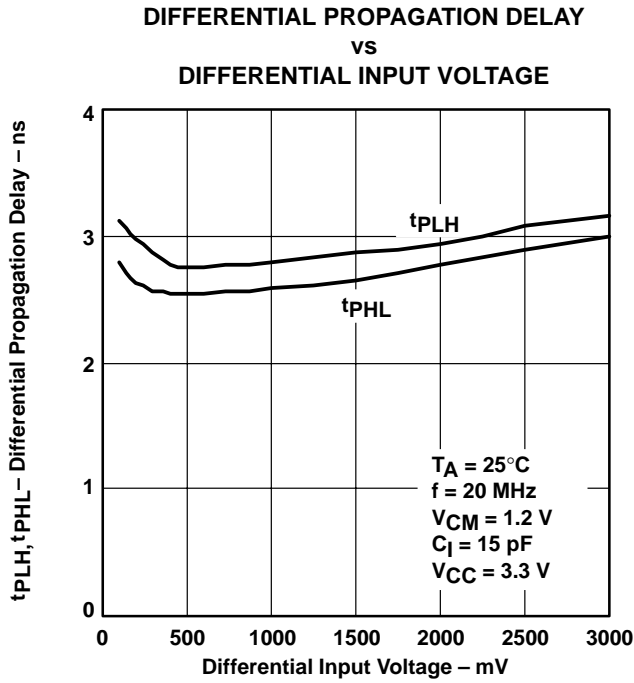


Figure 8

# SN65LVDS048A LVDS QUAD DIFFERENTIAL LINE RECEIVER

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## TYPICAL CHARACTERISTICS





APPLICATION INFORMATION

fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between  $-100\text{ mV}$  and  $100\text{ mV}$  and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near  $V_{CC}$  through  $300\text{-k}\Omega$  resistors as shown in Figure 10. The fail-safe feature uses an AND gate with input voltage thresholds at about  $2.3\text{ V}$  to detect this condition and force the output to a high-level regardless of the differential input voltage.

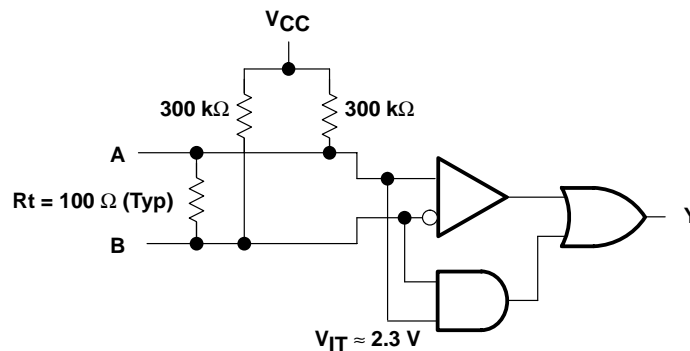


Figure 12. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a  $100\text{-mV}$  differential input voltage magnitude. The presence of the termination resistor,  $R_t$ , does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

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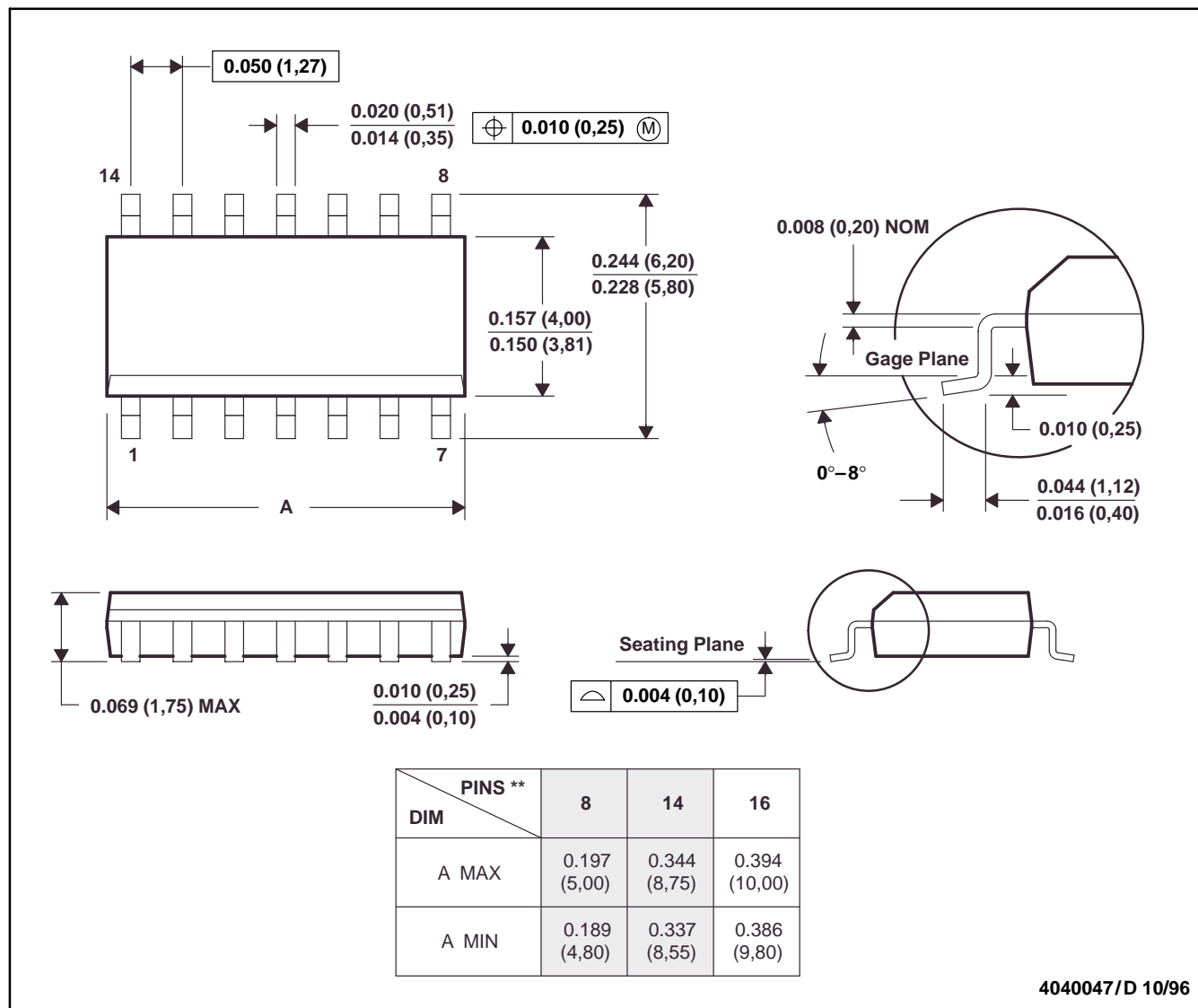
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## MECHANICAL DATA

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

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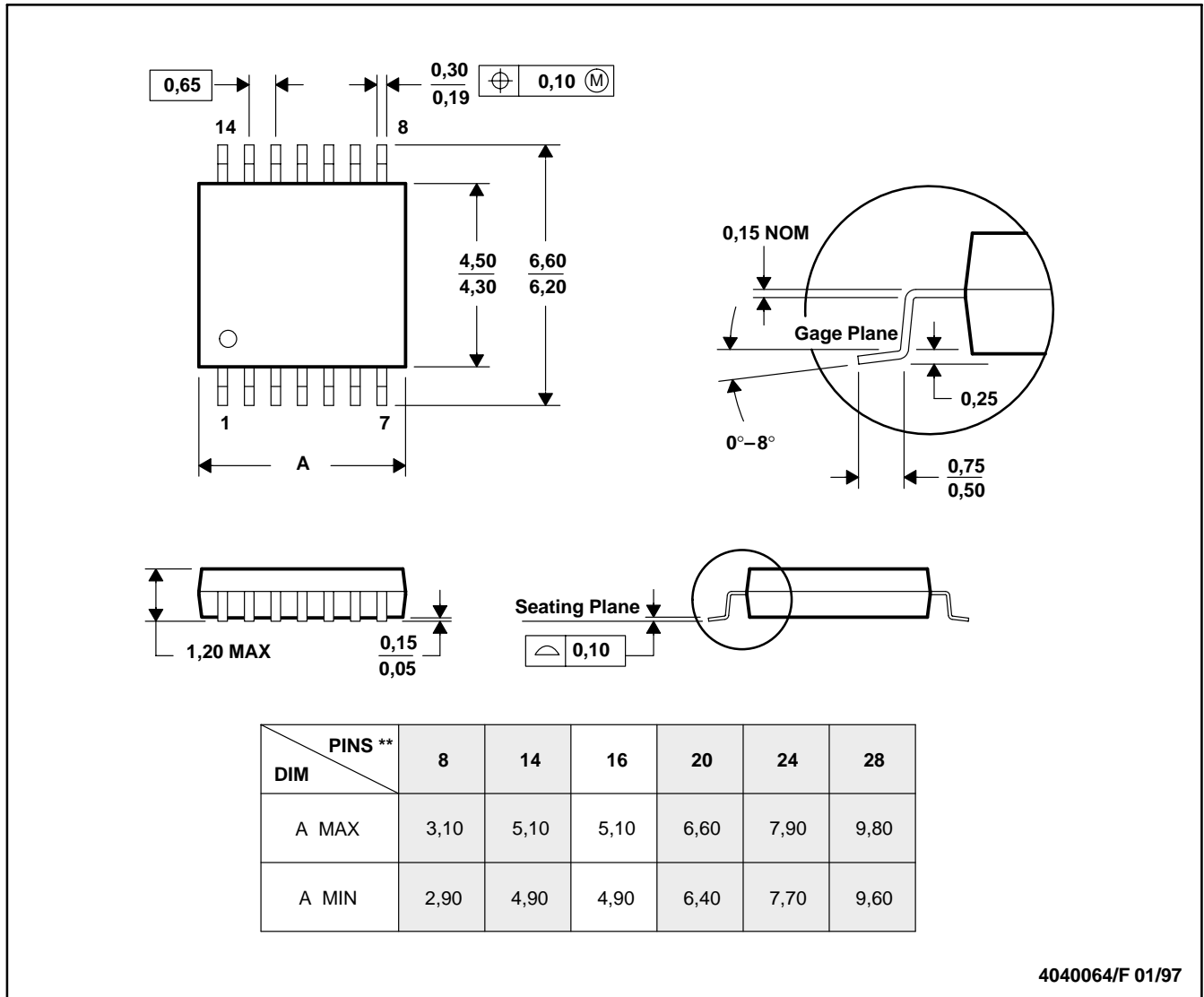
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## MECHANICAL DATA

**PW (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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