



## DIFFERENTIAL TRANSLATOR/REPEATER

### FEATURES

- Designed for Signaling Rates<sup>(1)</sup> ≥ 2 Gbps
- Total Jitter < 65 ps
- Low-Power Alternative for the MC100EP16
- Low 100 ps (Max) Part-To-Part Skew
- 25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range
- Inputs Electrically Compatible With LVPECL, CML, and LVDS Signal Levels
- 3.3-V Supply Operation
- LVDT Integrates 110-Ω Terminating Resistor
- Offered in SOIC and MSOP
- Chip Scale Package (Product Preview)

### APPLICATIONS

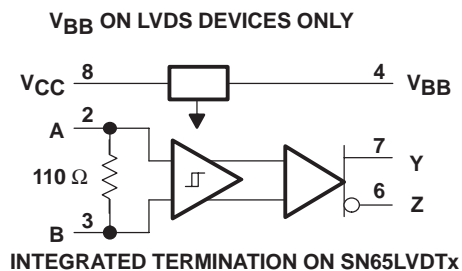
- 622 MHz Central Office Clock Distribution
- High-Speed Network Routing
- Wireless Basestations
- Low Jitter Clock Repeater
- Serdes LVPECL o/p to FPGA LVDS i/p Translator

### DESCRIPTION

These high-speed translators/repeaters were designed to address various high-speed network routing applications. Inputs accept LVDS, LVPECL, and CML levels. The SN65LVDSx100 provides LVDS outputs, while the SN65LVDSx101 supports LVPECL outputs. They are compatible with the TIA/EIA-644-A (LVDS) standard (exception; the LVPECL output). Utilization of the LVDS technology allows for low power and high-speed operation. Internal data paths from input to output are fully differential for lower noise generation and low pulse width distortion. The  $V_{BB}$  pin is an internally generated voltage supply to allow operation with single-ended (LVPECL) inputs. For those applications where board space is a premium, the LVDT devices have the integrated 110-Ω termination resistor. All devices are characterized for operation from -40°C to 85°C.

DEVICE	INPUT	OUTPUT
SN65LVDS100	LVDS or LVPECL or CML	LVDS
SN65LVDT100		
SN65LVDS101	LVDS or LVPECL or CML	LVPECL
SN65LVDT101		

### FUNCTIONAL DIAGRAM

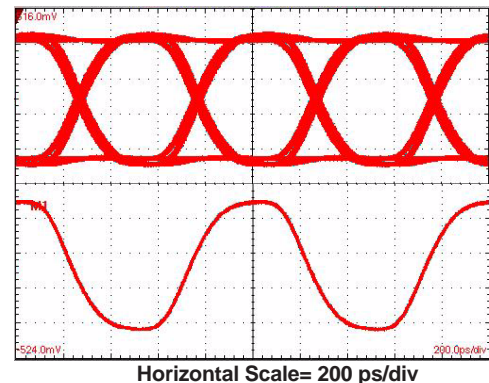


### EYE PATTERN

2 Gbps  
223 – 1 PRBS

$V_{CC} = 3.3\text{ V}$   
 $|V_{ID}| = 200\text{ mV}$ ,  $V_{IC} = 1.2\text{ V}$   
Vertical Scale= 200 mV/div

1 GHz



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

<sup>1</sup>The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

# SN65LVDS100, SN65LVDT100 SN65LVDS101, SN65LVDT101

SLLS516B – AUGUST 2002 – REVISED SEPTEMBER 2003



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION<sup>(1)</sup>

OUTPUT	TERMINATION RESISTOR	PART NUMBER	PART MARKING	PACKAGE	STATUS
LVDS	No	SN65LVDS100D	DL100	SOIC	Production
LVDS	No	SN65LVDS100DGK	AZK	MSOP	Production
LVDS	Yes	SN65LVDT100D	DE100	SOIC	Production
LVDS	Yes	SN65LVDT100DGK	AZL	MSOP	Production
LVPECL	No	SN65LVDS101D	DL101	SOIC	Production
LVPECL	No	SN65LVDS101DGK	AZM	MSOP	Production
LVPECL	Yes	SN65LVDT101D	DE101	SOIC	Production
LVPECL	Yes	SN65LVDT101DGK	BAF	MSOP	Production

Add the suffix R for taped and reeled carrier (i.e. SN65LVDS100DR).

<sup>(1)</sup> Chipscale packaging is under consideration for SN65LVDS100 and SN65LVDT100. Contact your local TI sales office for further information.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

		SN65LVDS100, SN65LVDT100 SN65LVDS101, SN65LVDT101	
Supply voltage range, <sup>(2)</sup> $V_{CC}$		-0.5 V to 4 V	
Sink/source, $I_{BB}$		$\pm 0.5$ mA	
Voltage range, (A, B, Y, Z)		0 V to 4.3 V	
Differential voltage, $ V_A - V_B $ (LVDT only)		1 V	
ESD	Human Body Model <sup>(3)</sup>	A, B, Y, Z, and GND	$\pm 5$ kV
		All pins	$\pm 2$ kV
	Charged-Device Model <sup>(4)</sup>	All pins	$\pm 1500$ V
Continuous power dissipation		See Dissipation Rating Table	
Storage temperature range, $T_{stg}$		-65°C to 150°C	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C	

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>(2)</sup> All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

<sup>(3)</sup> Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.

<sup>(4)</sup> Tested in accordance with JEDEC Standard 22, Test Method C101.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		3	3.3	3.6	V
Magnitude of differential input voltage $ V_{ID} $	LVDS	0.1		1	V
	LVDT	0.1		0.8	
Input voltage (any combination of common-mode or input signals)		0		4	V
$V_{BB}$ output current				400	$\mu$ A
Junction temperature				125	°C
Operating free-air temperature, $T_A$ <sup>(1)</sup>		-40		85	°C

<sup>(1)</sup> Maximum free-air temperature operation is allowed as long as device recommended junction temperature is not exceeded.

## PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR <sup>(1)</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
DGK	377 mW	3.8 mW/°C	151 mW
D	481 mW	4.8 mW/°C	192 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## SN65LVDX101 POWER DISSIPATION

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_D$ Device power dissipation	$V_{CC} = 3.3\text{ V}, T_A = 25^\circ\text{C}$		116		mW
	$V_{CC} = 3.6\text{ V}, T_A = 85^\circ\text{C}$			142	

## DEVICE CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
$I_{CC}$ Supply current	LVDS100		25	30	mA
	LVDS101 <sup>(1)</sup>		50	61	
$V_{BB}$ Switching reference voltage <sup>(2)</sup>		1890	1950	2010	mV

(1) Supply current specifications while fully loaded (two 50- $\Omega$  resistors to  $V_{TT}$ ).

(2)  $V_{BB}$  parameter varies 1:1 with  $V_{CC}$

## INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
$V_{IT+}$ Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV	
$V_{IT-}$ Negative-going differential input voltage threshold		-100				
$V_{ID(HYS)}$ Differential input voltage hysteresis, $V_{IT+} - V_{IT-}$			25		mV	
$I_I$ Input current (A or B inputs 'LVDS)	$V_I = 0\text{ V or } 2.4\text{ V}, \text{ Second input at } 1.2\text{ V}$	-20		20	$\mu\text{A}$	
	$V_I = 4\text{ V}, \text{ Second input at } 1.2\text{ V}$			33		
	Input current (A or B inputs 'LVDT)	$V_I = 0\text{ V or } 2.4\text{ V}, \text{ Other input open}$	-40		40	$\mu\text{A}$
		$V_I = 4\text{ V}, \text{ Other input open}$			66	
$I_{I(OFF)}$ Power off input current (A or B inputs 'LVDS)	$V_{CC} = 1.5\text{ V}, V_I = 0\text{ V or } 2.4\text{ V}, \text{ Second input at } 1.2\text{ V}$	-20		20	$\mu\text{A}$	
	$V_{CC} = 1.5\text{ V}, V_I = 4\text{ V}, \text{ Second input at } 1.2\text{ V}$			33		
	Power off input current (A or B inputs 'LVDT)	$V_{CC} = 1.5\text{ V}, V_I = 0\text{ V or } 2.4\text{ V}, \text{ Other input open}$	-40		40	$\mu\text{A}$
		$V_{CC} = 1.5\text{ V}, V_I = 2.4\text{ V or } 4\text{ V}, \text{ Other input open}$			66	
$I_{IO}$ Input offset current ( $ I_{IA} - I_{IB} $ ) ('LVDS)	$V_{IA} = V_{IB}, 0 \leq V_{IA} \leq 4\text{ V}$	-6		6	$\mu\text{A}$	
$R_{(T)}$ Termination resistance ('LVDT)	Termination resistance ('LVDT)	$V_{ID} = 300\text{ mV and } 500\text{ mV}, V_{IC} = 0\text{ to } 2.4\text{ V}$	90	110	132	$\Omega$
	Termination resistance ('LVDT with power-off)	$V_{ID} = 300\text{ mV and } 500\text{ mV}, V_{CC} = 1.5\text{ V}, V_{IC} = 0\text{ to } 2.4\text{ V}$	90	110	132	
$C_i$ Differential input capacitance			0.6		pF	

(1) All typical values are at 25°C and with a 3.3-V supply.

## OUTPUT ELECTRICAL CHARACTERISTICS FOR SN65LVDX100 WITH LVDS OUTPUTS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V <sub>OD</sub>	Differential output voltage magnitude	See Figure 2	247	340	454	mV
Δ V <sub>OD</sub>	Change in differential output voltage magnitude between logic states	See Figure 2	-50		50	
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
ΔV <sub>OC(SS)</sub>	Change in steady-state common-mode output voltage between logic states		-50		50	mV
V <sub>OC(PP)</sub>	Peak-to-peak common-mode output voltage			50	150	mV
I <sub>OS</sub>	Short-circuit output current	V <sub>O(Y)</sub> or V <sub>O(Z)</sub> = 0 V	-24		24	mA
I <sub>OS(D)</sub>	Differential short-circuit output current	V <sub>OD</sub> = 0 V	-12		12	mA
C <sub>O</sub>	Differential output capacitance			1.5		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

## OUTPUT ELECTRICAL CHARACTERISTICS FOR SN65LVDX101 WITH LVPECL OUTPUTS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V <sub>OH</sub>	Output high voltage <sup>(2)</sup>	See Figure 4	2055	2280	2405	mV
V <sub>OL</sub>	Output low voltage <sup>(2)</sup>		1475	1690	1775	mV
V <sub>OD</sub>	Differential output voltage magnitude		475	575	750	mV
C <sub>O</sub>	Differential output capacitance			0.8		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) Outputs are terminated through a 50-Ω resistor to V<sub>CC</sub> – 2 V; PECL level specifications are referenced to V<sub>CC</sub> and will track 1:1 with variation of V<sub>CC</sub>.

## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM(1)	MAX	UNIT	
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	LVDx100	See Figure 5	300	470	800	ps
		LVDx101		400	630	900	ps
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	LVDx100		300	470	800	ps
		LVDx101		400	630	900	ps
t <sub>r</sub>	Differential output signal rise time (20% – 80%)	See Figure 5			220	ps	
t <sub>f</sub>	Differential output signal fall time (20% – 80%)				220	ps	
t <sub>sk(p)</sub>	Pulse skew ( t <sub>PHL</sub> – t <sub>PLH</sub>  ) <sup>(2)</sup>			5	50	ps	
t <sub>sk(pp)</sub>	Part-to-part skew <sup>(3)</sup>	V <sub>ID</sub> = 0.2 V			100	ps	
t <sub>jit(per)</sub>	Period jitter, rms (1 standard deviation) <sup>(4)</sup>	1 GHz clock input <sup>(5)</sup> , See Figure 6		1	3.7	ps	
t <sub>jit(cc)</sub>	Cycle-to-cycle jitter (peak) <sup>(4)</sup>	1 GHz clock input <sup>(6)</sup> , See Figure 6		6	23	ps	
t <sub>jit(pp)</sub>	Peak-to-peak jitter <sup>(4)</sup>	2 Gbps 2 <sup>23</sup> -1 PRBS input <sup>(7)</sup> , See Figure 6		28	65	ps	
t <sub>jit(det)</sub>	Deterministic jitter, peak-to-peak <sup>(4)</sup>	2 Gbps 2 <sup>7</sup> -1 PRBS input <sup>(8)</sup> , See Figure 6		17	48	ps	

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) t<sub>sk(p)</sub> is the magnitude of the time difference between the t<sub>PLH</sub> and t<sub>PHL</sub> of any output of a single device.

(3) t<sub>sk(pp)</sub> is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(4) Jitter specifications are based on design and characterization. Stimulus system jitter of 2.3 ps t<sub>jit(per)</sub>, 8.5 ps t<sub>jit(cc)</sub>, 15.1 ps t<sub>jit(pp)</sub>, and 9.7 ps t<sub>jit(det)</sub> have been subtracted from the values.

(5) Input voltage = V<sub>ID</sub> = 200 mV, 50% duty cycle at 1 GHz, t<sub>r</sub> = t<sub>f</sub> = 50 ps (20% to 80%), measured over 1000 samples.

(6) Input voltage = V<sub>ID</sub> = 200 mV, 50% duty cycle at 1 GHz, t<sub>r</sub> = t<sub>f</sub> = 50 ps (20% to 80%).

(7) Input voltage = V<sub>ID</sub> = 200 mV, 2<sup>23</sup>-1 PRBS pattern at 2 Gbps, t<sub>r</sub> = t<sub>f</sub> = 50 ps (20% to 80%), measured over 200k samples.

(8) Input voltage = V<sub>ID</sub> = 200 mV, 2<sup>7</sup>-1 PRBS pattern at 2 Gbps, t<sub>r</sub> = t<sub>f</sub> = 50 ps (20% to 80%).

PARAMETER MEASUREMENT INFORMATION

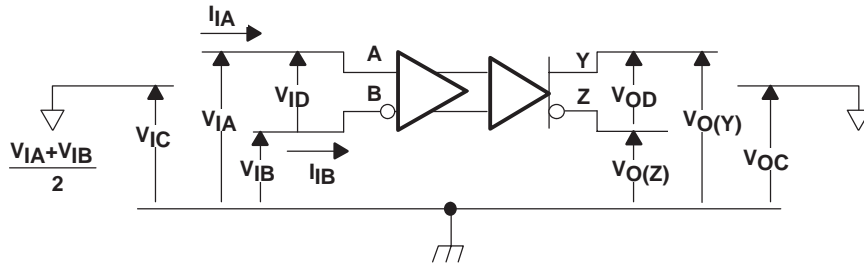


Figure 1. Voltage and Current Definitions

Table 1. Receiver Input Voltage Threshold Test

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT
V <sub>IA</sub>	V <sub>IB</sub>	V <sub>ID</sub>	V <sub>IC</sub>	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	-100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4.0 V	-100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	H
0.0 V	0.1 V	-100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	-1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	-1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	-1000 mV	0.5 V	L

H = high level, L = low level

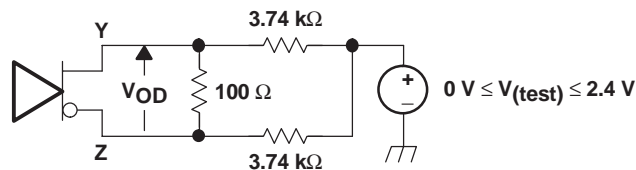
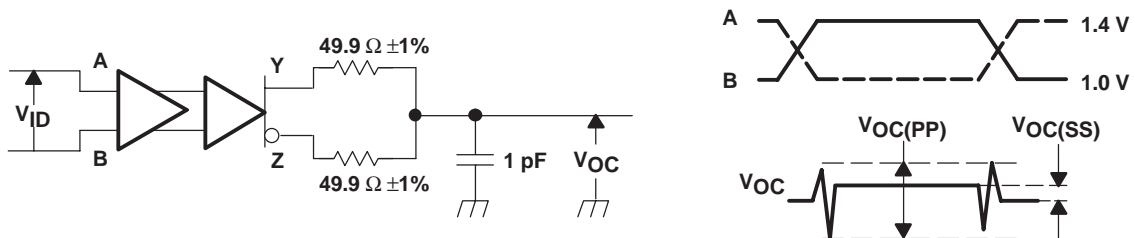


Figure 2. Differential Output Voltage (V<sub>OD</sub>) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 0.25$  ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width =  $500 \pm 10$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of  $V_{OC(PP)}$  is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

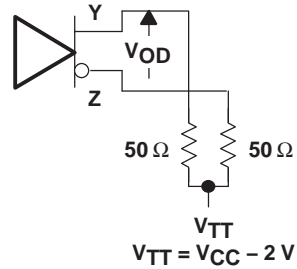
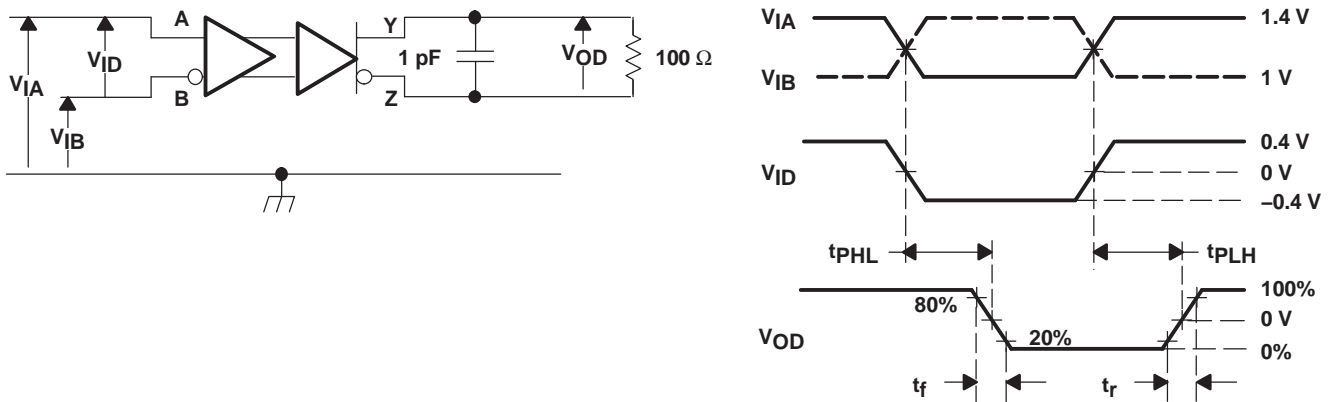
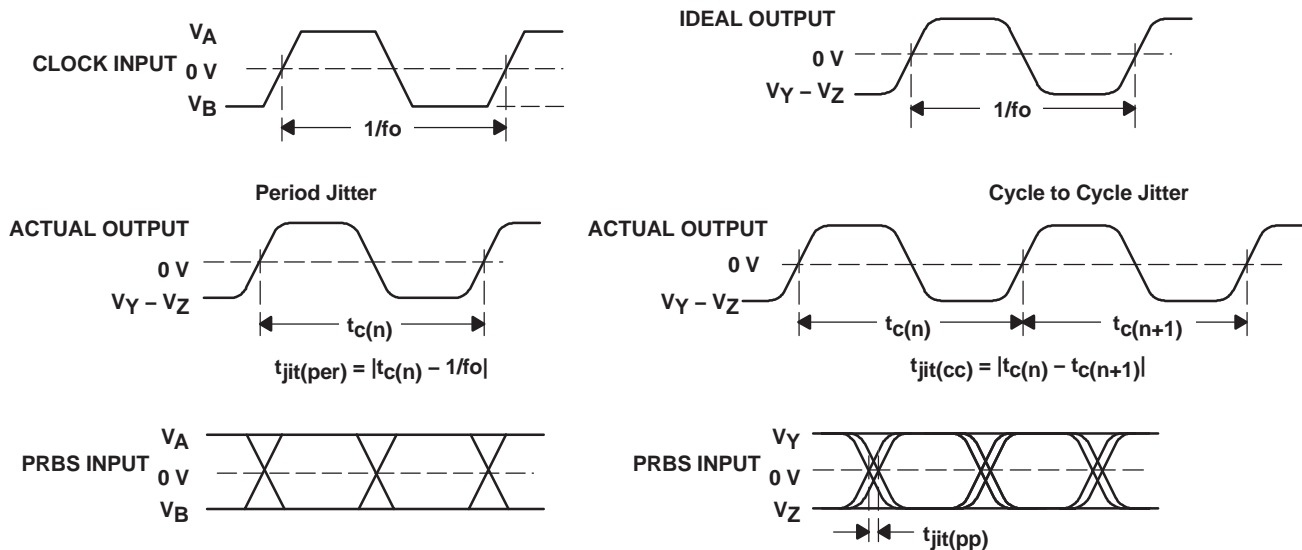


Figure 4. Typical Termination for LVPECL Output Driver (65LVDx101)



NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 0.25$  ns, pulse repetition rate (PRR) = 50 Mpps, pulse width =  $10 \pm 0.2$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. Measurement equipment provides a bandwidth of 5 GHz minimum.

Figure 5. Timing Test Circuit and Waveforms

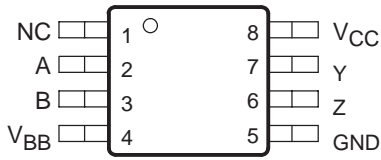


NOTES: A. All input pulses are supplied by a Agilent 81250 Stimulus System.  
B. The measurement is made on a TEK TDS6604 running TDFSJIT3 application software.

Figure 6. Driver Jitter Measurement Waveforms

**PIN ASSIGNMENTS**

**D AND DGK PACKAGE  
(TOP VIEW)**



V<sub>BB</sub> on 'LVDS devices only

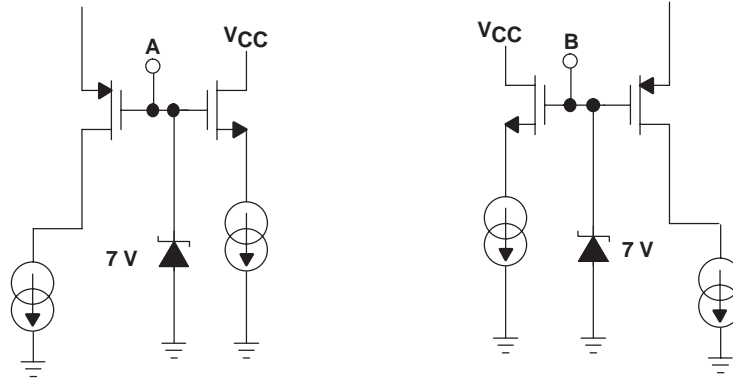
**FUNCTION TABLE**

DIFFERENTIAL INPUT	OUTPUTS	
	Y	Z
$V_{ID} = V_A - V_B$	Y	Z
$V_{ID} \geq 100 \text{ mV}$	H	L
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	?	?
$V_{ID} \leq -100 \text{ mV}$	L	H
Open	?	?

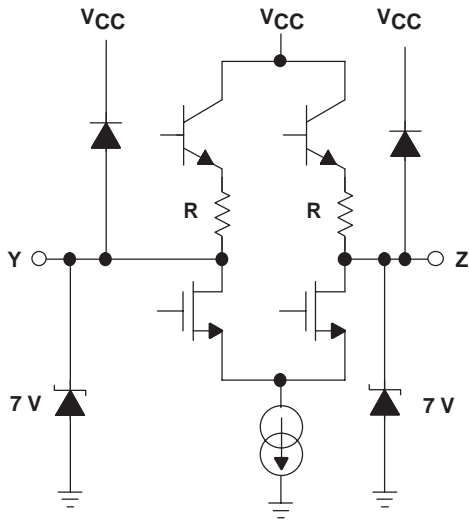
H = high level, L = low level, ? = intermediate

**EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS**

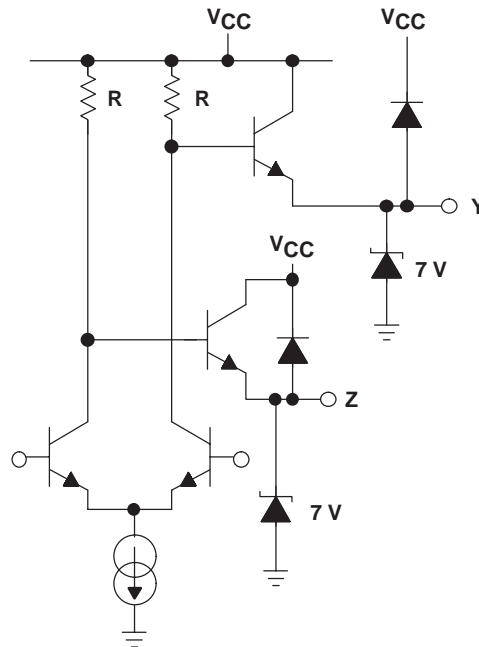
**INPUT LVDS100/101**



**OUTPUT LVDS100**



**OUTPUT LVDS101**



TYPICAL CHARACTERISTICS

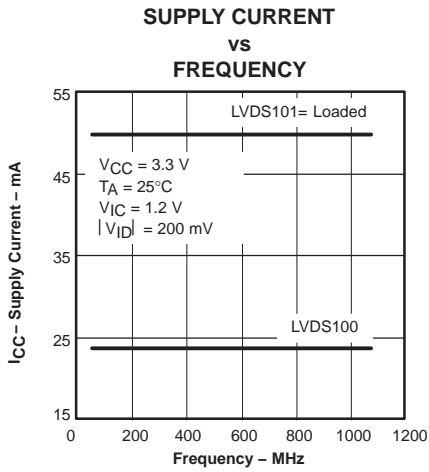


Figure 7

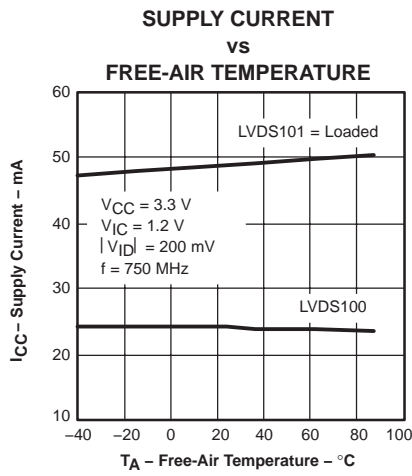


Figure 8

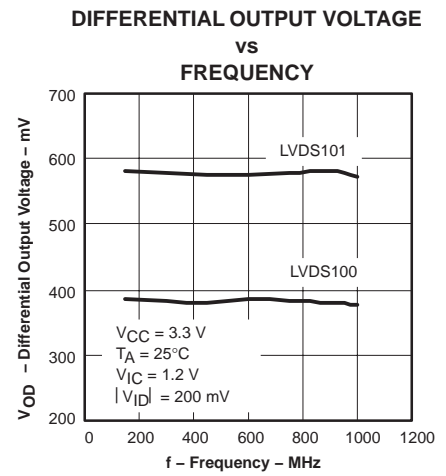


Figure 9

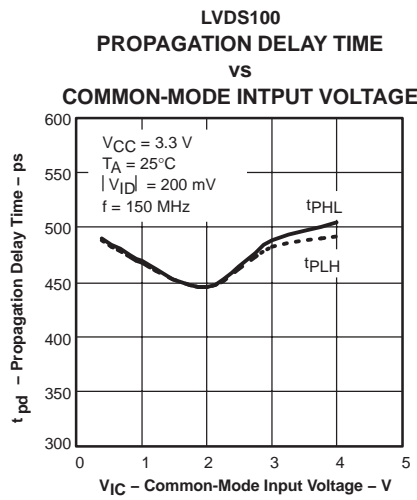


Figure 10

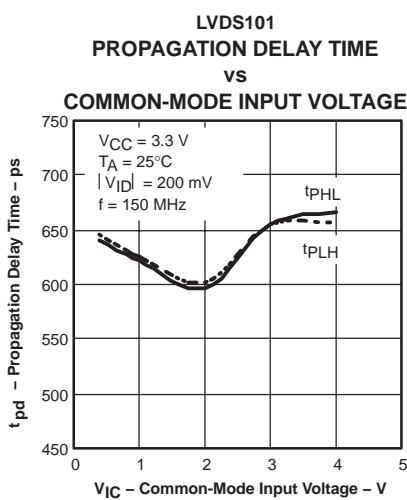


Figure 11

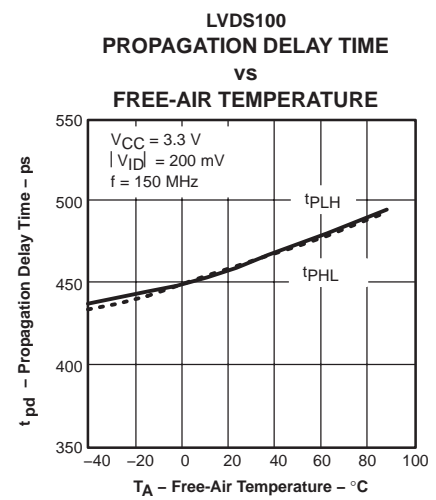


Figure 12

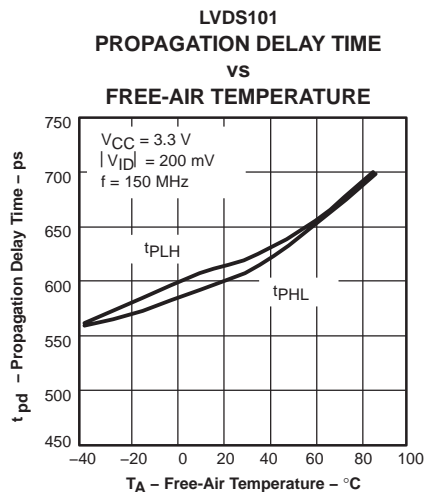


Figure 13

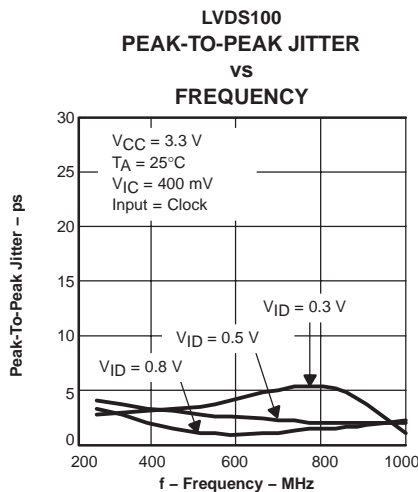


Figure 14

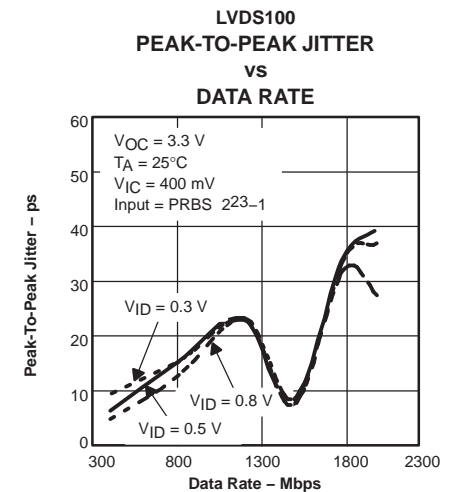


Figure 15



TYPICAL CHARACTERISTICS

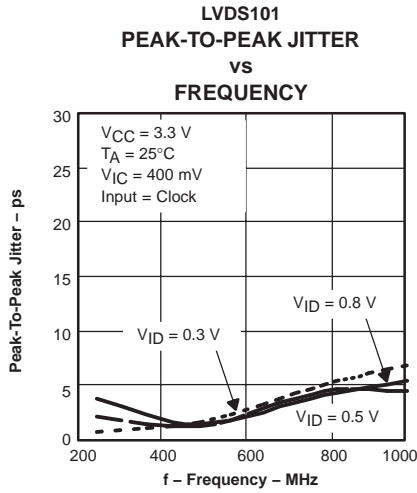


Figure 16

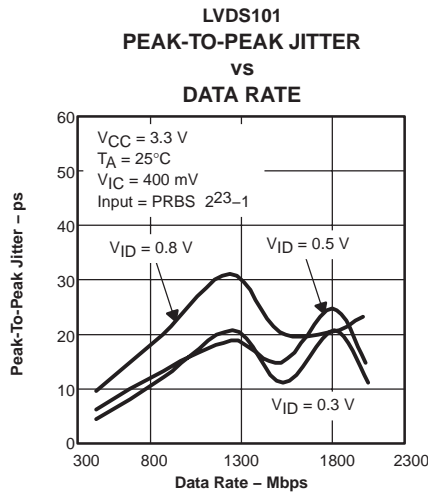


Figure 17

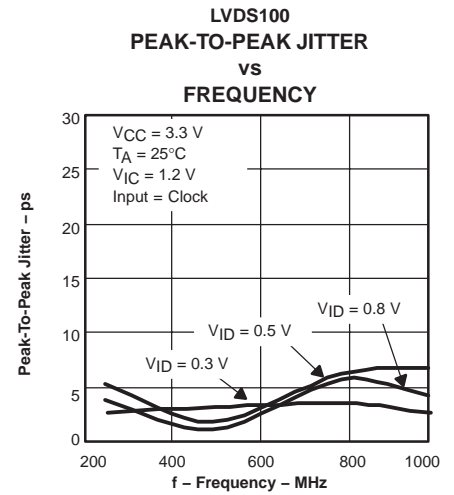


Figure 18

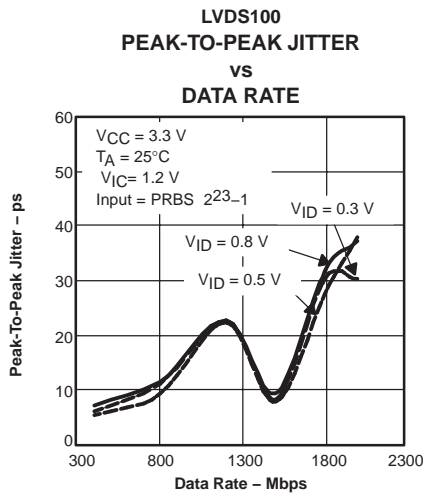


Figure 19

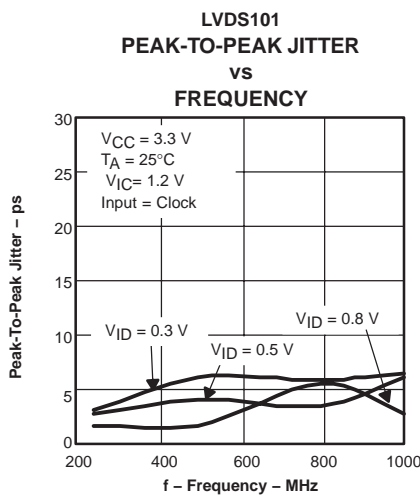


Figure 20

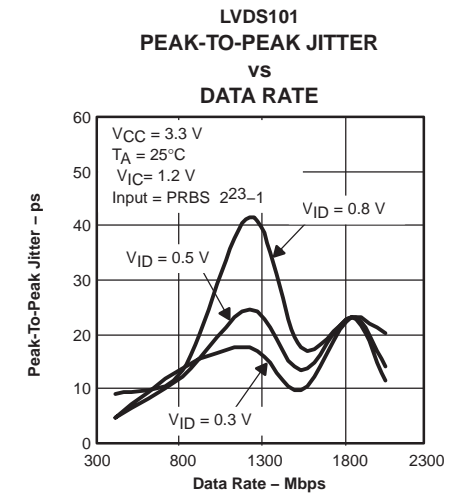


Figure 21

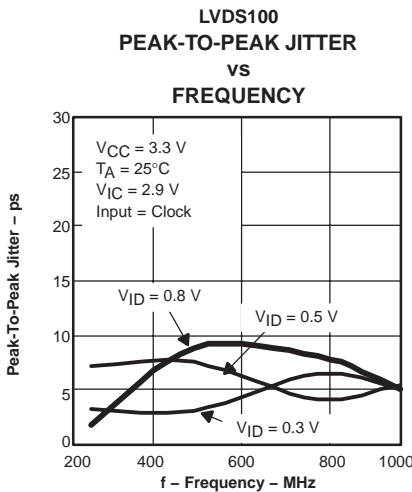


Figure 22

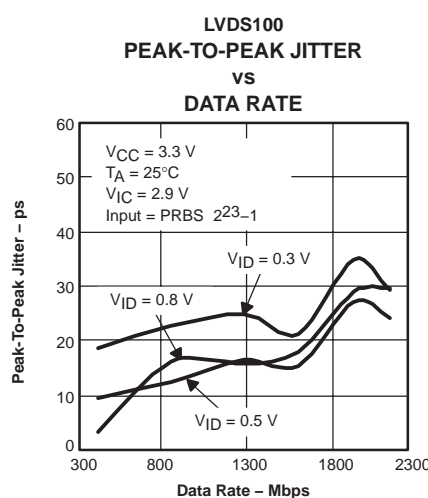


Figure 23

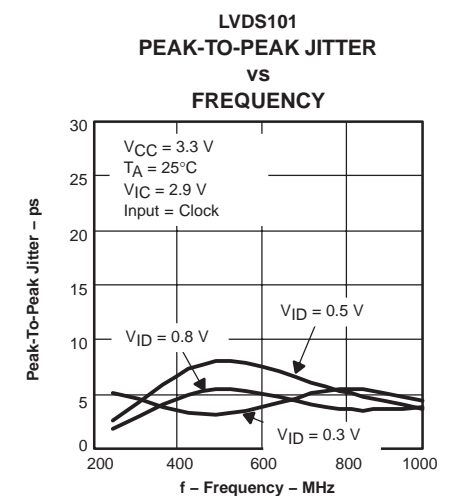
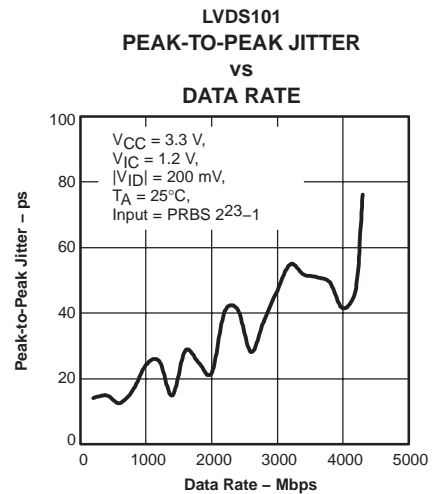
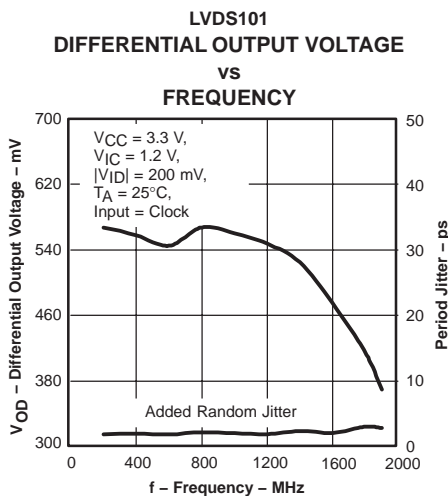
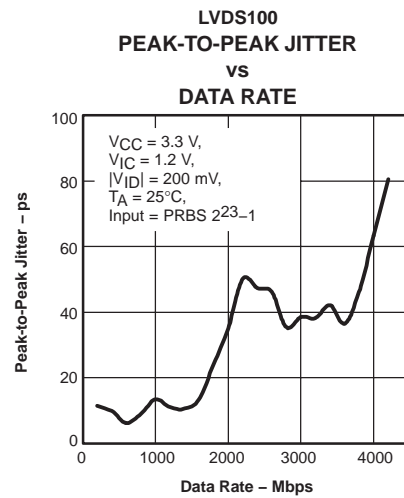
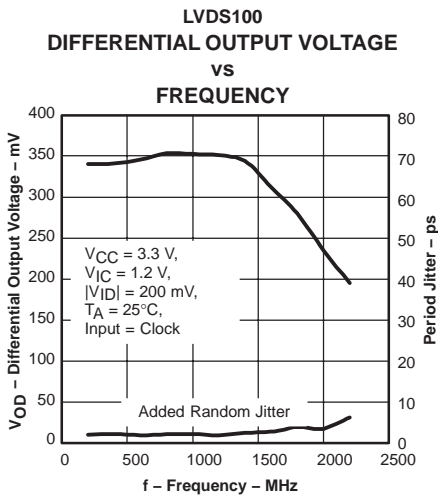
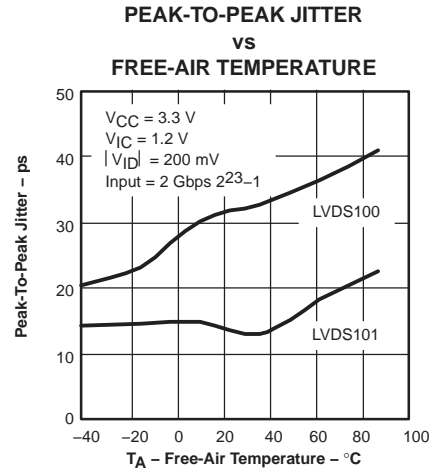
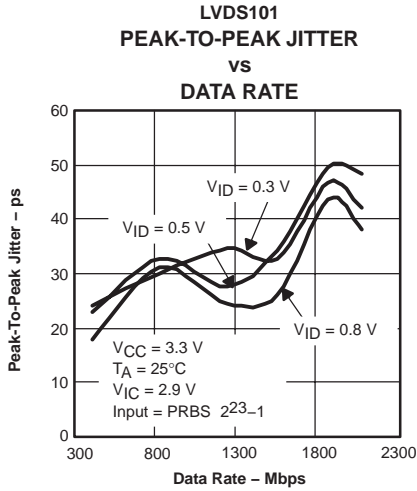
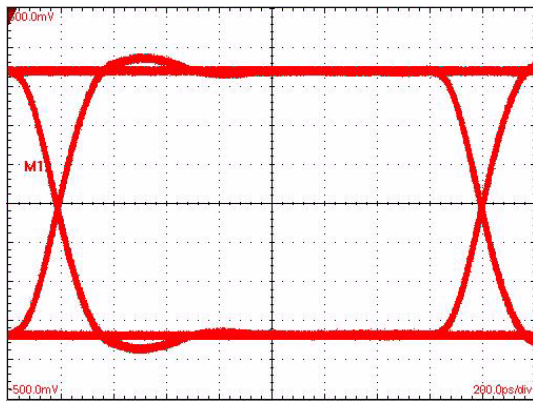


Figure 24

TYPICAL CHARACTERISTICS



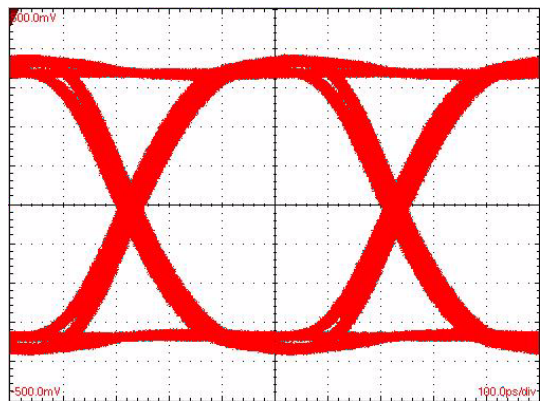
LVDS100  
622 Mbps,  $2^{23} - 1$  PRBS



Horizontal Scale= 200 ps/div  
LVPECL-to-LVDS

Figure 31

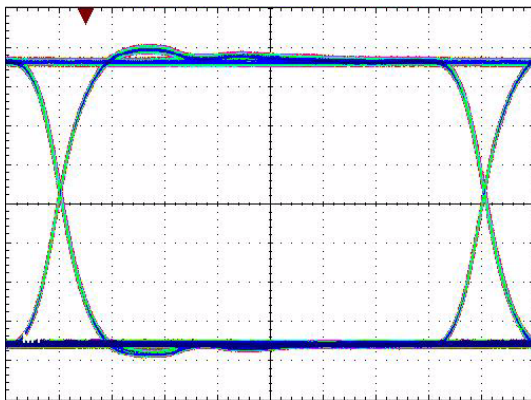
LVDS100  
2 Gbps,  $2^{23} - 1$  PRBS



Horizontal Scale= 100 ps/div  
LVPECL-to-LVDS

Figure 32

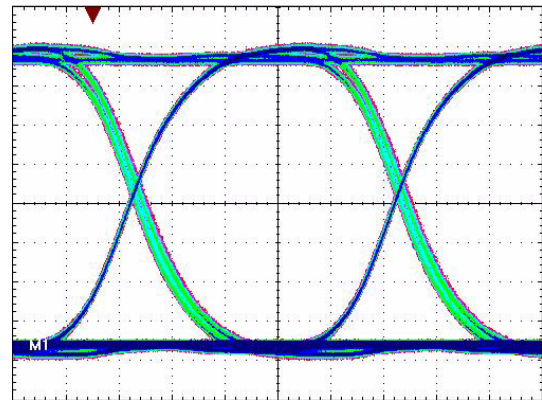
LVDS101  
622 Mbps,  $2^{23} - 1$  PRBS



Horizontal Scale= 200 ps/div  
LVDS-to-LVPECL

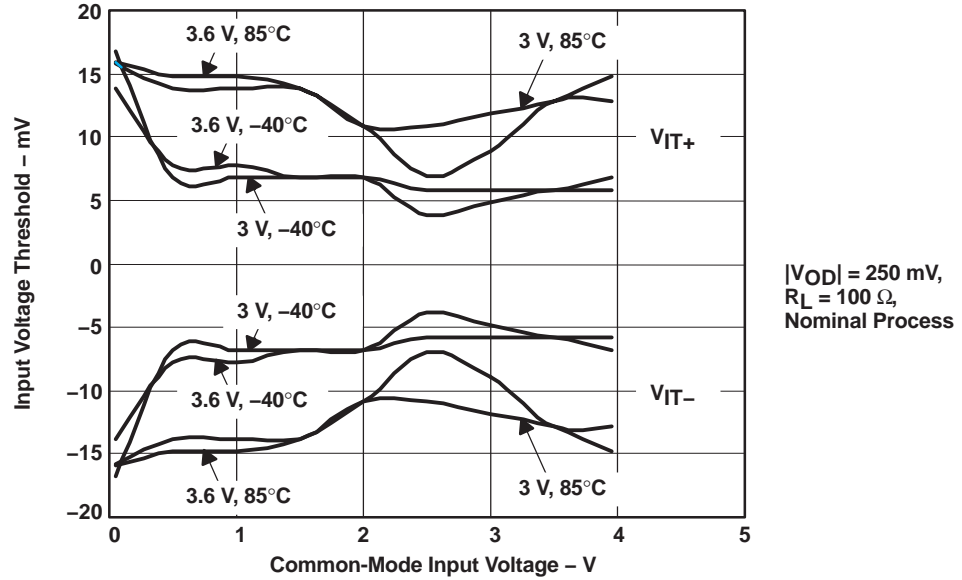
Figure 33

LVDS101  
2 Gbps,  $2^{23} - 1$  PRBS



Horizontal Scale= 100 ps/div  
LVDS-to-LVPECL

Figure 34



NOTE:  $V_{IL}$  is a steady-state parameter. The switching time is influenced by the input overdrive above this steady-state threshold up to a differential input voltage magnitude of 100 mV.

Figure 35. SN65LVDS100 Simulated Input Voltage Threshold vs Common-Mode Input Voltage, Supply Voltage, and Temperature

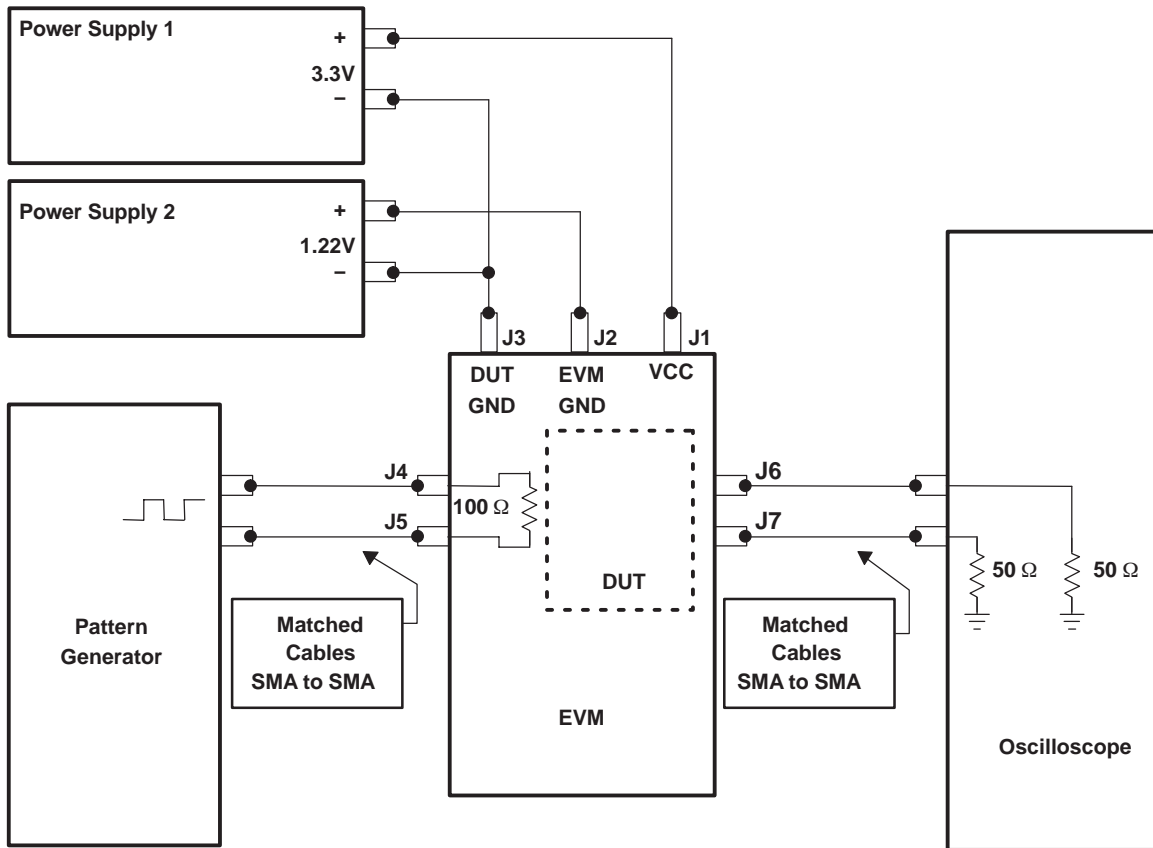


Figure 36. Jitter Setup Connections for SN65LVDS100 and SN65LVDS101

## APPLICATION INFORMATION

For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage. When  $V_{BB}$  is used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01- $\mu\text{F}$  capacitor and limit the current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

### TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, ETC.)

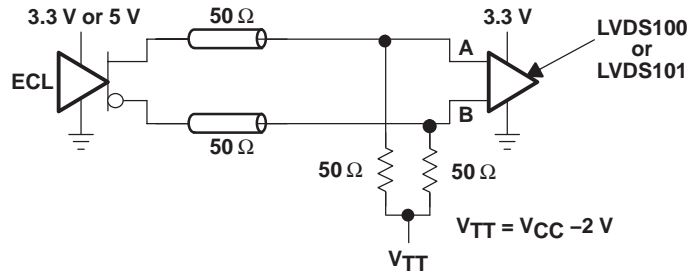


Figure 37. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

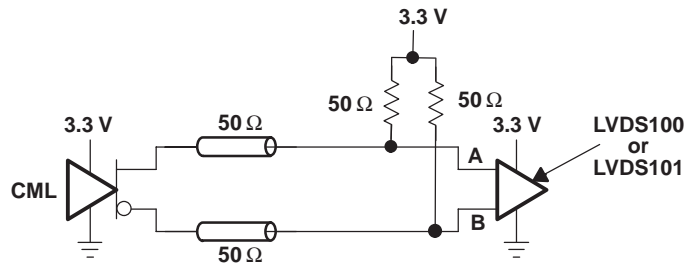


Figure 38. Current-Mode Logic (CML)

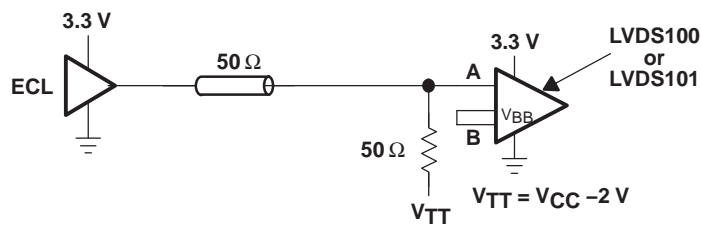


Figure 39. Single-Ended (LVPECL)

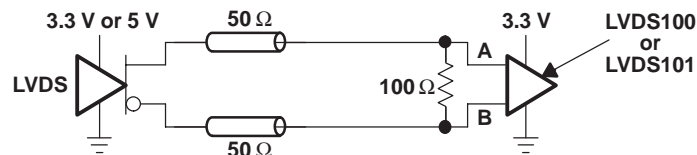


Figure 40. Low-Voltage Differential Signaling (LVDS)

## FAILSAFE CONSIDERATIONS

Failsafe, in regard to a line receiver, usually means that the output goes to a defined logical state with no input signal. To keep added jitter to an absolute minimum, the SN65LVDS100 does not include this feature. It does exhibit 25 mV of input voltage hysteresis to prevent oscillation and keep the output in the last state prior to input-signal loss (assuming the differential noise in the system is less than the hysteresis).

Should failsafe be required, it may be added externally with a 1.6-k $\Omega$  pull-up resistor to the 3.3-V supply and a 1.6-k $\Omega$  pull-down resistor to ground as shown in Figure 41. The default output state is determined by which line is pulled up or down and is the user's choice. The location of the 1.6-k $\Omega$  resistors is not critical. However the 100- $\Omega$  resistor should be located at the end of the transmission line.

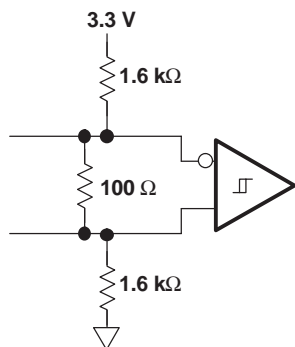


Figure 41. External Failsafe Circuit

Addition of this external failsafe will reduce the differential noise margin and add jitter to the output signal. The roughly 100-mV steady-state voltage generated across the 100- $\Omega$  resistor adds (or subtracts) from the signal generated by the upstream line driver. If the line driver's differential output is symmetrical about zero volts, then the input at the receiver will appear asymmetrical with the external failsafe. Perhaps more important, is the extra time it takes for the input signal to overcome the added failsafe offset voltage.

In Figure 42 and using an external failsafe, the high-level differential voltage at the input of the SN65LVDS100 reaches 340 mV and the low-level -400 mV indicating a 60-mV differential offset induced by the external failsafe circuitry. The figure also reveals that the lowest peak-to-peak time jitter does not occur at zero-volt differential (the nominal input threshold of the receiver) but at -60 mV, the failsafe offset.

The added jitter from external failsafe increases as the signal transition times are slowed by cable effects. When a ten-meter CAT-5 UTP cable is introduced between the driver and receiver, the zero-crossing peak-to-peak jitter at the receiver output adds 250 ps when the external failsafe is added with this specific test set up. If external failsafe is used in conjunction with the SN65LVDS100, the noise margin and jitter effects should be budgeted.

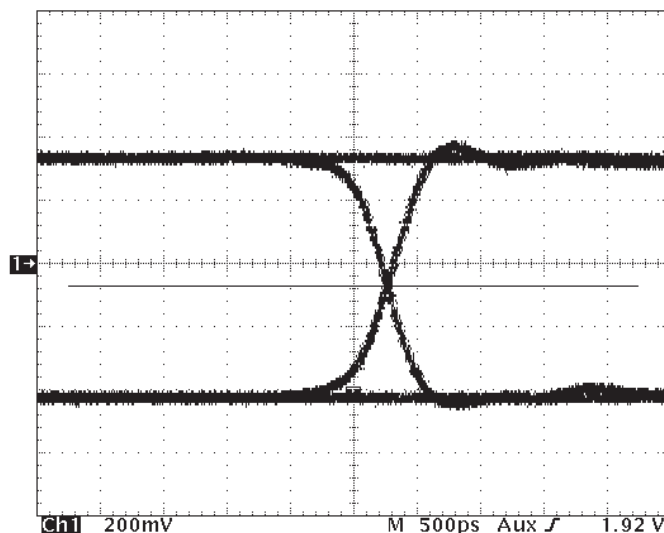
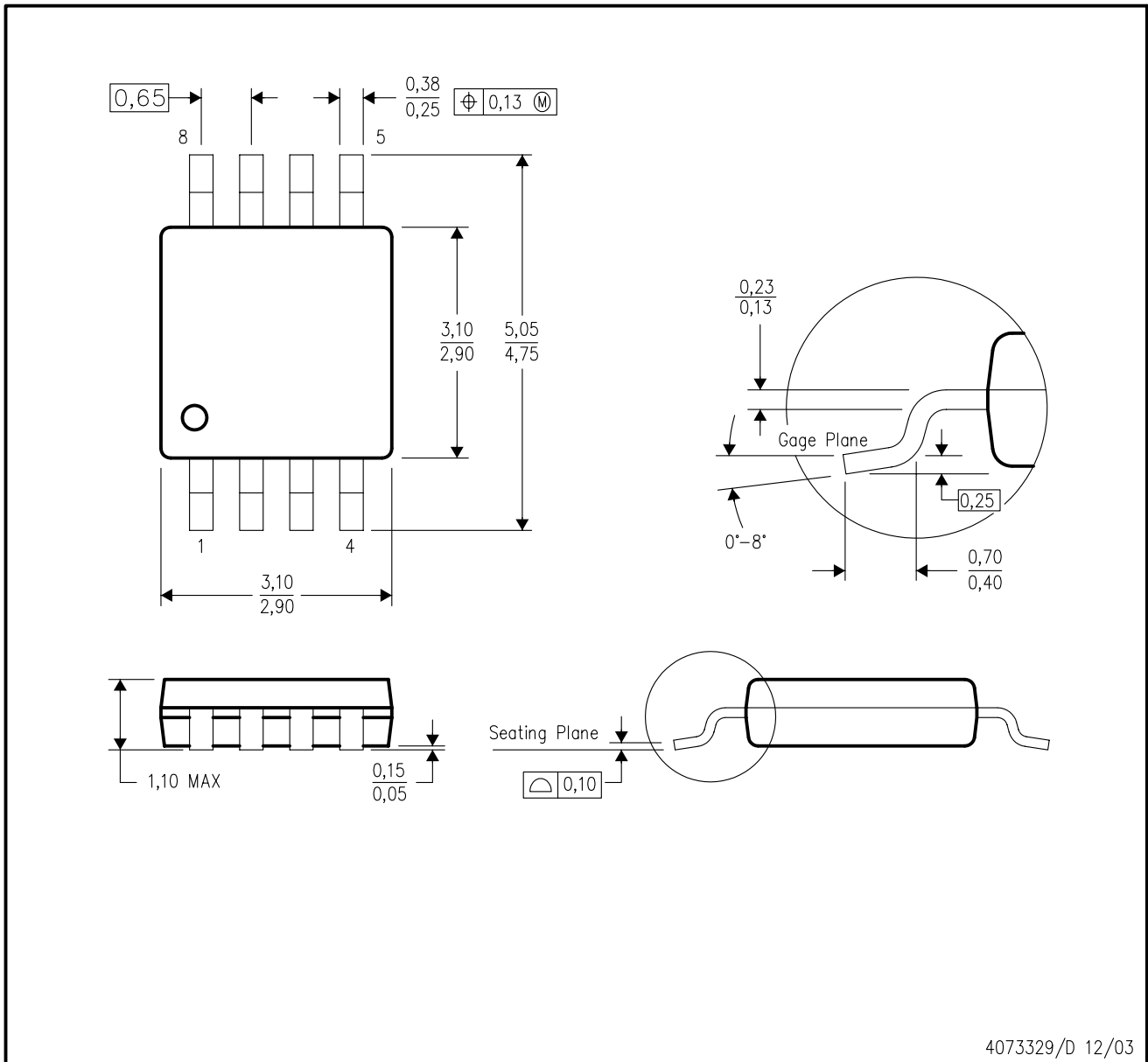


Figure 42. Receiver Input Eye Pattern With External Failsafe

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-187 variation AA.

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated