The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

SN54125, SN54126, SN54LS125A, SN54LS126A, SN74125, SN74126, SN74LS125A, SN74LS126A
QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

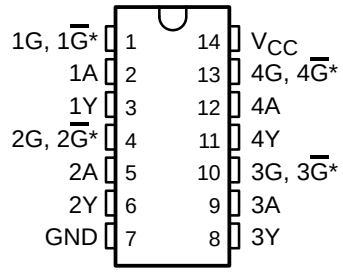
SDLS044A – DECEMBER 1983 – REVISED MARCH 2002

- **Quad Bus Buffers**
- **3-State Outputs**
- **Separate Control for Each Channel**

description

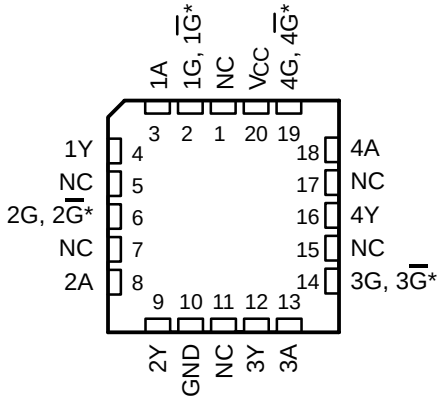
These bus buffers feature three-state outputs that, when enabled, have the low impedance characteristics of a TTL output with additional drive capability at high logic levels to permit driving heavily loaded bus lines without external pullup resistors. When disabled, both output transistors are turned off, presenting a high-impedance state to the bus so the output will act neither as a significant load nor as a driver. The ’125 and ’LS125A devices’ outputs are disabled when $\overline{G}$ is high. The ’126 and ’LS126A devices’ outputs are disabled when G is low.

SN54125, SN54126, SN54LS125A, SN54LS126A . . . J OR W PACKAGE
SN74125, SN74126 . . . N PACKAGE
SN74LS125A, SN74LS126A . . . D, N, OR NS PACKAGE
(TOP VIEW)



*$\overline{G}$ on ’125 and ’LS125A devices;
G on 126 and ’LS126A devices

SN54LS125A, SN54LS126A . . . FK PACKAGE
(TOP VIEW)



*$\overline{G}$ on ’125 and ’LS125A devices;
G on 126 and ’LS126A devices
NC – No internal connection

The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

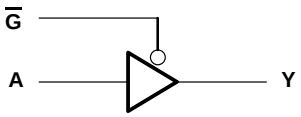
ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS125AN	SN74LS125AN
		Tube	SN74LS126AN	SN74LS126AN
	SOIC – D	Tube	SN74LS125AD	LS125A
		Tape and reel	SN74LS125ADR	
		Tube	SN74LS126AD	LS126A
		Tape and reel	SN74LS126ADR	
	SOP – NS	Tape and reel	SN74LS125ANSR	74LS125A
		Tape and reel	SN74LS126ANSR	74LS126A
–55°C to 125°C	CDIP – J	Tube	SN54LS125AJ	SN54LS125AJ
		Tube	SNJ54LS125AJ	SNJ54LS125AJ
	CFP – W	Tube	SNJ54LS125AW	SNJ54LS125AW
	LCCC – FK	Tube	SNJ54LS125AFK	SNJ54LS125AFK

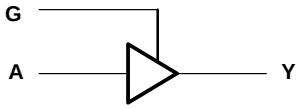
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

logic diagram (each gate)

’125, ’LS125A

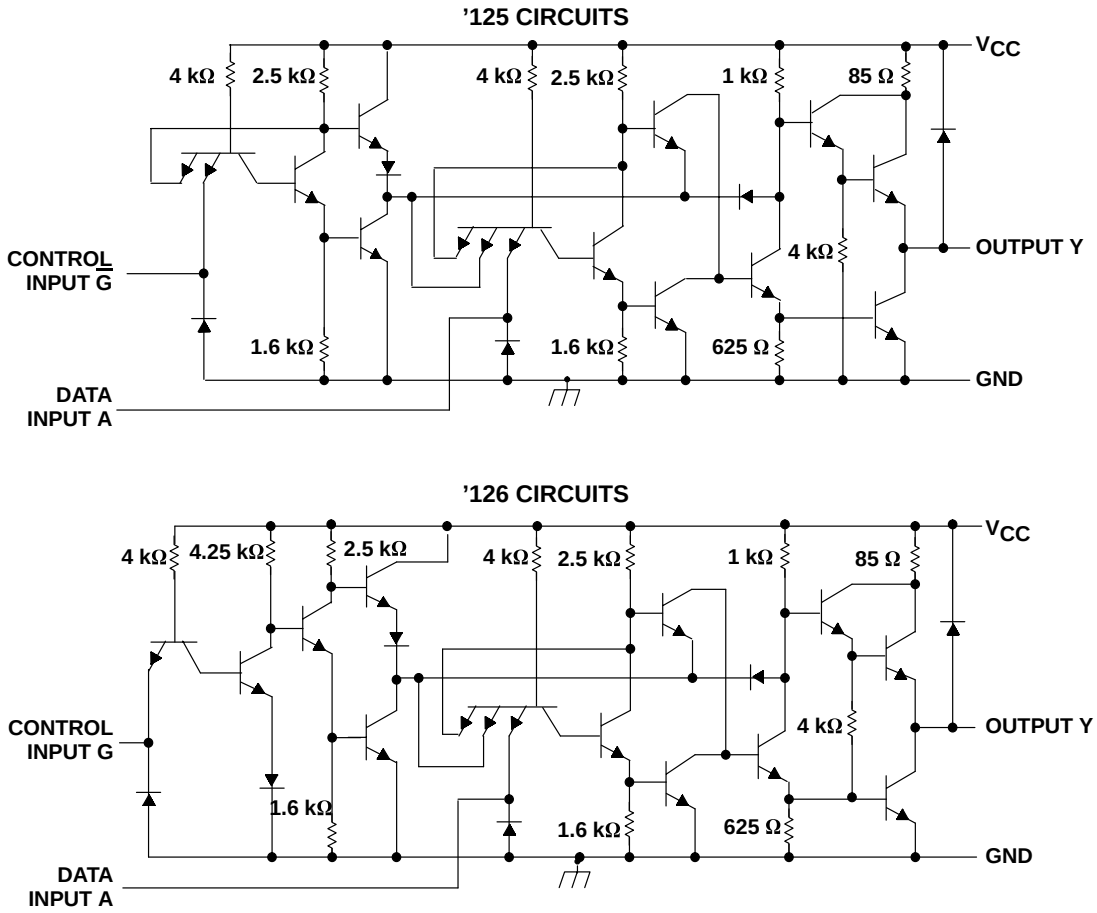


’126, ’LS126A



Y = A

schematics (each gate)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)† ('125 and '126)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Package thermal impedance, θ_{JA} (see Note 2): N package . . . . . 80°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

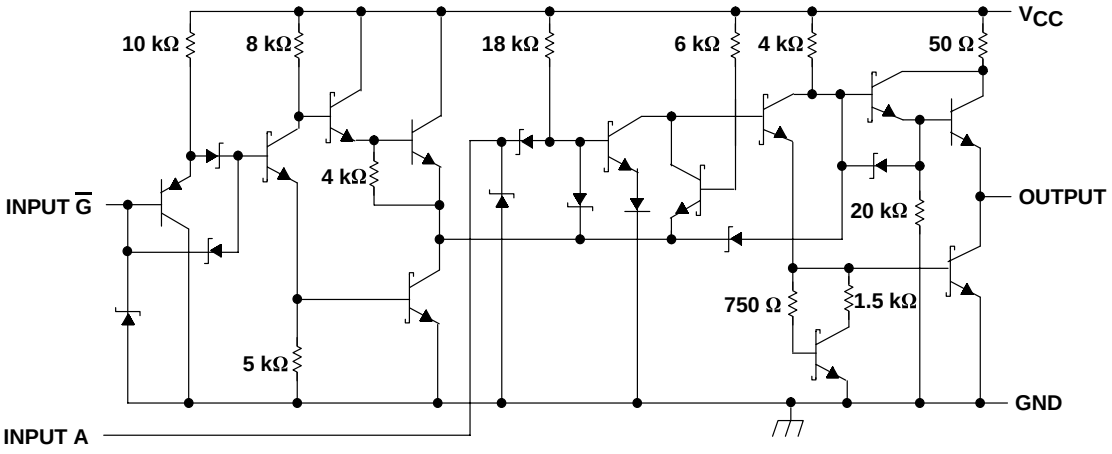
† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package termal impedance is calculated in accordance with JESD 51-7.

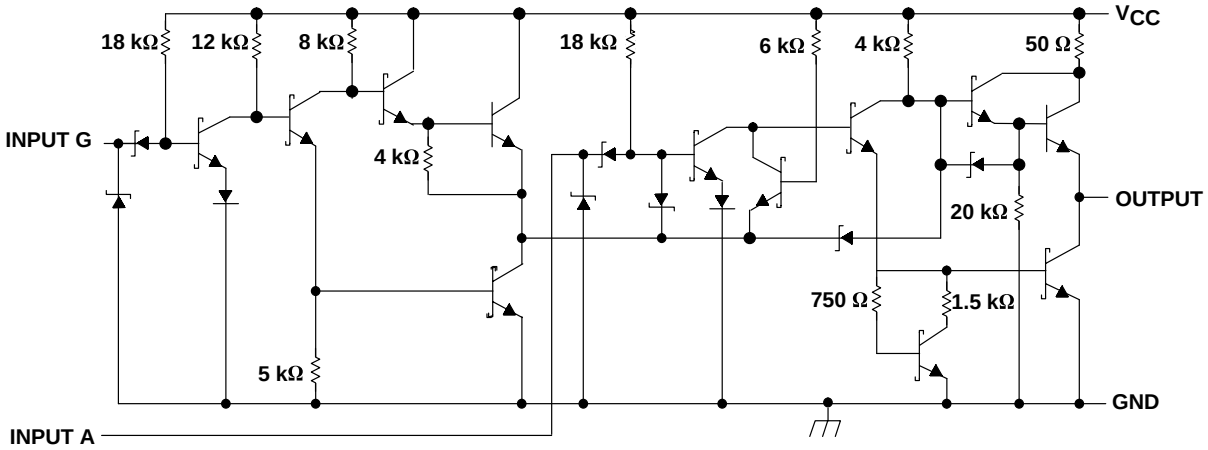
The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

schematics (each gate)

'LS125A CIRCUITS



'LS126A CIRCUITS



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)† ('LS125A and 'LS126A)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package termal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54125 SN54126			SN74125 SN74126			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–2			–5.2	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54125 SN54126			SN74125 SN74126			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = –12 mA				–1.5			–1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = –2 mA	2.4	3.3					V
		I_{OH} = –5.2 mA				2.4	3.1		
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4			0.4	V
I_{OZ}	V_{CC} = MAX V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			40			40	µA
		V_O = 0.4 V			–40			–40	
I_I	V_{CC} = MAX, V_I = 6.5 V				1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V				40			40	µA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V				–1.6			–1.6	mA
I_{OS}§	V_{CC} = MAX		–30		–70	–28		–70	mA
I_{CC}	V_{CC} = MAX (see Note 3)	’125		32	54		32	54	mA
		’126		36	62		36	62	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 3: Data inputs = 0 V; output control = 4.5 V for ’125 and 0 V for ’126.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	TEST CONDITIONS		SN54125 SN74125			SN54126 SN74126			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	R_L = 400 Ω,	C_L = 50 pF		8	13		8	13	ns
t_{PHL}				12	18		12	18	
t_{PZH}	R_L = 400 Ω,	C_L = 50 pF		11	17		11	18	ns
t_{PZL}				16	25		16	25	
t_{PHZ}	R_L = 400 Ω,	C_L = 5 pF		5	8		10	16	ns
t_{PLZ}				7	12		12	18	

The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

recommended operating conditions

		SN54LS125A SN54LS126A			SN74LS125A SN74LS126A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–1			–2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

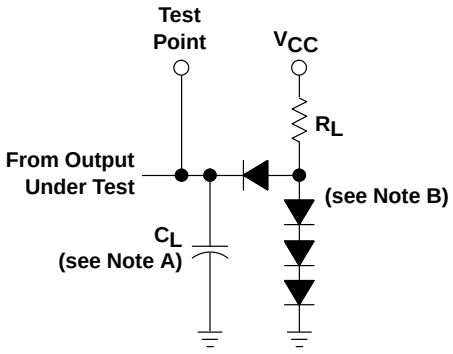
PARAMETER	TEST CONDITIONS†			SN54LS125A SN54LS126A			SN74LS125A SN74LS126A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = –18 mA				–1.5			–1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V	V_{IL} = 0.7 V,	I_{OH} = –1 mA	2.4						V
		V_{IL} = 0.8 V	I_{OH} = –2.6 mA				2.4			
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V	V_{IL} = 0.7 V,	I_{OL} = 12 mA		0.25	0.4				V
		V_{IL} = 0.8 V,	I_{OL} = 12 mA					0.25	0.4	
		V_{IL} = 0.8 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZ}	V_{CC} = MAX, V_{IH} = 2 V,	V_{IL} = 0.7 V	V_O = 2.4 V			20				μA
			V_O = 0.4 V			–20				
		V_{IL} = 0.8 V	V_O = 2.4 V						20	
			V_O = 0.4 V						–20	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V	’LS125A-$\overline{G}$ inputs				–0.2			–0.2	mA
		’LS125A-A inputs; ’LS126A All inputs				–0.4			–0.4	mA
I_{OS}§	V_{CC} = MAX			–40		–225	–40		–225	mA
I_{CC}	V_{CC} = MAX (see Note 4)		’LS125A		11	20		11	20	mA
			’LS126A		12	22		12	22	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 4: Data inputs = 0 V; output control = 4.5 V for ’LS125A and 0 V for ’LS126A.

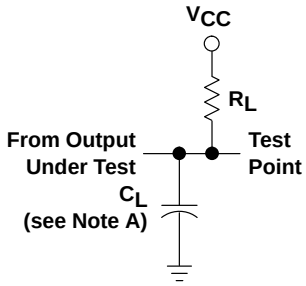
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	TEST CONDITIONS		SN54LS125A SN74LS125A			SN54LS126A SN74LS126A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	R_L = 667 Ω,	C_L = 45 pF		9	15		9	15	ns
t_{PHL}				7	18		8	18	
t_{PZH}	R_L = 667 Ω,	C_L = 45 pF		12	20		16	25	ns
t_{PZL}				15	25		21	35	
t_{PHZ}	R_L = 667 Ω,	C_L = 5 pF			20			25	ns
t_{PLZ}					20			25	

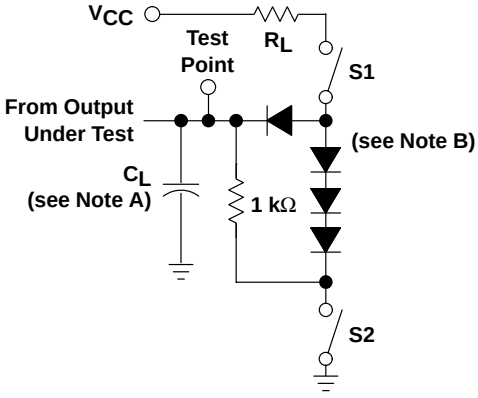
PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 DEVICES



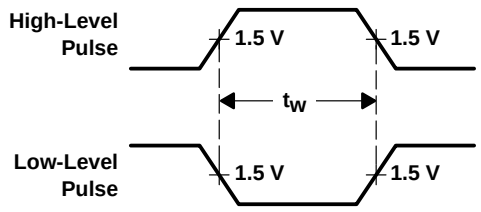
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



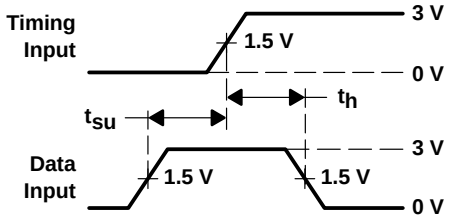
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



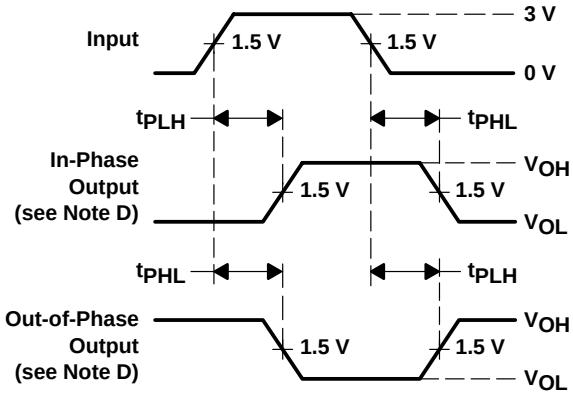
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



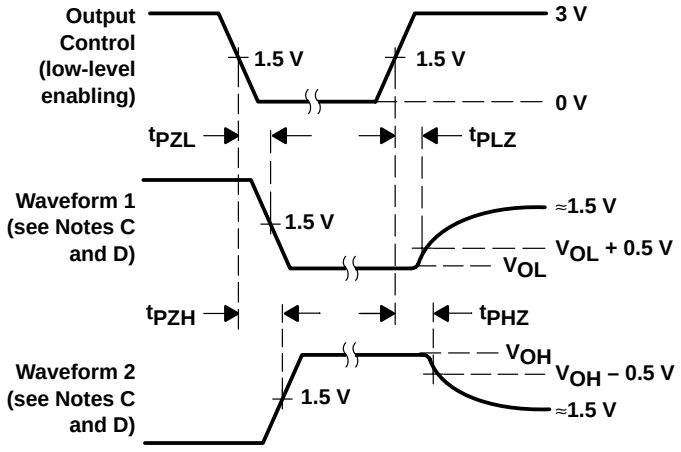
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



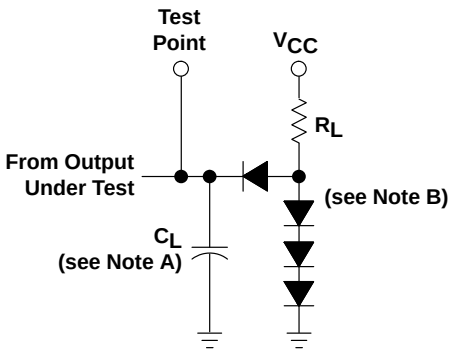
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω; t_r and t_f ≤ 7 ns for Series 54/74 devices and t_r and t_f ≤ 2.5 ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

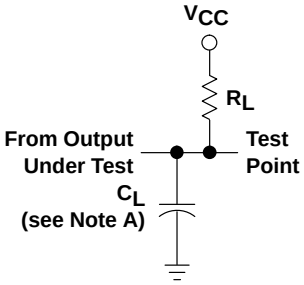
Figure 1. Load Circuits and Voltage Waveforms

The SN54125, SN54126, SN74125, SN74126, and SN54LS126A are obsolete and are no longer supplied.

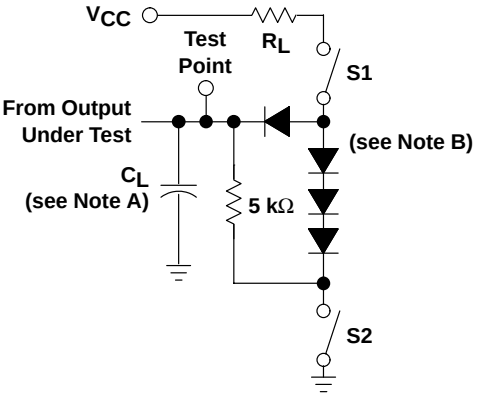
PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



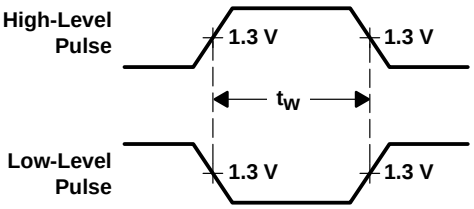
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



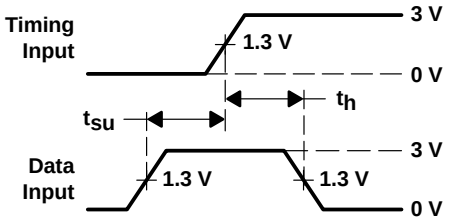
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



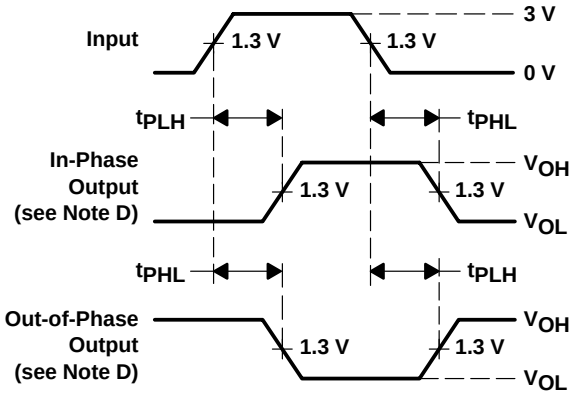
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



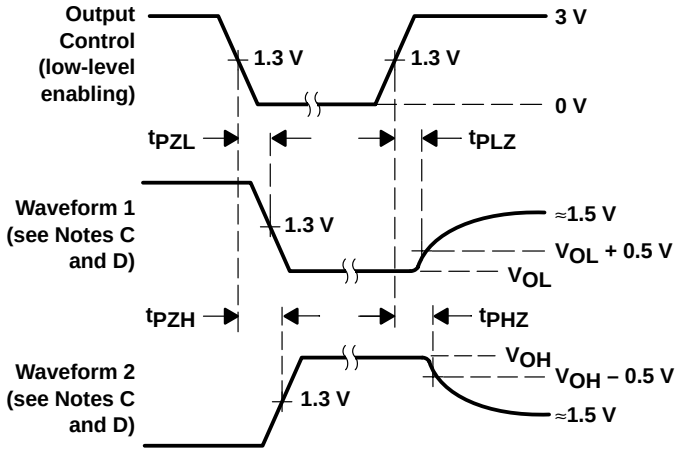
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \le 1.5$ ns, $t_f \le 2.6$ ns.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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