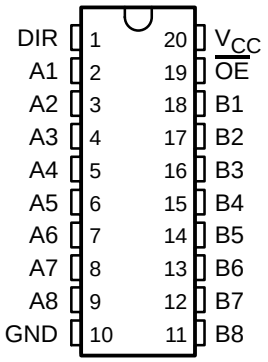
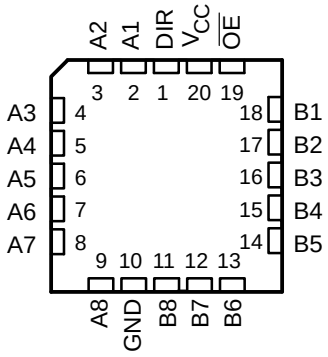
- **4.5-V to 5.5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 8 ns at 5 V**
- **Inputs Are TTL-Voltage Compatible**

SN54ACT245 . . . J OR W PACKAGE
SN74ACT245 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54ACT245 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

When the output-enable ($\overline{OE}$) is low, the device passes noninverted data from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. A high on $\overline{OE}$ disables the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

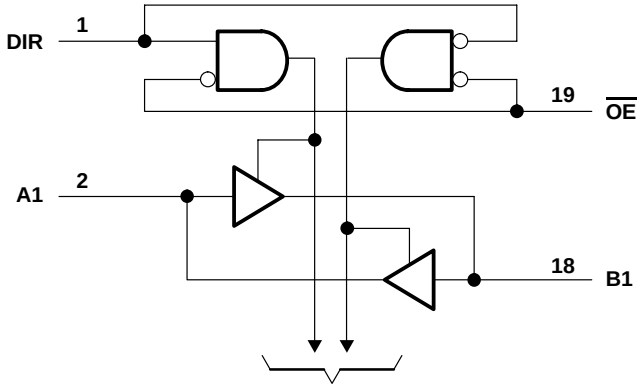
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74ACT245N	SN74ACT245N
	SOIC – DW	Tube	SN74ACT245DW	ACT245
		Tape and reel	SN74ACT245DWR	
	SOP – NS	Tape and reel	SN74ACT245NSR	ACT245
	SSOP – DB	Tape and reel	SN74ACT245DBR	AD245
	TSSOP – PW	Tape and reel	SN74ACT245PWR	AD245
–55°C to 125°C	CDIP – J	Tube	SNJ54ACT245J	SNJ54ACT245J
	CFP – W	Tube	SNJ54ACT245W	SNJ54ACT245W
	LCCC – FK	Tube	SNJ54ACT245K	SNJ54ACT245FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
PW package . . . . . 83°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54ACT245		SN74ACT245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		8		8	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54ACT245		SN74ACT245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	4.5 V	4.4	4.49		4.4		4.4		V
			5.5 V	5.4	5.49		5.4		5.4		
		I_{OH} = –24 mA	4.5 V	3.88			3.7		3.76		
			5.5 V	4.86			4.7		4.76		
		I_{OH} = –50 mA†	5.5 V				3.85				
		I_{OH} = –75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V		0.001	0.1		0.1		0.1	V
			5.5 V		0.001	0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_I	OE or DIR	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.6			1.6		1.5	mA
C_i		$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}		$V_O = V_{CC}$ or GND	5 V		15						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

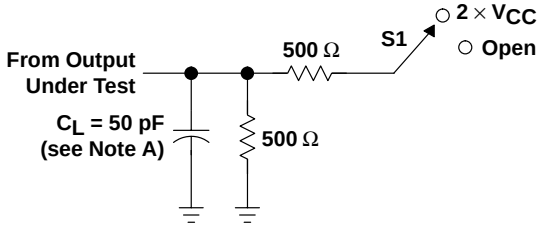
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54ACT245		SN74ACT245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	4	7.5	1	9	1.5	8	ns
t_{PHL}			1	4	8	1	10	1	9	
t_{PZH}	$\overline{OE}$	A or B	1	5	10	1	12	1.5	11	ns
t_{PZL}			1	5.5	10	1	13	1.5	12	
t_{PHZ}	$\overline{OE}$	A or B	1	5.5	10	1	12	1	11	ns
t_{PLZ}			1	5	10	1	12	1.5	11	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

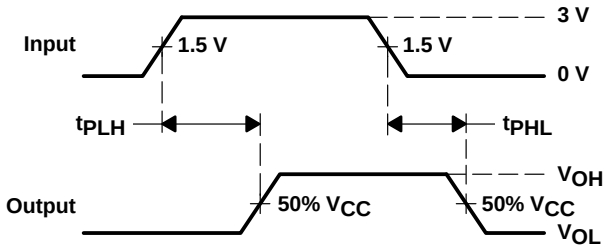
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	45	pF

PARAMETER MEASUREMENT INFORMATION

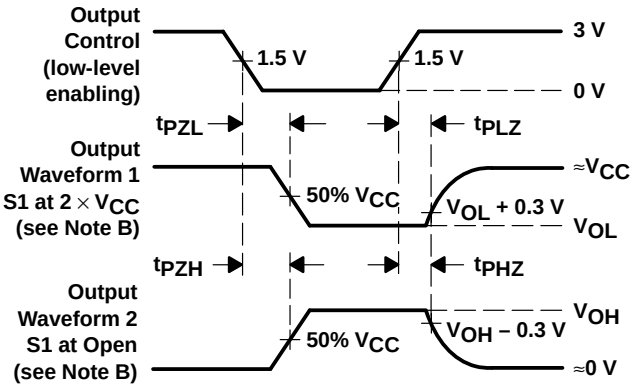


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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