

SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS048D – DECEMBER 1989 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- True Logic Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages

description

These octal D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

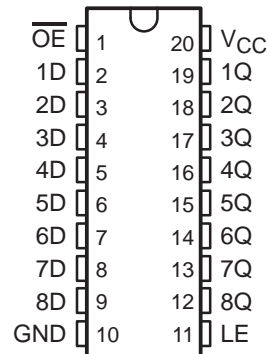
While the latch-enable (LE) input is high, outputs (Q) respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

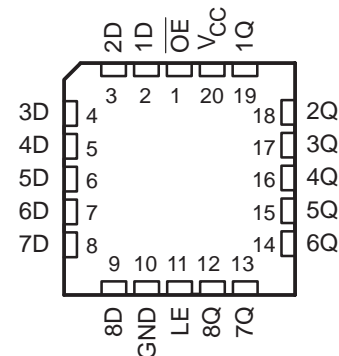
\overline{OE} does not affect internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS573C and SN54AS573A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS573C and SN74AS573A are characterized for operation from 0°C to 70°C .

SN54ALS573C, SN54AS573A . . . J OR W PACKAGE
SN74ALS573C, SN74AS573A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS573C, SN54AS573A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

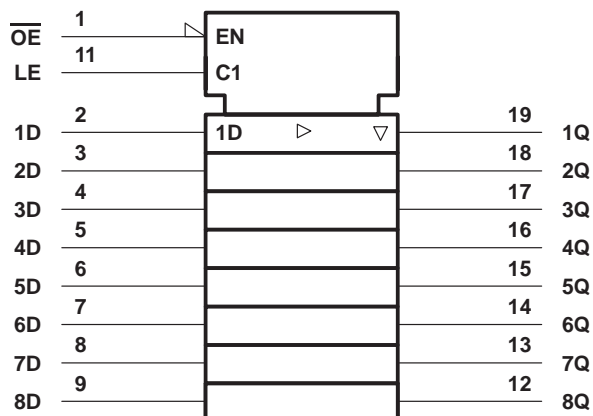
SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A

OCTAL D-TYPE TRANSPARENT LATCHES

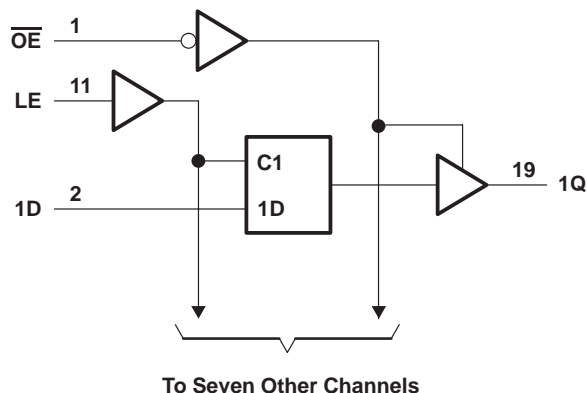
WITH 3-STATE OUTPUTS

SDAS048D – DECEMBER 1989 – REVISED JANUARY 1995

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54ALS573C	-55°C to 125°C
SN74ALS573C	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	SN54ALS573C			SN74ALS573C			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			-1			-2.6	mA
I_{OL} Low-level output current			12			24	mA
t_w Pulse duration, LE high	25			10			ns
t_{su} Setup time, data before LE↓	10			10			ns
t_h Hold time, data after LE↓	7			7			ns
T_A Operating free-air temperature	-55		125	0		70	°C

SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A

OCTAL D-TYPE TRANSPARENT LATCHES

WITH 3-STATE OUTPUTS

SDAS048D – DECEMBER 1989 – REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS573C		SN74ALS573C		UNIT
			MIN	TYP†	MAX	MIN	
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$	-1.2		-1.2		V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$,	$I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$		$V_{CC} - 2$		V
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.4	3.3			
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4	0.25	0.4	V
		$I_{OL} = 24\text{ mA}$			0.35	0.5	
I_{OZH}	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$	20		20		μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.4\text{ V}$	-20		-20		μA
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$	0.1		0.1		mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$	20		20		μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$	-0.13		-0.1		mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$	-20	-112	-30	-112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high	10	17	10	17	mA
		Outputs low	15	24	15	24	
		Outputs disabled	16	27	16	27	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$, $T_A = \text{MIN to MAX}\S$				UNIT
			SN54ALS573C		SN74ALS573C		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	20	2	14	ns
t_{PHL}			2	17	2	14	
t_{PLH}	LE	Q	8	33	6	20	ns
t_{PHL}			8	24	6	19	
t_{PZH}	\overline{OE}	Q	4	28	3	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	\overline{OE}	Q	2	20	1	10	ns
t_{PLZ}			3	26	1	15	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A

OCTAL D-TYPE TRANSPARENT LATCHES

WITH 3-STATE OUTPUTS

SDAS048D – DECEMBER 1989 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54AS573A	–55°C to 125°C
SN74AS573A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS573A			SN74AS573A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			32			48	mA
t_w^*	Pulse duration, LE high	5.5			4.5			ns
t_{su}^*	Setup time, data before LE↓	2			2			ns
t_h^*	Hold time, data after LE↓	3			3			ns
T_A	Operating free-air temperature	–55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS573A			SN74AS573A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V	$I_{OH} = -12$ mA	2.4	3.2		2.4	3.3	
		$I_{OH} = -15$ mA						
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 32$ mA	0.28	0.5				V
		$I_{OL} = 48$ mA				0.33	0.5	
I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			50			50	μA
I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.4$ V			–50			–50	μA
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20			20	μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			–0.1			–0.5	mA
$I_{O§}$	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	–30		–112	–30		–112	mA
I_{CC}	$V_{CC} = 5.5$ V	Outputs high	56	93	56	93		mA
		Outputs low	55	90	55	90		
		Outputs disabled	65	106	65	106		

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



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switching characteristics (see Figure 1)

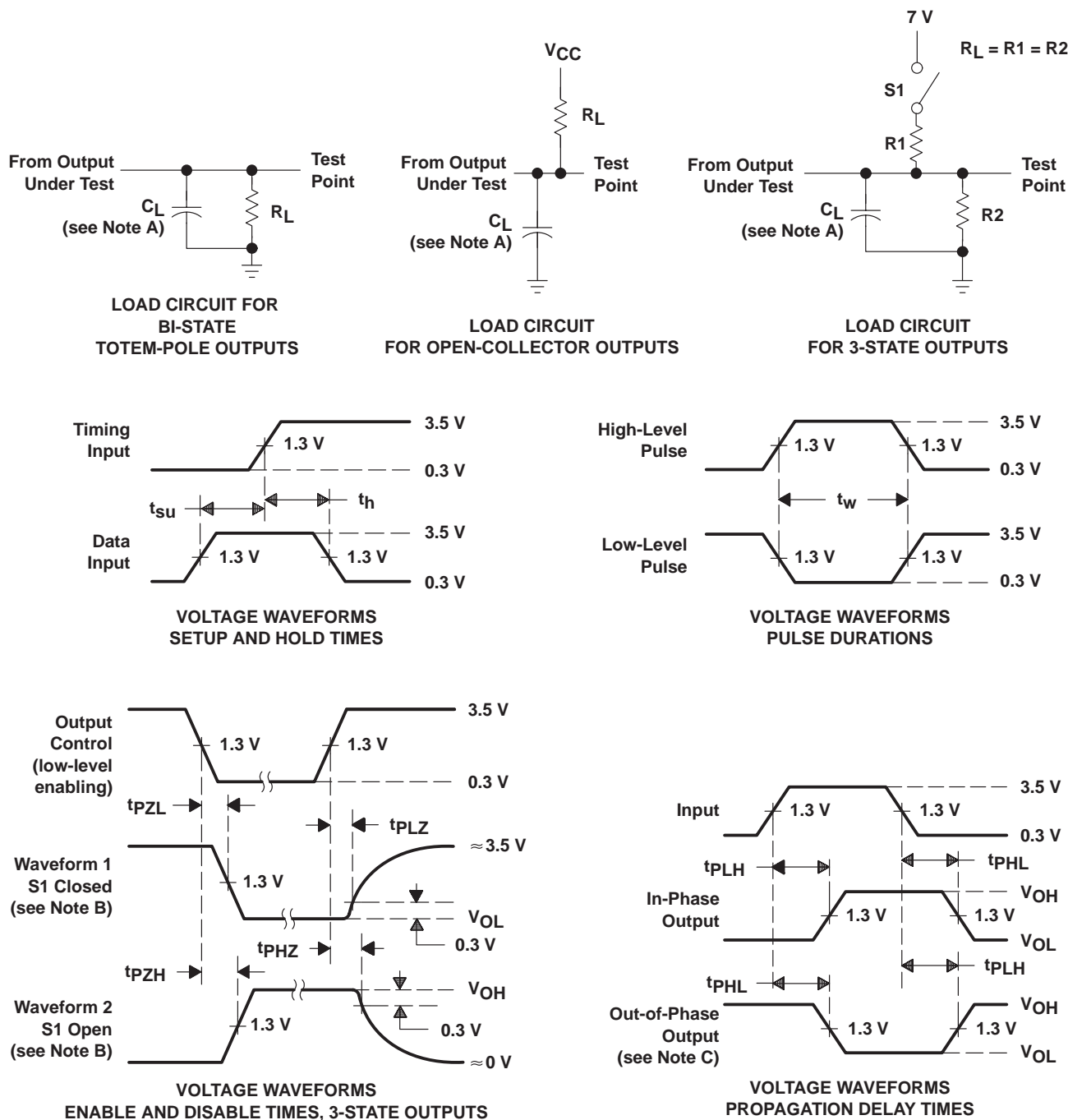
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = \text{MIN to MAX}^\dagger$				UNIT
			SN54AS573A		SN74AS573A		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	11	3	8	ns
t_{PHL}			3	8	3	7	
t_{PLH}	LE	Q	6	16.5	6	13	ns
t_{PHL}			4	9	4	7.5	
t_{PZH}	\overline{OE}	Q	2	8	2	6.5	ns
t_{PZL}			4	11	4	9.5	
t_{PHZ}	\overline{OE}	Q	2	8	2	6.5	ns
t_{PLZ}			2	8	2	7	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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SDAS048D – DECEMBER 1989 – REVISED JANUARY 1995

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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