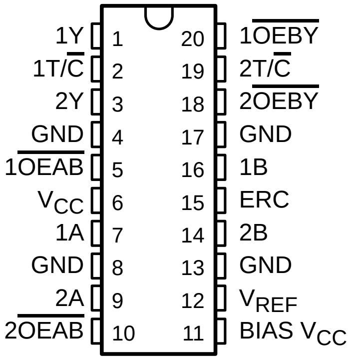
SN74GTLP1395
TWO 1-BIT LVTTL-TO-GTLP ADJUSTABLE-EDGE-RATE BUS TRANSCEIVERS WITH SPLIT LVTTL PORT, FEEDBACK PATH, AND SELECTABLE POLARITY

SCES349C – JUNE 2001 – REVISED NOVEMBER 2001

- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **Split LVTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Polarity Control Selects True or Complementary Outputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74GTLP1395 is two 1-bit, high-drive, 3-wire bus transceivers that provide LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation for applications, such as primary and secondary clocks, that require individual output-enable and true/complement controls. The device allows for transparent and inverted transparent modes of data transfer with separate LVTTL input and LVTTL output pins, which provide a feedback path for control and diagnostics monitoring. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels and is designed especially to work with the Texas Instruments 3.3-V 1394 backplane physical-layer controller. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuitry minimizes bus settling time, and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes, with equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP1395 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. For information on using GTLP devices in FB+/BTL applications, refer to TI application reports, *Texas Instruments GTLP Frequently Asked Questions*, literature number SCEA019, and *GTLP in BTL Applications*, literature number SCEA017.

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description (continued)

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL or 5-V CMOS devices. V_{REF} is the B-port differential input reference voltage.

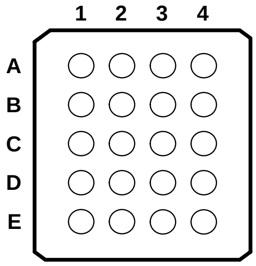
This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between low and high adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

GQN PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4
A	1T/$\overline{C}$	1Y	1$\overline{OEBY}$	2T/$\overline{C}$
B	GND	GND	2Y	2$\overline{OEBY}$
C	V_{CC}	1$\overline{OEAB}$	ERC	1B
D	GND	GND	1A	2B
E	2$\overline{OEAB}$	2A	BIAS V_{CC}	V_{REF}

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74GTLP1395DW	GTLP1395
		Tape and reel	SN74GTLP1395DWR	
	TSSOP – PW	Tape and reel	SN74GTLP1395PWR	GP395
	TVSOP – DGV	Tape and reel	SN74GTLP1395DGVR	GP395
	VFBGA – GQN	Tape and reel	SN74GTLP1395GQNR	GP395

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The output-enable (1$\overline{\mathrm{OEAB}}$, 1$\overline{\mathrm{OEBY}}$) and polarity-control (1T/$\overline{\mathrm{C}}$) inputs control 1A, 1B, and 1Y. 2$\overline{\mathrm{OEAB}}$, 2$\overline{\mathrm{OEBY}}$, and 2T/$\overline{\mathrm{C}}$ control 2A, 2B, and 2Y.

$\overline{\mathrm{OEAB}}$ controls the activity of the B port. When $\overline{\mathrm{OEAB}}$ is low, the B-port output is active. When $\overline{\mathrm{OEAB}}$ is high, the B-port output is disabled.

A separate LVTTL A input and Y output provide a feedback path for control and diagnostics monitoring. $\overline{\mathrm{OEBY}}$ controls the Y output. When $\overline{\mathrm{OEBY}}$ is low, the Y output is active. When $\overline{\mathrm{OEBY}}$ is high, the Y output is disabled.

T/$\overline{\mathrm{C}}$ selects polarity of data transmission in both directions. When T/$\overline{\mathrm{C}}$ is high, data transmission is true, and A data goes to the B bus and B data goes to the Y bus. When T/$\overline{\mathrm{C}}$ is low, data transmission is complementary, and inverted A data goes to the B bus and inverted B data goes to the Y bus.

Function Tables

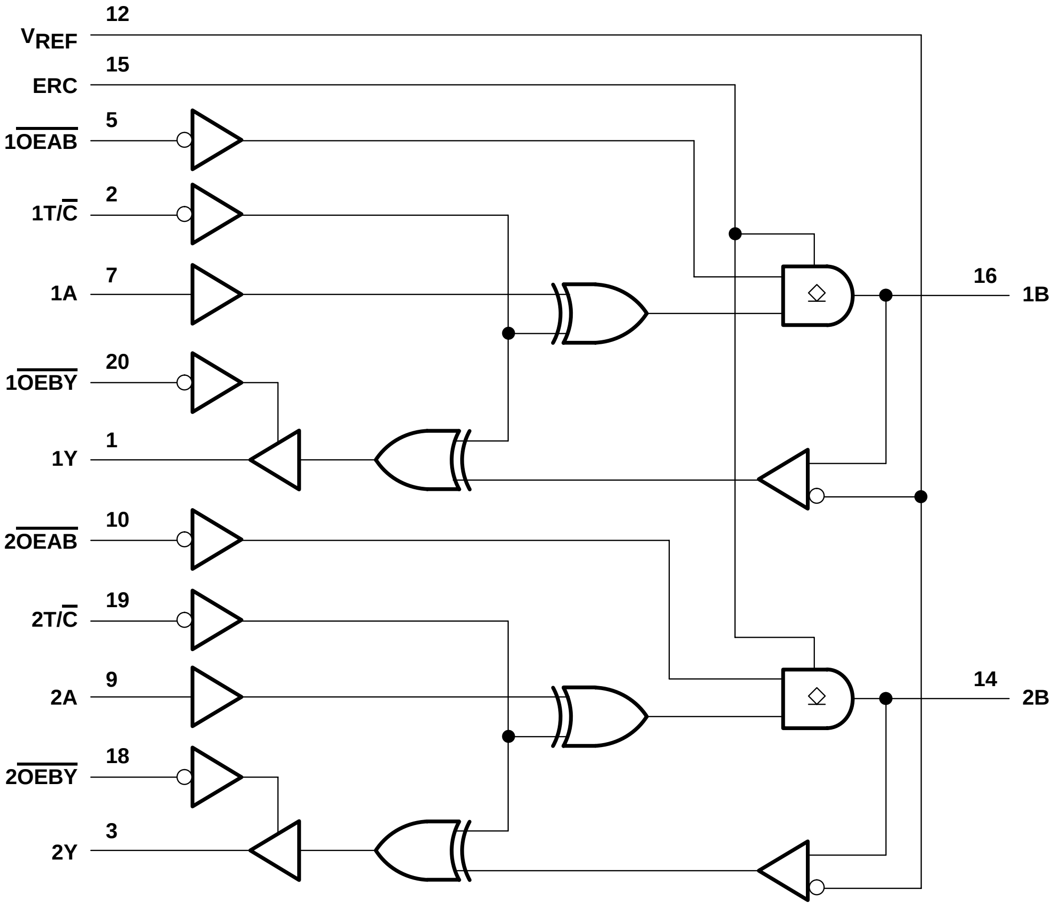
OUTPUT CONTROL

INPUTS			OUTPUT	MODE
T/$\overline{\mathrm{C}}$	$\overline{\mathrm{OEAB}}$	$\overline{\mathrm{OEBY}}$		
X	H	H	Z	Isolation
H	L	H	A data to B bus	True transparent
H	H	L	B data to Y bus	
H	L	L	A data to B bus, B data to Y bus	True transparent with feedback path
L	L	H	Inverted A data to B bus	Inverted transparent
L	H	L	Inverted B data to Y bus	
L	L	L	Inverted A data to B bus, Inverted B data to Y bus	Inverted transparent with feedback path

OUTPUT EDGE-RATE CONTROL (ERC)

INPUT ERC LOGIC LEVEL	OUTPUT B-PORT EDGE RATE
H	Slow
L	Fast

logic diagram (positive logic)



Pin numbers shown are for the DGV, DW, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A inputs, ERC, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): Y outputs	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: Y outputs	48 mA
B port	200 mA
Current into any output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGV package	92°C/W
DW package	58°C/W
GQN package	78°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

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† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			V
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	Y outputs			–24	mA
I_{OL}	Low-level output current	Y outputs			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES:

4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally it is two-thirds V_{TT}. TI-OPC is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	Y outputs	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	Y outputs	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I[‡]	A-port and control inputs	V_{CC} = 3.45 V,	V_I = 0 to 5.5 V			±10	µA
I_{OZ}[‡]	Y outputs	V_{CC} = 3.45 V,	V_O = 0 to 5.5 V			±10	µA
	B port	V_{CC} = 3.45 V, V_{REF} within 0.6 V of V_{TT},	V_O = 0 to 2.3 V			±10	
I_{CC}	Y outputs or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A or control inputs) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			20	mA
			Outputs low			20	
			Outputs disabled			20	
ΔI_{CC}[§]		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	A-port inputs	V_I = 3.15 V or 0			4	4.5	pF
	Control inputs				3.5	5	
C_o	Y outputs	V_O = 3.15 V or 0			5	5.5	pF
C_{io}	B port	V_O = 1.5 V or 0			7	10.5	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.
[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

hot-insertion specifications for A inputs and Y outputs over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OEBY}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OEBY}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS				MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V,	$\overline{OEAB}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V,	$\overline{OEAB}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V			5	mA
	V_{CC} = 3.15 V to 3.45 V					10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0		0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V		–1		µA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE[†]	MIN	TYP[‡]	MAX	UNIT
t_{PLH}	A	B	Slow	3.3		6.3	ns
t_{PHL}				1.9		6	
t_{PLH}	A	B	Fast	2.5		5.3	ns
t_{PHL}				1.6		4.9	
t_{PLH}	A	Y	Slow	3.4		9.7	ns
t_{PHL}				3.3		9.2	
t_{PLH}	A	Y	Fast	2.9		8.7	ns
t_{PHL}				2.9		8.1	
t_{PLH}	$T/\overline{C}$	B	Slow	3.7		6.7	ns
t_{PHL}				1.8		6.2	
t_{PLH}	$T/\overline{C}$	B	Fast	1.5		5.6	ns
t_{PHL}				1.7		5.5	
t_{en}	$\overline{OEAB}$	B	Slow	3.8		6.4	ns
t_{dis}				1.9		6.1	
t_{en}	$\overline{OEAB}$	B	Fast	2.8		5.3	ns
t_{dis}				1.5		5	
t_r	Rise time, B outputs (20% to 80%)		Slow		2.4		ns
			Fast		1.3		
t_f	Fall time, B outputs (80% to 20%)		Slow		3		ns
			Fast		2.7		
t_{PLH}	B	Y		1.3		5.3	ns
t_{PHL}				1.4		4.5	
t_{PLH}	$T/\overline{C}$	Y		1		4.5	ns
t_{PHL}				1.1		4	
t_{en}	$\overline{OEBY}$	Y		1		4.5	ns
t_{dis}				1		4.7	

[†] Slow (ERC = H) and Fast (ERC = L)
[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

skew characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1 V, standard lumped loads (C_L = 30 pF for B port and C_L = 50 pF for Y port) (unless otherwise noted)(see Figure 1)[†]

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE[‡]	MIN	MAX	UNIT
$t_{sk(LH)}$[§]	A	B	Slow		0.3	ns
$t_{sk(HL)}$[§]					0.4	
$t_{sk(LH)}$[§]	A	B	Fast		0.3	ns
$t_{sk(HL)}$[§]					0.3	
$t_{sk(LH)}$[§]	B	Y			0.4	ns
$t_{sk(HL)}$[§]					0.2	
$t_{sk(t)}$[§]	A	B	Slow		1.8	ns
			Fast		1.5	
	B	Y			1	
$t_{sk(prLH)}$[¶]	A	B	Slow		0.7	ns
$t_{sk(prHL)}$[¶]					2	
$t_{sk(prLH)}$[¶]	A	B	Fast		0.5	ns
$t_{sk(prHL)}$[¶]					1.7	
$t_{sk(prLH)}$[¶]	B	Y			1.2	ns
$t_{sk(prHL)}$[¶]					1.6	

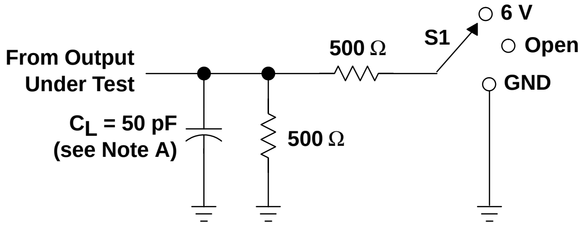
[†] Actual skew values between GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

[‡] Slow (ERC = L) and Fast (ERC = H)

[§] $t_{sk(LH)}$/$t_{sk(HL)}$ and $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs with the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in the same direction either high to low [$t_{sk(HL)}$] or low to high [$t_{sk(LH)}$] or in opposite directions, both low to high and high to low [$t_{sk(t)}$].

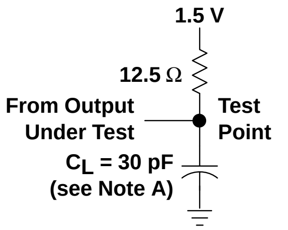
[¶] $t_{sk(prLH)}$/$t_{sk(prHL)}$ – The magnitude of the difference in propagation delay times between corresponding terminals of two logic devices when both logic devices operate with the same supply voltages and at the same temperature, and have identical package types, identical specified loads, and identical logic functions. Furthermore, these values are provided by SPICE simulations.

PARAMETER MEASUREMENT INFORMATION

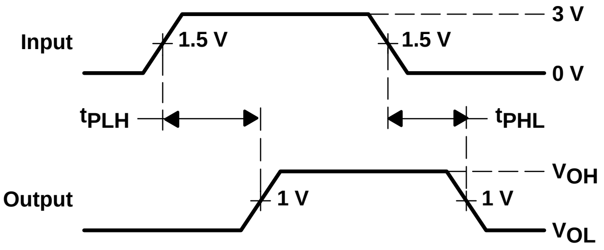


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

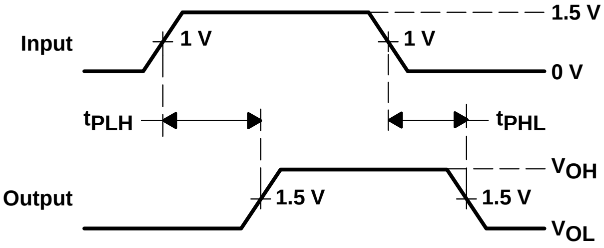
LOAD CIRCUIT FOR Y OUTPUTS



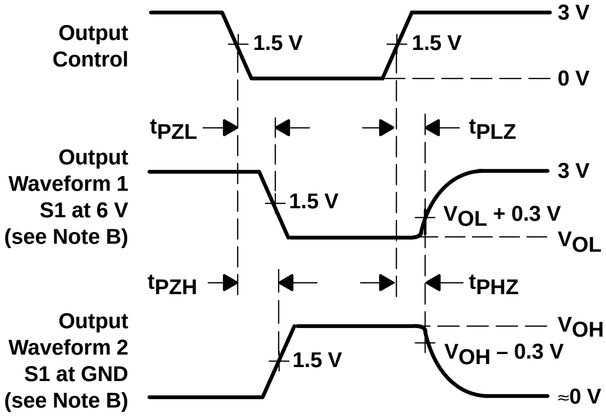
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (A input to B port)



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (B port to Y output)



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES (A input)

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in the backplane. See www.ti.com/sc/gtlp for more information.

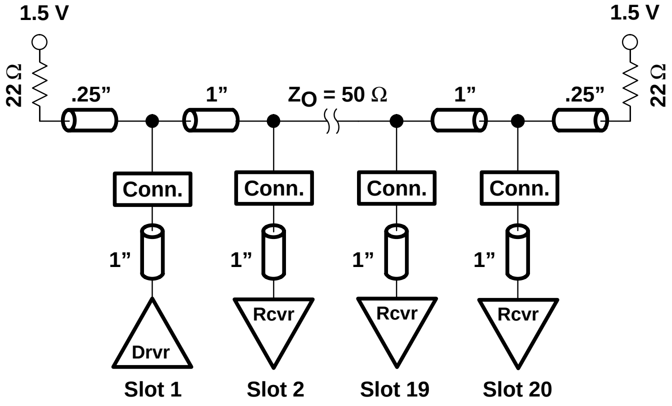


Figure 2. High-Drive Test Backplane

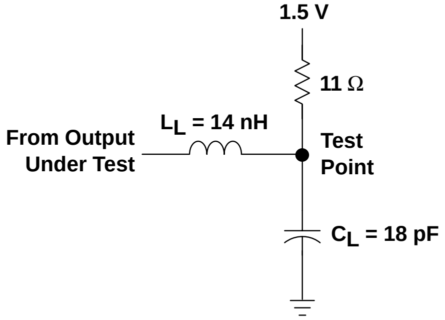


Figure 3. High-Drive RLC Network

switching characteristics over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE[†]	TYP[‡]	UNIT
t_{PLH}	A	B	Slow	4.3	ns
t_{PHL}				4.2	
t_{PLH}	A	B	Fast	3.8	ns
t_{PHL}				3.4	
t_{PLH}	A	Y	Slow	6.1	ns
t_{PHL}				5.9	
t_{PLH}	A	Y	Fast	5.6	ns
t_{PHL}				5.4	
t_r	Rise time, B outputs (20% to 80%)		Slow	1.5	ns
			Fast	1	
t_f	Fall time, B outputs (80% to 20%)		Slow	2.6	ns
			Fast	2	

[†] Slow (ERC = H) and Fast (ERC = L)
[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI SPICE models.

APPLICATION INFORMATION

operational description

The GTLP1395 is designed specifically for use with the TI 1394 backplane layer controller family to transmit the 1394 backplane serial bus across parallel backplanes. But, it is a versatile two 1-bit device that also can provide multiple 1-bit clocks or an ATM read and write clock in multislot parallel backplane applications.

The 1394–1995 is an IEEE designation for a high-performance serial bus. This serial bus defines both a backplane (e.g., GTLP, VME, FB+, CPCI, etc.) physical layer and a point-to-point cable-connected virtual bus. The backplane version operates at 25, 50, or 100 Mbps, whereas the cable version supports data rates of 100, 200, and 400 Mbps. Both versions are compatible at the link layer and above. The interface standard defines the transmission method, media in the cable version, and protocol. The primary application of the cable version is the interconnection of digital A/V equipment and integration of I/O connectivity at the back panel of personal computers using a low-cost, scalable, high-speed serial interface. The primary application of the backplane version is to provide a robust control interface to each daughter card. The 1394 standard also provides new services such as real-time I/O and live connect/disconnect capability for external devices.

electrical

The 1394 standard is a transaction-based packet technology for cable- or backplane-based environments. Both chassis and peripheral devices can use this technology. The 1394 serial bus is organized as if it were memory space interconnected between devices, or as if devices resided in slots on the main backplane. Device addressing is 64 bits wide, partitioned as 10 bits for bus ID, 6 bits for node ID, and 48 bits for memory addresses. The result is the capability to address up to 1023 buses, each having up to 63 nodes and each with 281 terabytes of memory. Memory-based addressing, rather than channel addressing, views resources as registers or memory that can be accessed with processor-to-memory transactions. Each bus entity is termed a unit, to be individually addressed, reset, and identified. Multiple nodes can reside physically in a single module, and multiple ports can reside in a single node.

Some key features of the 1394 topology are multimaster capabilities, live connect/disconnect (hot plugging) capability, genderless cabling connectors on interconnect cabling, and dynamic node address allocation as nodes are added to the bus. A maximum of 63 nodes can be connected to one network.

The cable-based physical interface uses dc-level line states for signaling during initialization and arbitration. Both environments use dominant mode addresses for arbitration. The backplane environment does not have the initialization requirements of the cable environment because it is a physical bus and does not contain repeaters. Due to the differences, a backplane-to-cable bridge is required to connect these two environments.

The signals transmitted on both the cable and backplane environments are NRZ with data-strobe (DS) encoding. DS encoding allows only one of the two signal lines to change each data bit period, essentially doubling the jitter tolerance with very little additional circuitry overhead in the hardware.

APPLICATION INFORMATION

protocol

Both asynchronous and isochronous data transfers are supported. The asynchronous format transfers data and transaction layer information to an explicit address. The isochronous format broadcasts data based on channel numbers rather than specific addressing. Isochronous packets are issued on the average of each 125 µs in support of time-sensitive applications. Providing both asynchronous and isochronous formats on the same interface allows both non-real-time and real-time critical applications on the same bus. The cable environment's tree topology is resolved during a sequence of events, triggered each time a new node is added or removed from the network. This sequence starts with a bus reset phase, where previous information about a topology is cleared. The tree ID sequence determines the actual tree structure, and a root node is dynamically assigned, or it is possible to force a particular node to become the root. After the tree is formed, a self-ID phase allows each node on the network to identify itself to all other nodes. During the self-ID process, each node is assigned an address. After all the information has been gathered on each node, the bus goes into an idle state, waiting for the beginning of the standard arbitration process.

The backplane physical layer shares some commonality with the cable physical layer. Common functions include: bus-state determination, bus-access protocols, encoding and decoding functions, and synchronization of received data to a local clock.

backplane features

- 25-, 50-, and 100-Mbps data rates for backplane environments
- Live connection/disconnection possible without data loss or interruption
- Configuration ROM and status registers supporting plug and play
- Multidrop or point-to-point topologies supported.
- Specified bandwidth assignments for real-time applications

applicability and typical application for IEEE 1394 backplane

The 1394 backplane serial bus (BPSB) plays a supportive role in backplane systems, specifically GTLP, FutureBus+, VME64, and proprietary backplane bus systems. This supportive role can be grouped into three categories:

- Diagnostics
  - Alternate control path to the parallel backplane bus
  - Test, maintenance, and troubleshooting
  - Software debug and support interface
- System enhancement
  - Fault tolerance
  - Live insertion
  - CSR access
  - Auxiliary 2-bit bus with a 64-bit address space to the parallel backplane bus
- Peripheral monitoring
  - Monitoring of peripherals (disk drives, fans, power supplies, etc.) in conjunction with another externally wired monitor bus, such as defined by the Intelligent Platform Management Interface (IPMI)

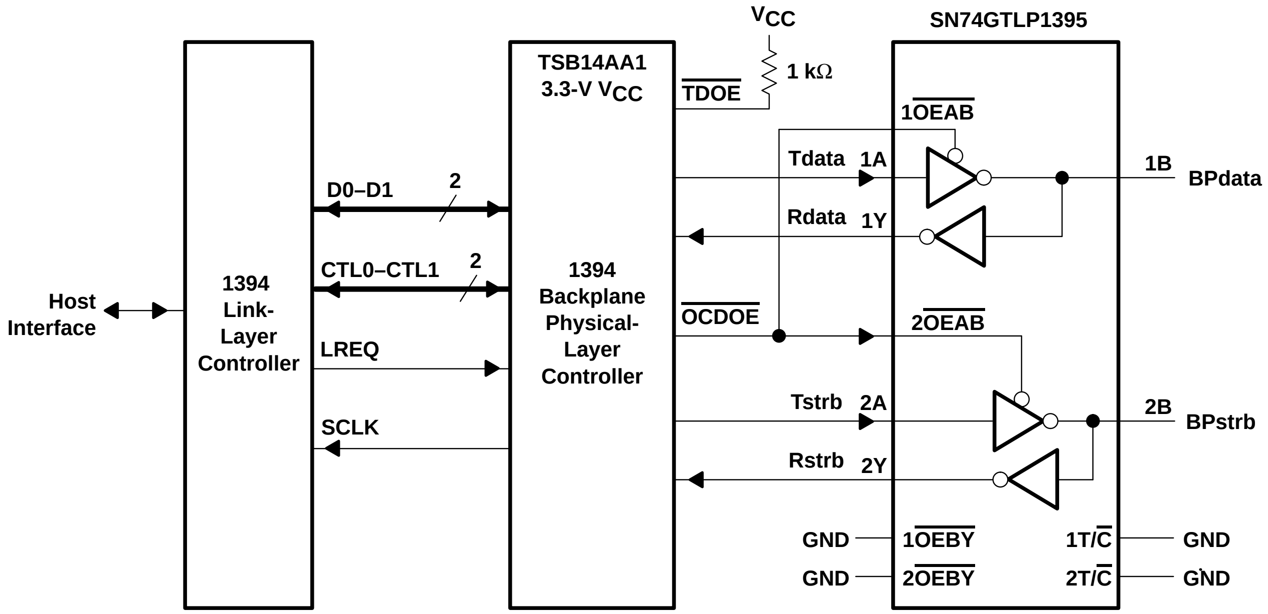
The 1394 backplane physical layer (PHY) and the SN74GTLP1395 provide a cost-effective way to add high-speed 1394 connections to every daughter card in almost any backplane. More information on the backplane PHY devices and how to implement the 1394 standard in backplane and cable applications can be found at www.ti.com/sc/1394.

APPLICATION INFORMATION

SN74GTLP1395 interface with the TSB14AA1 1394 backplane PHY

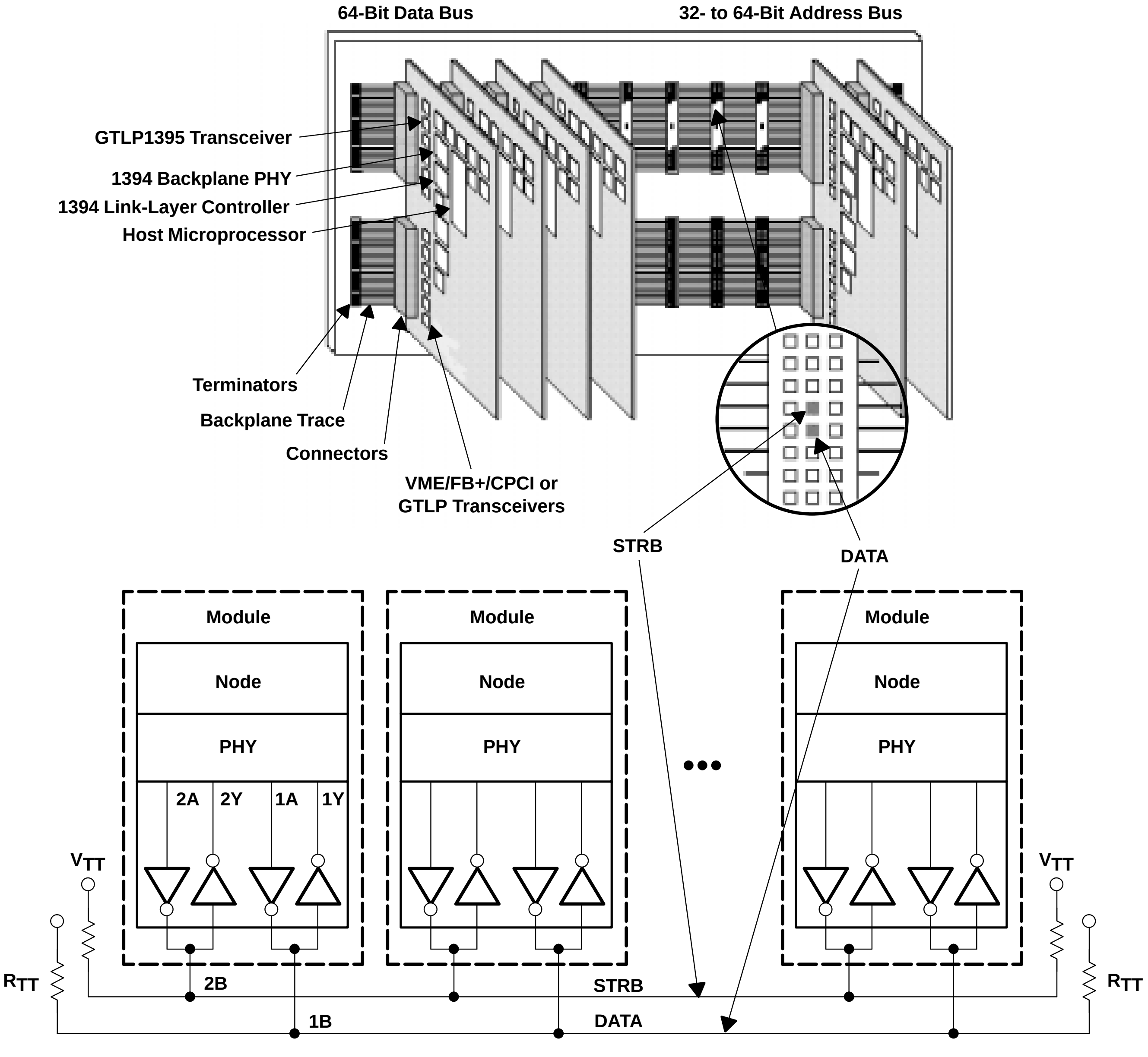
- 1A, 1B, and 1Y are used for the PHY data signals.
- 2A, 2B, and 2Y are used for the PHY strobe signals.
- PHY N_OEB_D or $\overline{\text{OCDOE}}$ connects to 1$\overline{\text{OEAB}}$ and 2$\overline{\text{OEAB}}$, which control the PHY transmit signals.
- 1$\overline{\text{OEBY}}$ and 2$\overline{\text{OEBY}}$ are connected to GND because the transceiver must always be able to receive signals from the backplane and relay them to the PHY.
- 1T/$\overline{\text{C}}$ and 2T/$\overline{\text{C}}$ are connected to GND for inverted signals.
- V_{CC} is nominal 3.3 V.
- BIAS V_{CC} is connected to nominal 3.3 V to support live insertion.
- V_{REF} is normally 2/3 of V_{TT}.
- ERC is normally connected to V_{CC} for slow edge-rate operation because frequencies of only 50 MHz (S100) and 25 MHz (S50) are required.

logical representation

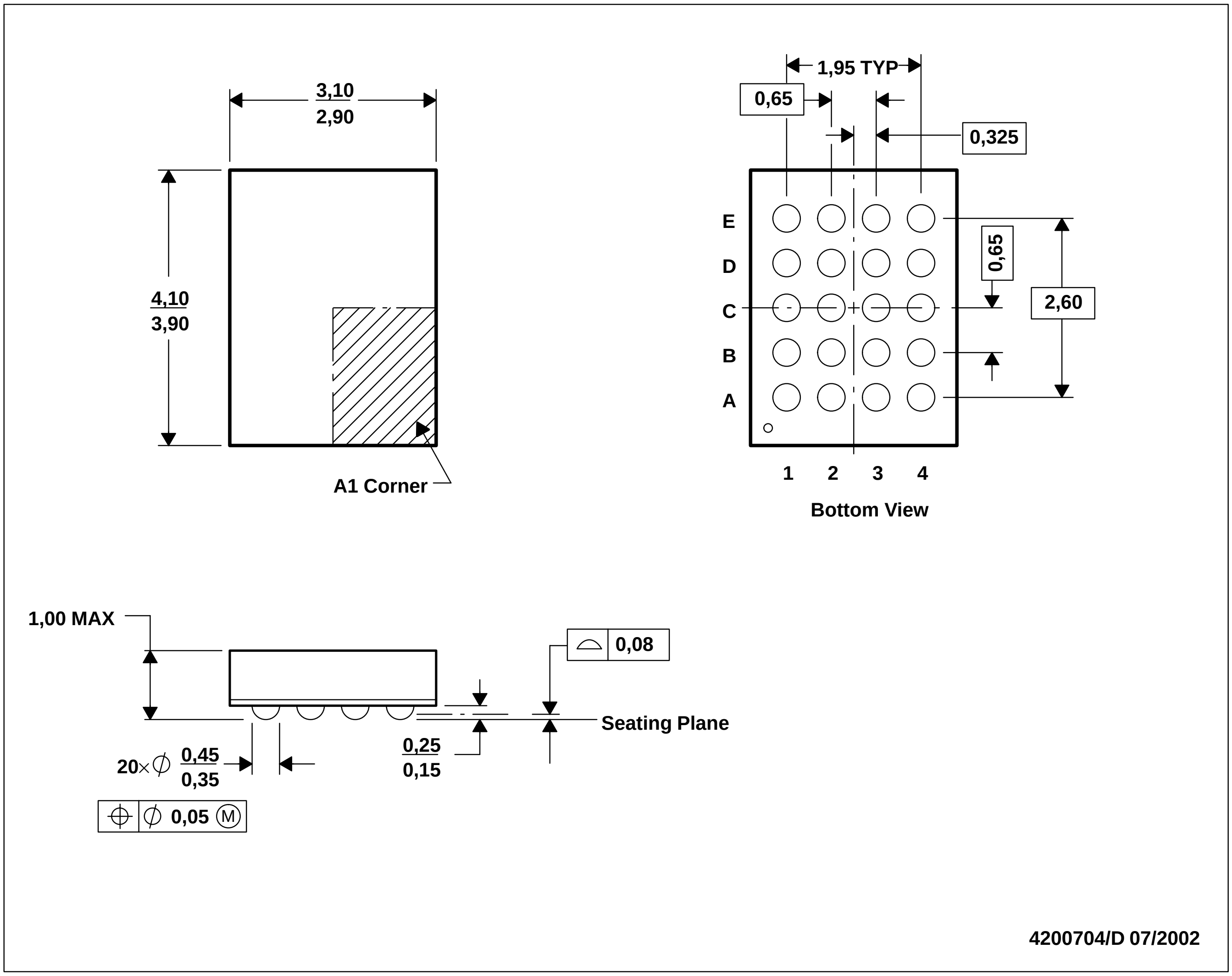


APPLICATION INFORMATION

physical representation



GQN (R-PBGA-N20) PLASTIC BALL GRID ARRAY

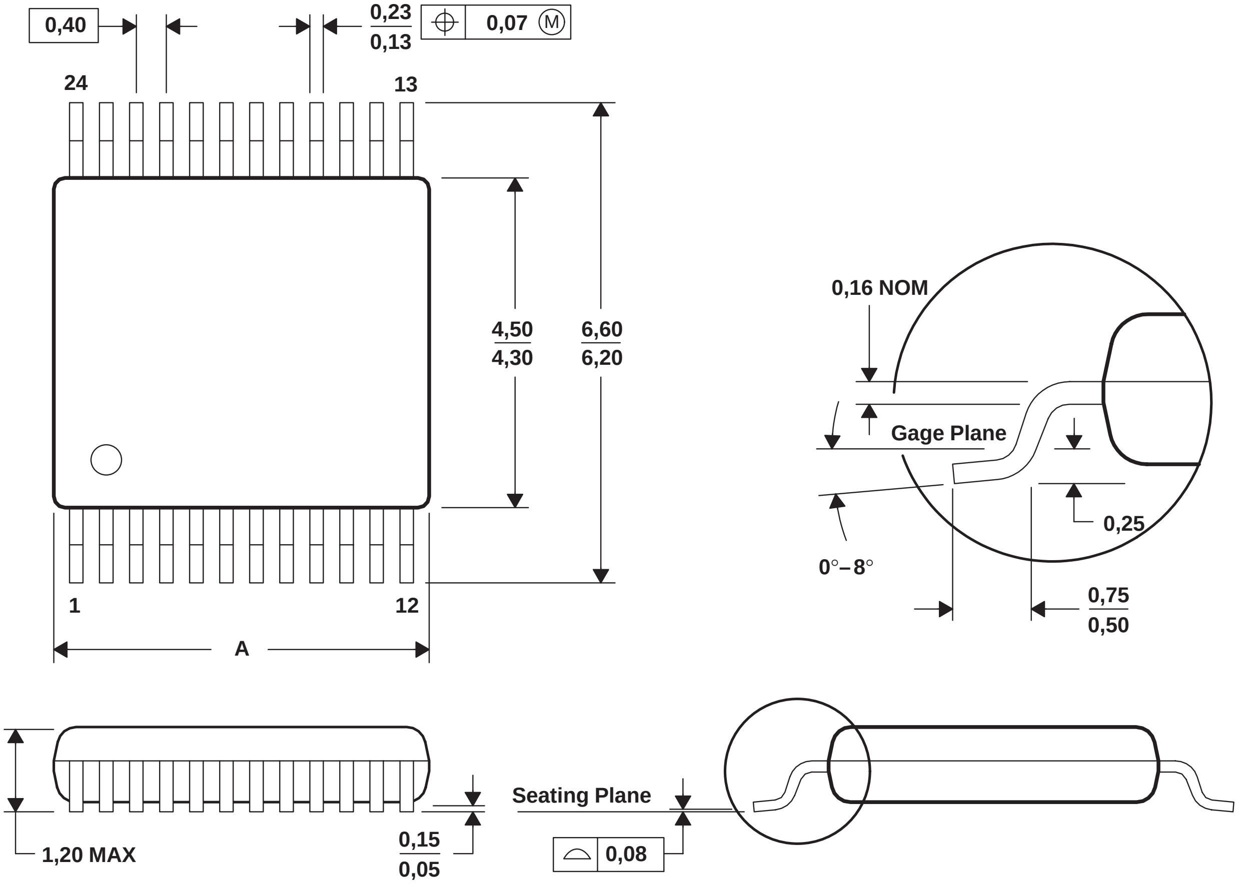


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar Junior™ configuration
- D. Falls within JEDEC MO-225 variation BC.
- E. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

24 PINS SHOWN



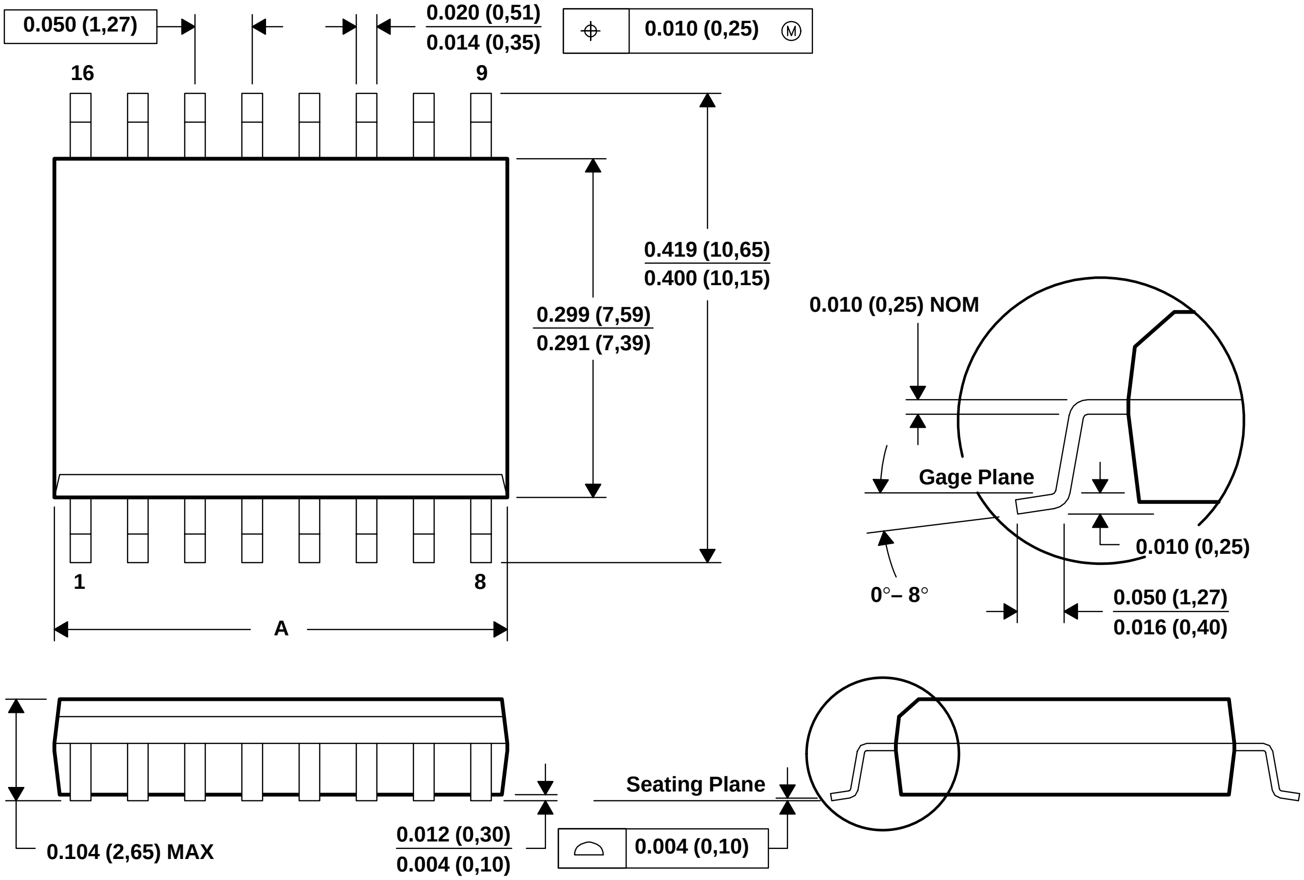
DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

DW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



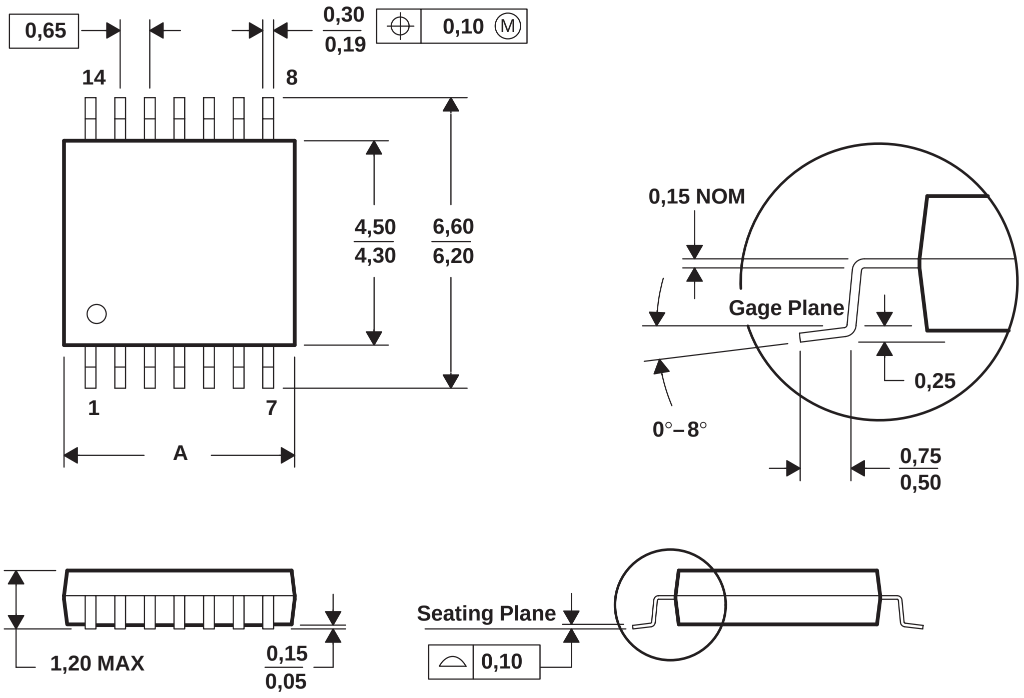
PINS ** / DIM	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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