



STP40NF10 STB40NF10

N-CHANNEL 100V - 0.024Ω - 50A TO-220/D²PAK LOW GATE CHARGE STripFET™ II POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP40NF10	100 V	< 0.028 Ω	50 A
STB40NF10	100 V	< 0.028 Ω	50 A

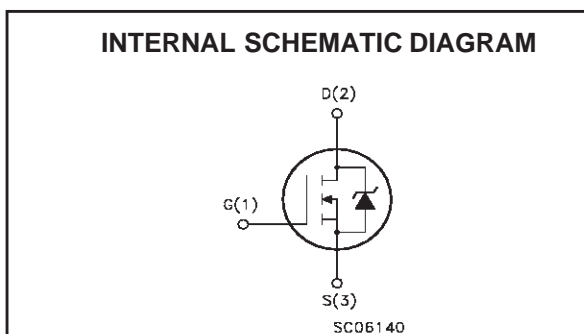
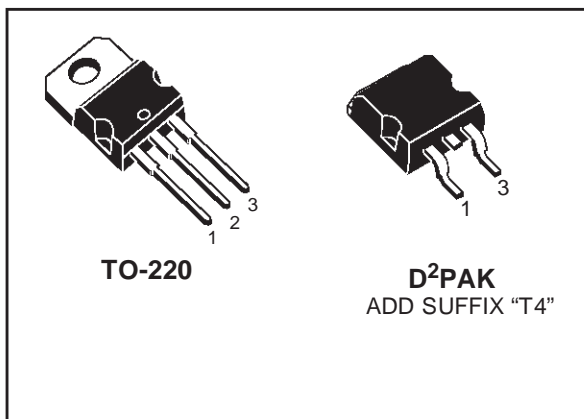
- TYPICAL R_{DS(on)} = 0.024Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION

DESCRIPTION

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	100	V
V _{GS}	Gate- source Voltage	± 20	V
I _D (*)	Drain Current (continuous) at T _C = 25°C	50	A
I _D	Drain Current (continuous) at T _C = 100°C	35	A
I _{DM} (†)	Drain Current (pulsed)	200	A
P _{TOT}	Total Dissipation at T _C = 25°C	150	W
	Derating Factor	1	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	20	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	320	mJ
T _{stg}	Storage Temperature	- 55 to 175	°C
T _j	Operating Junction Temperature		

(●) Pulse width limited by safe operating area

(*) Limited by Package

(1) I_{SD} ≤ 40A, di/dt ≤ 600A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(2) Starting T_j = 25°C, I_D = 25A, V_{DD} = 50V

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THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	100			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2	2.8	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 20 A		0.024	0.028	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 25V, I _D = 20 A		20		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1780		pF
C _{oss}	Output Capacitance			265		pF
C _{rss}	Reverse Transfer Capacitance			112		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 50\text{ V}, I_D = 20\text{ A}$		28		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		63		ns
Q_g	Total Gate Charge	$V_{DD} = 80\text{ V}, I_D = 40\text{ A}, V_{GS} = 10\text{ V}$		60	80	nC
Q_{gs}	Gate-Source Charge			10		nC
Q_{gd}	Gate-Drain Charge			23		nC

SWITCHING OFF

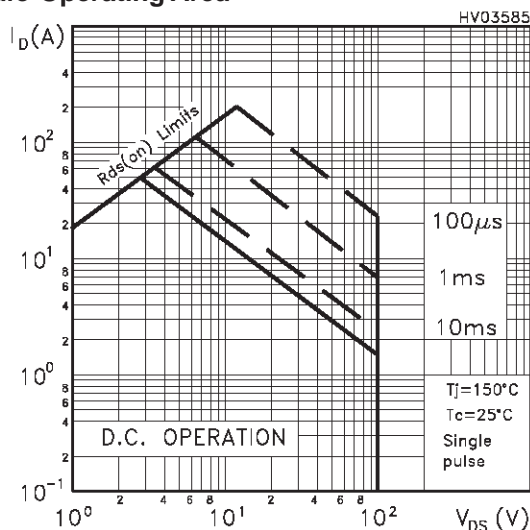
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 50\text{ V}, I_D = 20\text{ A},$		84		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		28		ns

SOURCE DRAIN DIODE

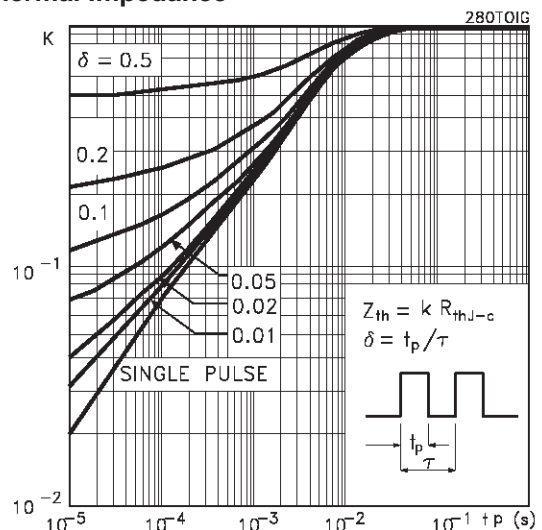
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				40	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				160	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 40\text{ A}, V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 40\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$		114		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 25\text{ V}, T_j = 150^\circ\text{C}$		456		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		8		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Safe Operating Area

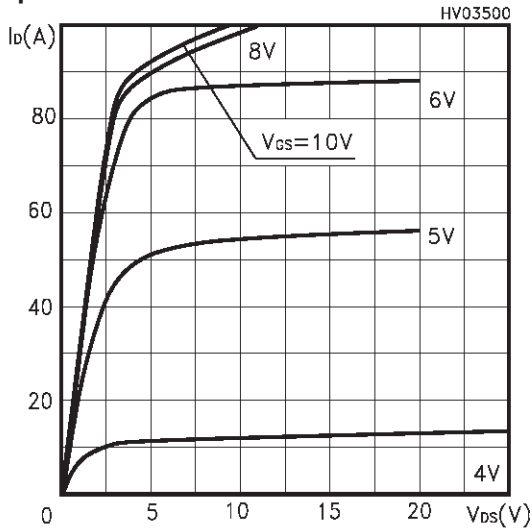


Thermal Impedance

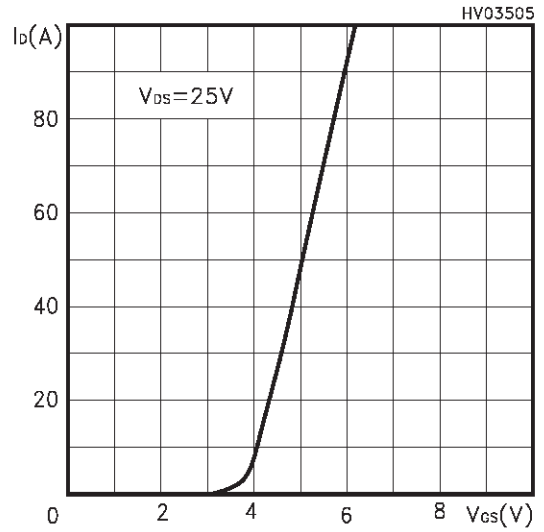


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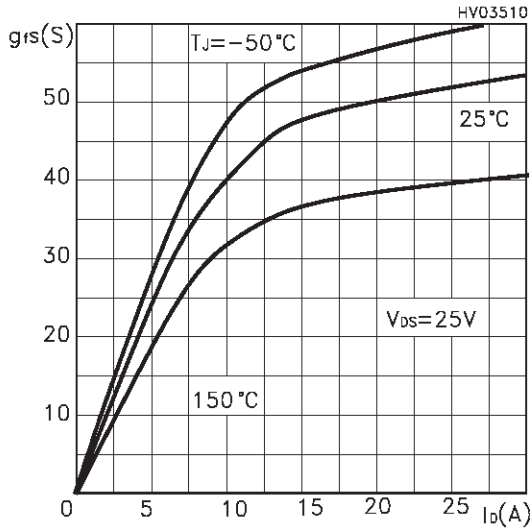
Output Characteristics



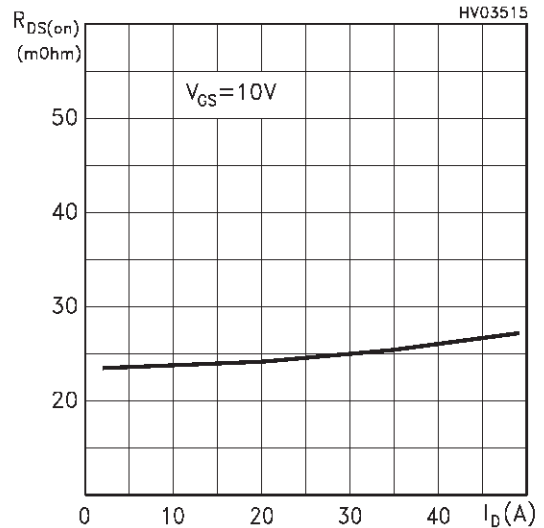
Transfer Characteristics



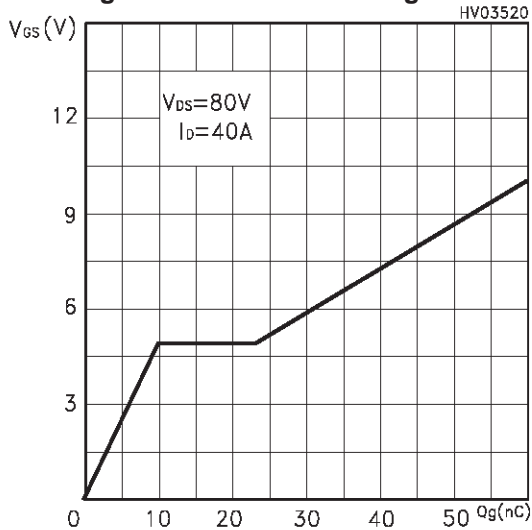
Transconductance



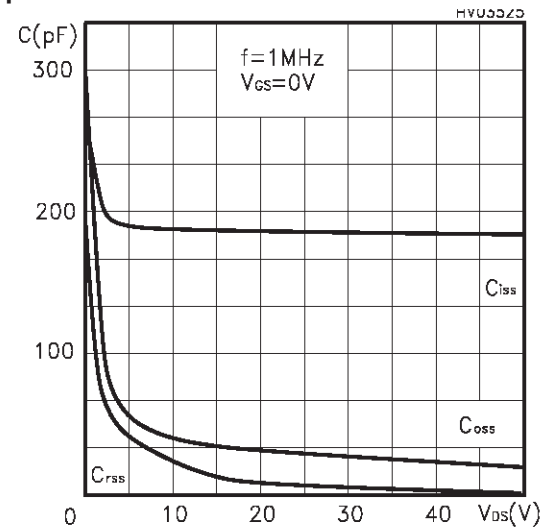
Static Drain-source On Resistance



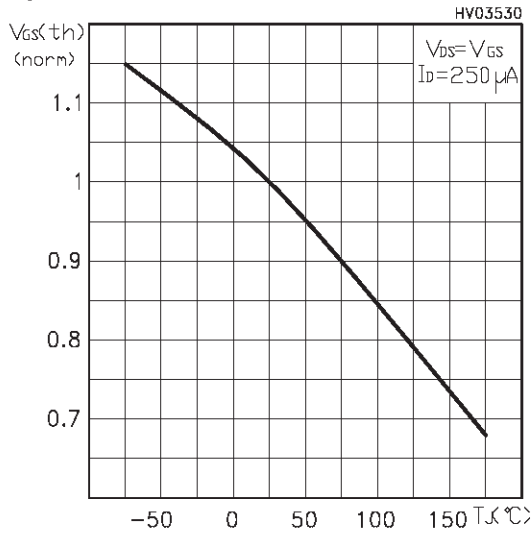
Gate Charge vs Gate-source Voltage



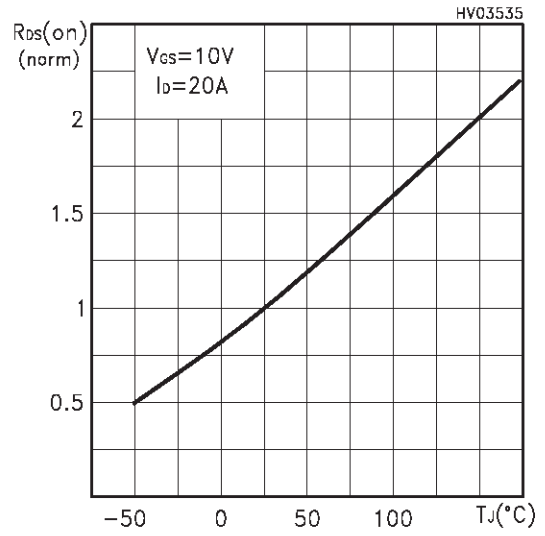
Capacitance Variations



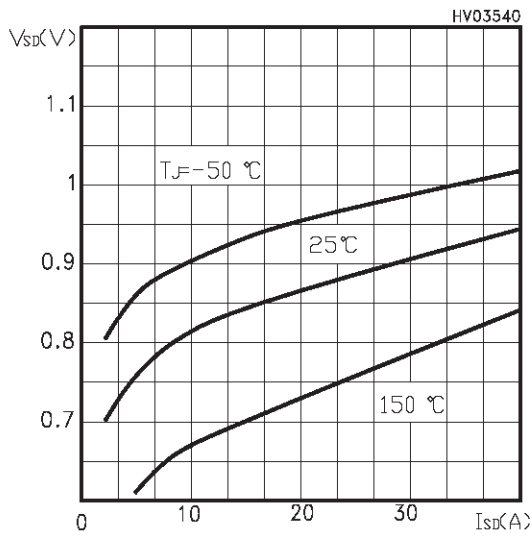
Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Drain-Source Breakdown vs Temperature

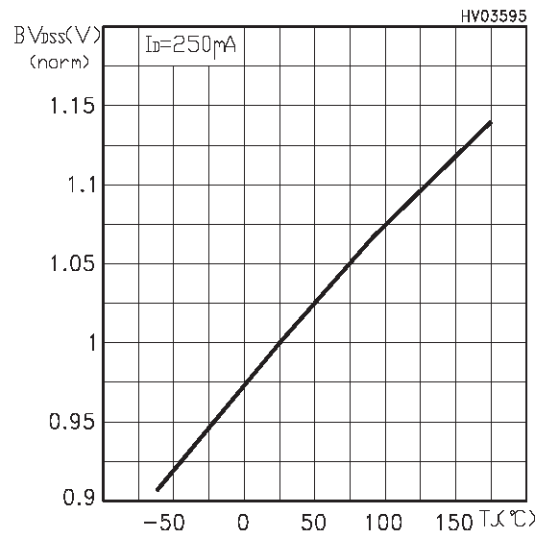


Fig. 1: Unclamped Inductive Load Test Circuit

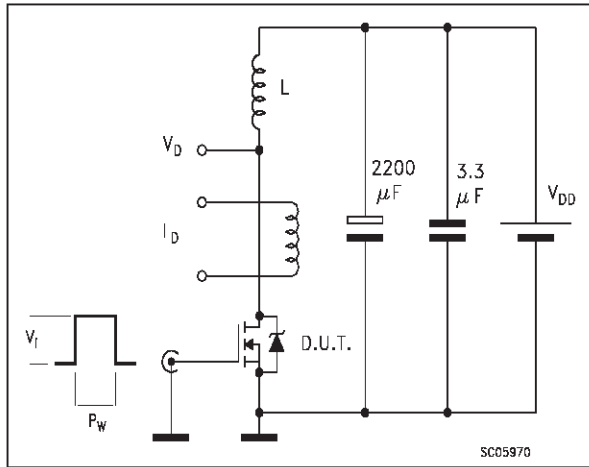


Fig. 2: Unclamped Inductive Waveform

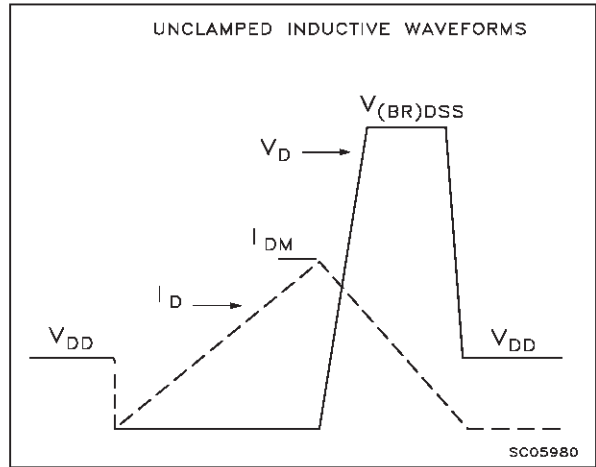


Fig. 3: Switching Times Test Circuit For Resistive Load

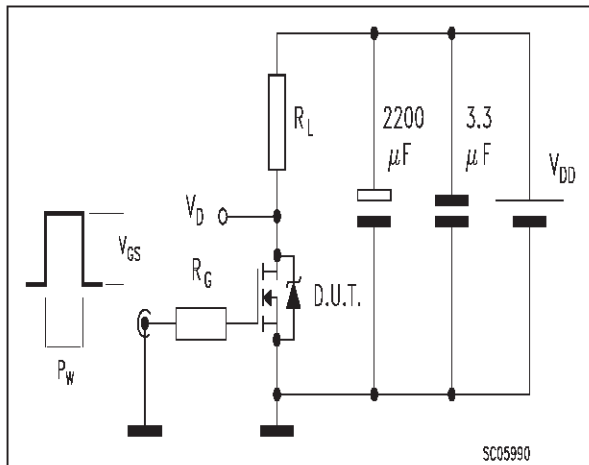


Fig. 4: Gate Charge test Circuit

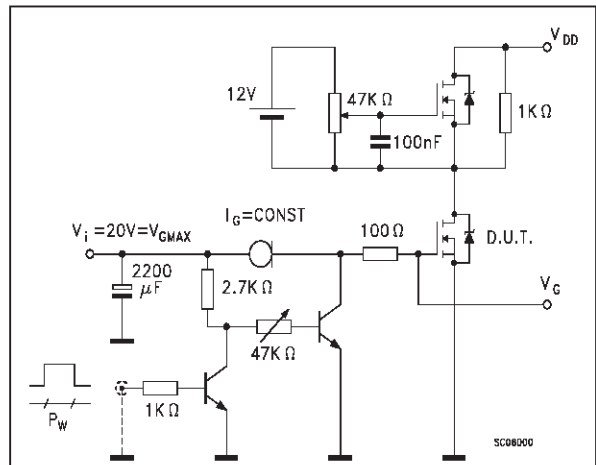
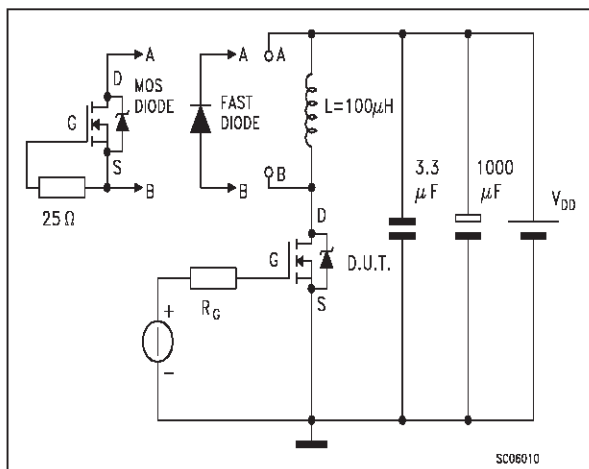
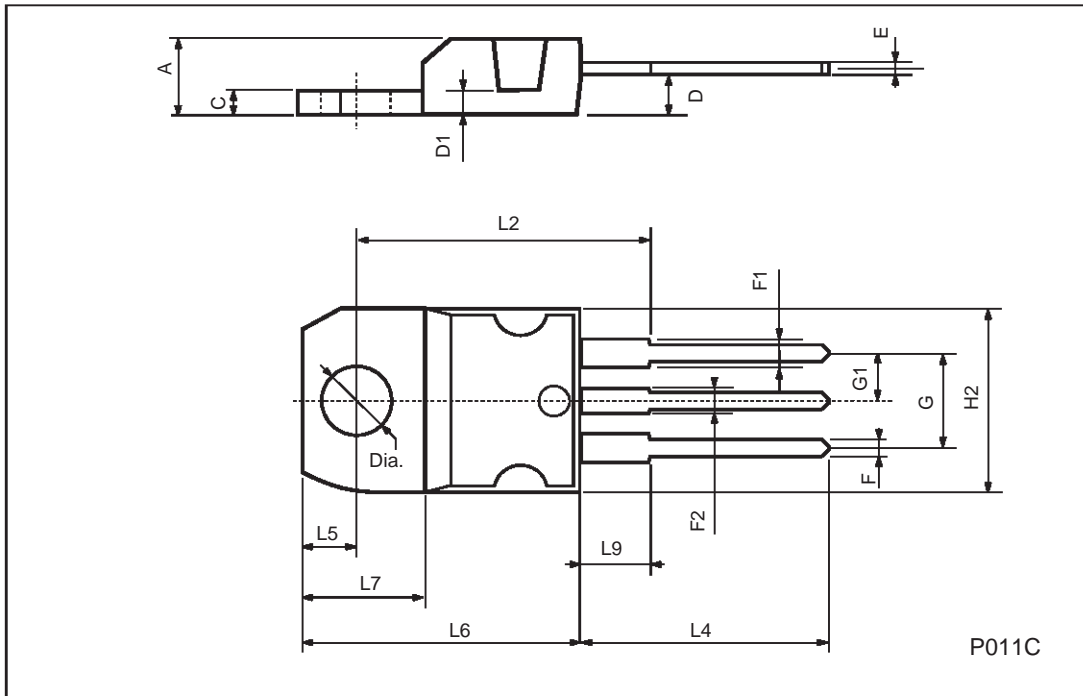


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



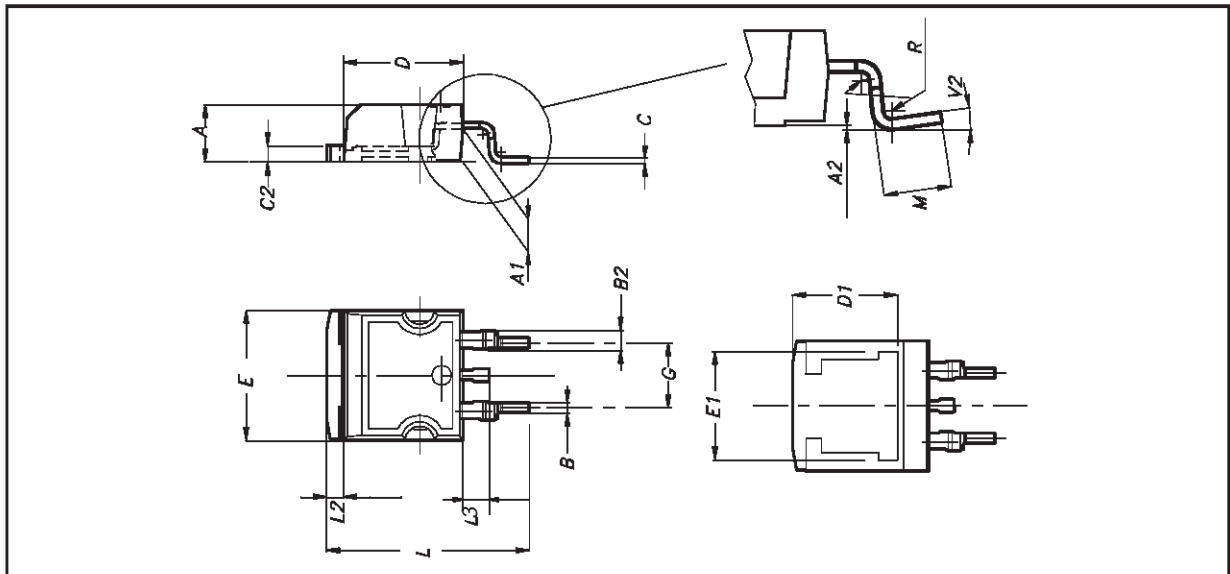
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151

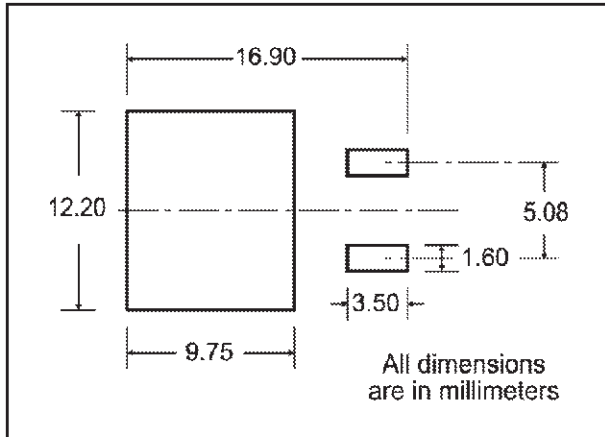


D²PAK MECHANICAL DATA

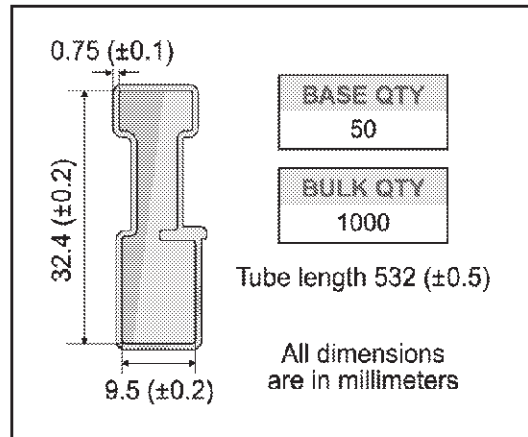
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

Diagram showing the tape mechanical data. It includes a circular reel view with dimensions A, B, C, D, and G. A 40 mm min. access hole is located at the slot location. The tape slot in the core has a 2.5 mm min. width. The full radius is indicated. A side view shows dimensions T, N, and G measured at the hub.

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

Diagram showing the reel mechanical data. It includes a side view of the reel with dimensions K₀, Y, D, P_y, P_t, E, F, w, B₀, A₀, P₁, and Center line of cavity. A note indicates a 10 pitches cumulative tolerance on tape of ±0.2 mm. A top view shows the TRL (Top Reel Layer) and the FEED DIRECTION. A bending radius diagram shows R min.

* on sales type



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