TDA3301B

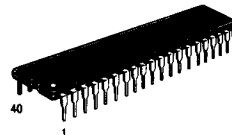**TV COLOR PROCESSOR**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

TV COLOR PROCESSOR

This device will accept a PAL or NTSC composite video signal and output the three color signals, needing only a simple driver amplifier to interface to the picture tube. The provision of high bandwidth on-screen display inputs makes it suitable for text display, TV games, cameras, etc. The TDA3301B has user control laws, and also a phase shift control which operates in PAL, as well as NTSC.

- Automatic Black Level Setup
- Beam Current Limiting
- Uses Inexpensive 4.43 MHz to 3.58 MHz Crystal
- No Oscillator Adjustment Required
- Three OSD Inputs Plus Fast Blanking Input
- Four DC, High Impedance User Controls
- Interfaces with TDA33030B SECAM Adaptor
- Single 12 V Supply
- Low Dissipation, Typically 600 mW

**P SUFFIX
PLASTIC PACKAGE
CASE 711**

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PIN CONNECTIONS

Chroma Input	1		40	Hue Control/NTSC Switch
ACC Capacitor	2		39	+ 12 V
Chroma DL Driver, Emitter	3		38	Ground
Chroma DL Driver, Collector	4		37	1.0 V Composite Video Input
Saturation Control	5		36	Delayed Luma input
Identification Capacitor	6		35	Luma DL Drive and 3.0 Inverted Output
V Input	7		34	Luma Emitter Load
U Input	8		33	Luma Collector Load
90° Loop Capacitor	9		32	Contrast Control
Oscillator Loop Filer	10		31	Black Level Clamp
Crystal Drive	11		30	Brightness Control
Drystal Feedback	12		29	Peak Beam Limit Adjust
Ground	13		28	Frame Pulse Input
Blue Output	14		27	Sandcastle Pulse Input
Blue Output Clamp Capacitor	15		26	OSD Input Green
Blue Output Feedback	16		25	OSD Input Red
Green Output	17		24	OSD Input Blue
Green Output Clamp Capacitor	18		23	OSD Input Fast Blanking
Green Output Feedback	19		22	Red Output Feedback
Red Output	20		21	Red Output Clamp Capacitor

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MAXIMUM RATINGS (T$_A$ = + 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage (Pin 39)	V$_{CC}$	14	Vdc
Operating Temperature Range	T$_A$	0 to + 70	°C
Storage Temperature Range	T$_{stg}$	–65 to +150	°C

ELECTRICAL CHARACTERICISTICS (T$_A$ = 25°C, V$_{CC}$ = 12 V)

Characteristics	Pin	Min	Typ	Max	Unit
Supply Voltage	39	10.8	12	13.2	V
Supply Current		—	45	60	mA
Composite Video Input	37	—	1.0	—	Vp-p
Video Input Resistance		13	18	23	kΩ
Video Gain to Pin 35		2.7	3.2	3.6	Vp-p
Input Window		0.8–3	0.7–3.2	—	V
Chrome Input (Burst)	1	10	100	200	mVp-p
Input Resistance	1	—	5.0	—	kΩ
ACC Effectiveness	4	—	1.2	3.0	dB
OSD Input	24, 25, 26	0.5	0.7	1.0	V
OSD Drive Impedance		—	—	180	Ω
OSD Frequency Response (–3.0 dB)		9.0	—	—	MHz
OSD Max Gain		—	7.2	—	
Gain Difference Between Any Two		—	—	15	%
Beam Current Ref. Threshold	16, 19, 22	1.7	2.0	2.3	V
Differential Voltage		—	—	20	mV
Beam Current Ref. Input Current		—	—	+1.5/–0.5	μA
Differential Current		—	—	1.0	
Luminance Gain Between Pin 36 and Outputs (Depends on R$_{333}$ and R$_{34}$)	14, 17, 20	—	4.7	—	
Luminance Bandwidth (–3.0 dB)		9.0	—	—	MHz
Output Resistance		120	170	300	Ω
Residual Carrier (4.43 Mc/s)		—	30	150	mVp-p
PAL Offset (H/2)		—	—	50	
Difference in Gain Between Y Input and any RGB o/p		—	5.0	—	%
U Input Sensitivity for 5.0 V Blue Output	8	—	340	—	mVp-p
Matrix Error	14, 17, 20	—	—	10	%
Oscillator Capture Range		350	—	—	Hz
U Ref. Phase Error		—	—	5.0	Degrees
V Ref. Phase Error		—	—	5.0	Degrees
Color Kill Attenuation	14, 17, 20	50	—	—	dB
Contrast Tracking OSD/Luma/Chroma	14, 17, 20	—	—	—	dB
OSD Contrast Tracking	14, 17, 20	—	—	±2.0	dB
OSD Enable Slice Level	23	—	0.7	—	V
Sandcastle Slice Level	27				
Burst Gate		6.5	7.2	8.0	V
Line Blanking		2.0	2.6	3.0	
R Input V$_{27}$ > 7.0 V		—	5.0	—	kΩ
V$_{27}$ < 7.0 V		—	22	—	
Frame Slice Level	28	2	2.8	3.6	V
R Input		—	15	—	kΩ
Peak Beam Limiter Threshold (I$_{29}$ Min = 250 μA)		3.4 x I$_{29}$	4 x I$_{29}$	4.6 x I$_{29}$	
Pin 29 Input Resistance	29	—	5.0	—	kΩ
Pin 29 Open Circuit Voltage	29	—	10.6	—	V

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INPUT/OUTPUT FUNCTIONS

Figure 1. Brillance Control
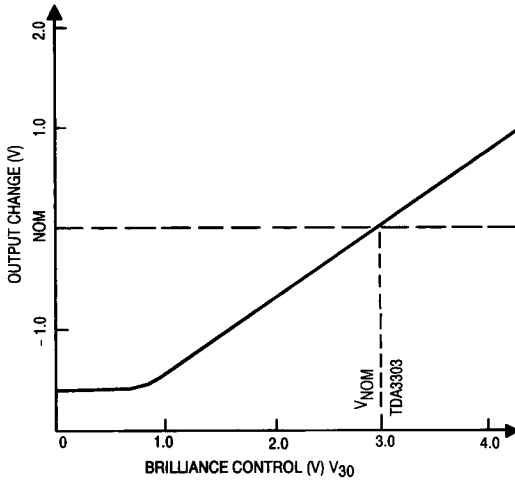
The brilliance control operates by adding a pedestal to the output signals. The amplitude of the pedestal is controlled by Pin 30.

During CRT beam current sampling a standard pedestal is substituted, its value being equivalent to the value given by V_{30} Nom Brightness at black level with V_{30} Nom is given by the sum of three gun currents at the sampling level, i.e. $3 \times 20 \mu A$ with 100 k reference resistors on Pins 16, 19, and 22.

During picture blanking the brilliance pedestal is zero; therefore, the output voltage during blanking is always the minimum brilliance black level (Note: Signal channels are also gain blanked).

Figure 2. Saturation Control Voltage
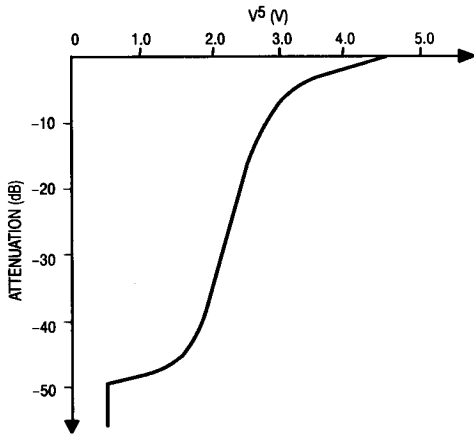
Note: Nominal 100% saturation point is given by choice of R_2 which sets ACC operating point.
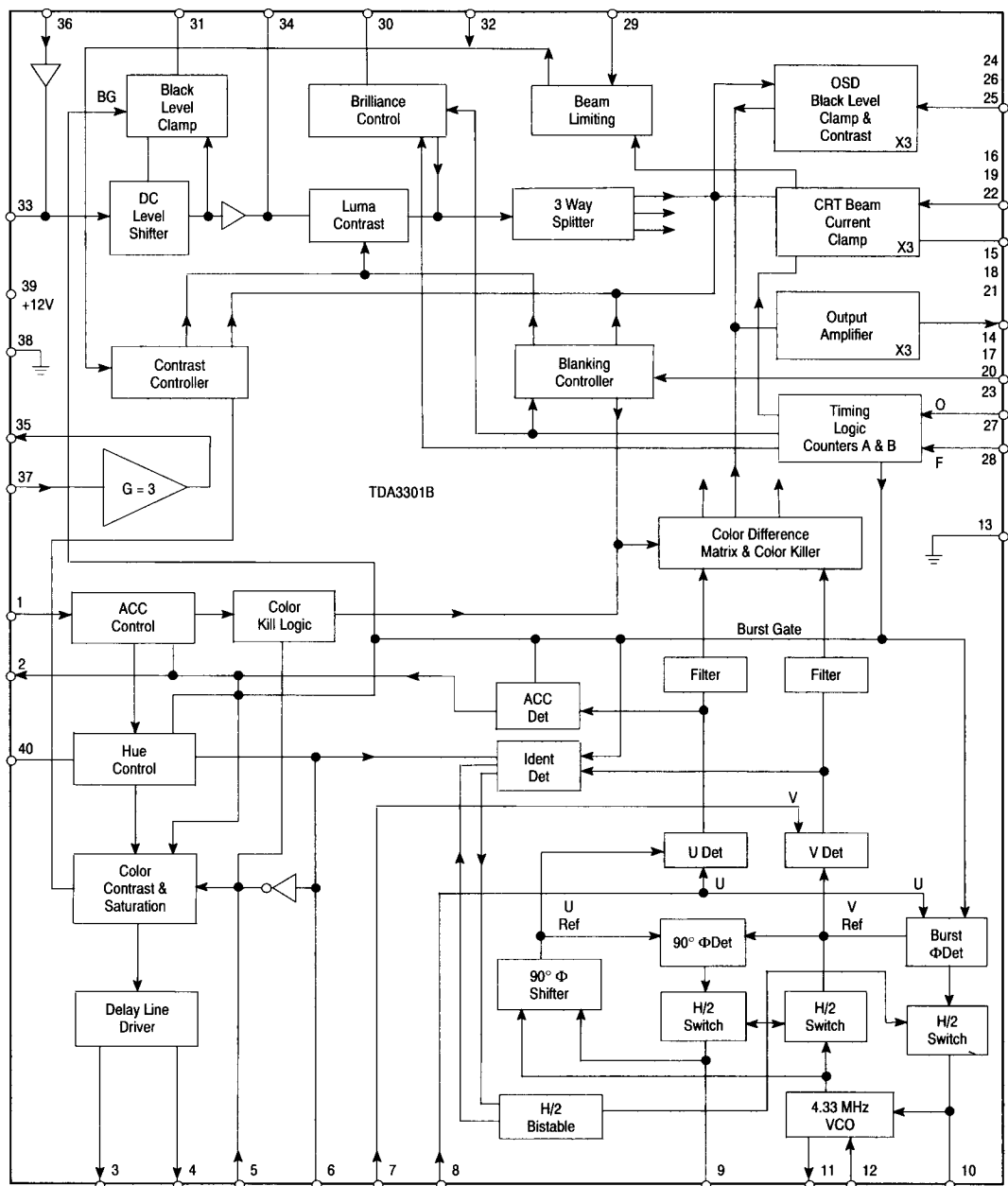Pin 5 is automatically pulled to ground with a misidentified PAL signal.

Figure 3. Contrast Control
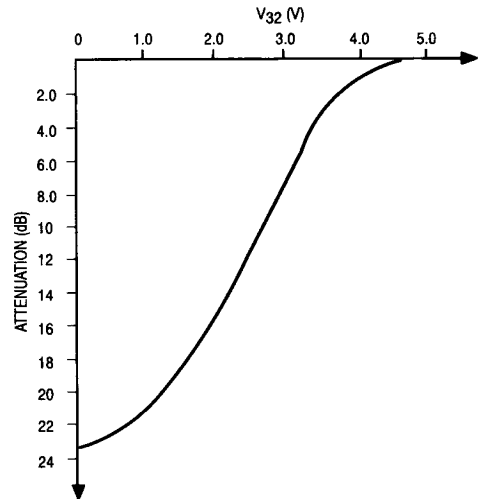
Note: Pin 32 is pulled down by the operation of the peak beam limiter.
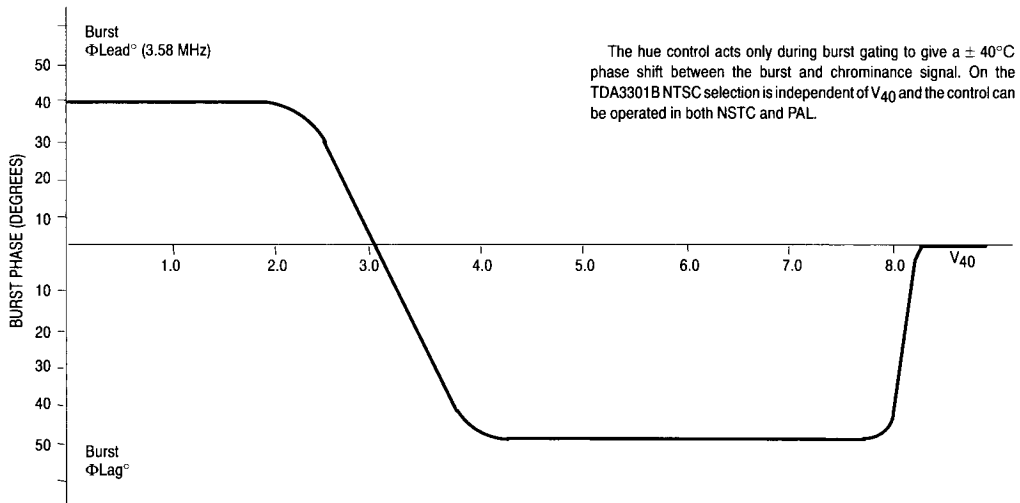
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Figure 4. Block Diagram

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Figure 5. Hue Control

Burst
ΦLead° (3.58 MHz)

The hue control acts only during burst gating to give a ± 40°C phase shift between the burst and chrominance signal. On the TDA3301B NTSC selection is independent of V_{40} and the control can be operated in both NSTC and PAL.

Burst
ΦLag°

CIRCUIT OPERATION

Chrominance Decoder

The chrominance decoder section of the TDA3301B consists of the following blocks:

Phase-locked reference oscillator; Figures 6, 7 and 8.
Phase-locked 90 degree servo loop; Figures 8 and 9.
U and V axis decoders
ACC detector and identification detector; Figure 10.
Identification circuits and PAL bistable; Figure 11.
Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

- A minimum number of factory adjustments,
- A minimum number of external components,
- Compatibility with SECAM adapter TDA3030B,
- Low dissipation,
- Use of a standard 4.433618 Mhz crystal rather than a 2.0 fc crystal with a divider.

Reference Regeneration

The crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. A great deal of care was taken to ensure that the oscillator loop gain and the crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade crystal (crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

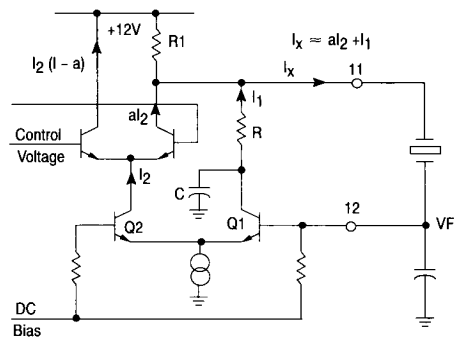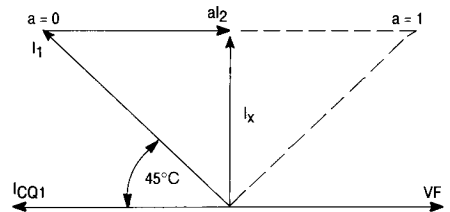### Figure 6. Voltage Controlled Osscillator (VCO)

Figure 7. Vector Diagram for VCO

By referring to Figures 6 and 7 it can be seen that the necessary $\pm 45°C$ phase shift is obtained by variable addition of two currents I_1 and I_2 which are then fed into the load resistance of the crystal tuned circuit R_1. Feedback is taken from the crystal load capacitance which gives a voltage of VF lagging the crystal current by 90°.

The RC network in the T_1 collector causes I_1 to lag the collector current of T_1 by 45°.

For SECAM operation, the currents I_1 and I_2 are added together in a fixed ratio giving a frequency close to nominal.

When decoding PAL there are two departures from normal chroma reference regeneration practice:

a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification

b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not dc. A commutator at the phase detector output also driven from the PAL bistable coverts this ac signal to a dc prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC this cannot be considered to be a serious disadvantage.

Figure 8. Block Diagram of Reference Section
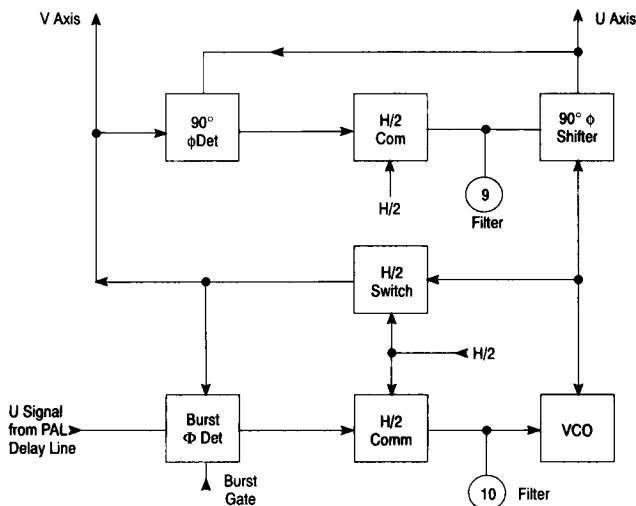
90° Reference Generation

To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the variable all-pass network (see Figure 9).

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B adapter.
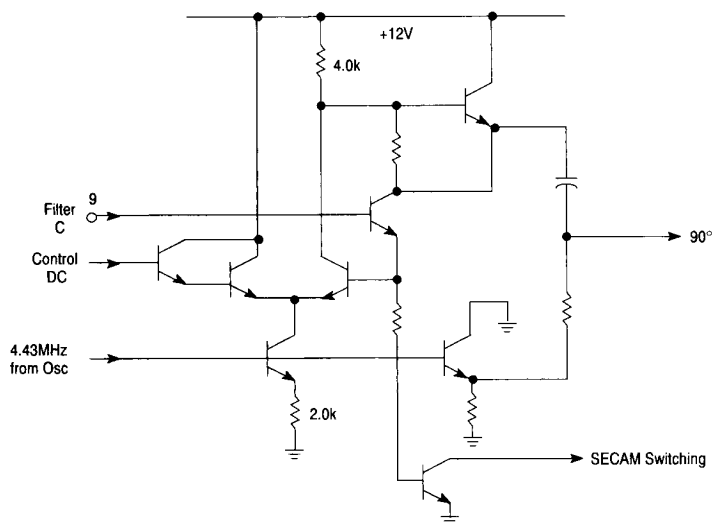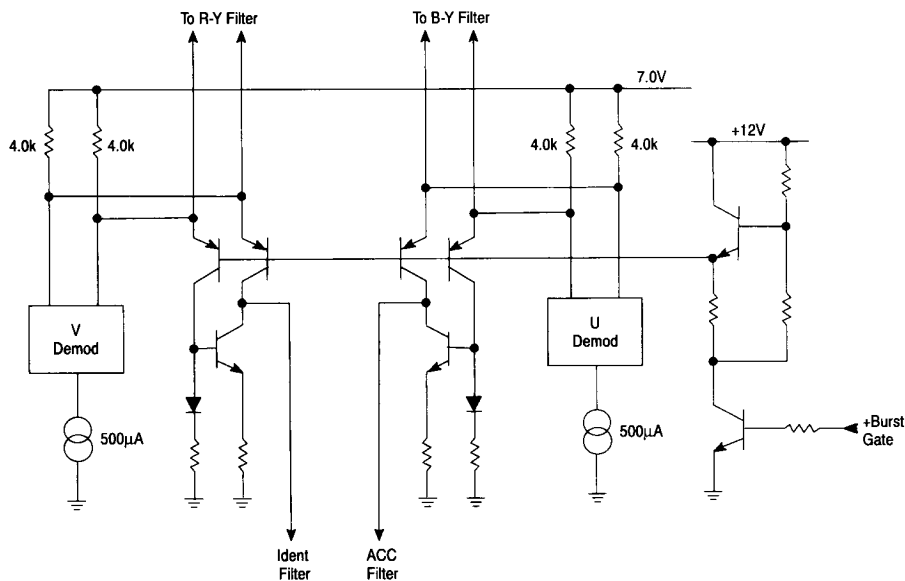
Figure 9. Variable All-Pass Network

Figure 10. ACC and Identification Detectors

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ACC and Identification Detectors

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push-pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

Identification

See Figure 11 for definitions.

Monochrome $\quad I_1 > I_2$
PAL Ident. OK $\quad I_1 < I_2$
PAL Ident. X $\quad I_1 > I_2$
NTSC $\qquad\quad I_3 > I_2$

Only for correctly identified PAL signal is the capacitor voltage held low since I_2 is then greater than I_1.

For monochrome and incorrectly identified PAL signals $I_1 > I_2$ hence voltage V_C rises with each burst gate pulse.

When $V_{ref}1$ is exceeded by 0.7 V Latch 1 is made to conduct which increases the rate of voltage rise on C. Maximum current is limited by R_1.

When $V_{ref}2$ is exceeded by 0.7 V then Latch 2 is made to conduct until C is completely discharged and the current drops to a value insufficient to hold on Latch 2.

As Latch 2 turns on Latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

The inhibit line on Latch 2 restricts its conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing Latch 2 in the correct phase for SECAM. For NTSC, Latch 2 is fired by a current injected on Pin 6.

If the voltage on C is greater than 1.4 V, then the saturation is held down. Only for SECAM/NTSC with Latch 2 on, or correctly identified PAL, can the saturation control be anywhere but minimum.

NTSC Switch

NTSC operation is selected when current (I_3) is injected into Pin 6. On the TDA3301B this current must be derived externally by connecting Pin 6 to +12 V via a 27 k resistor (as on TDA3300B). For normal PAL operation Pin 40 should be connected to +12 V and Pin 6 to the filter capacitor.

Figure 11. Identification Circuit
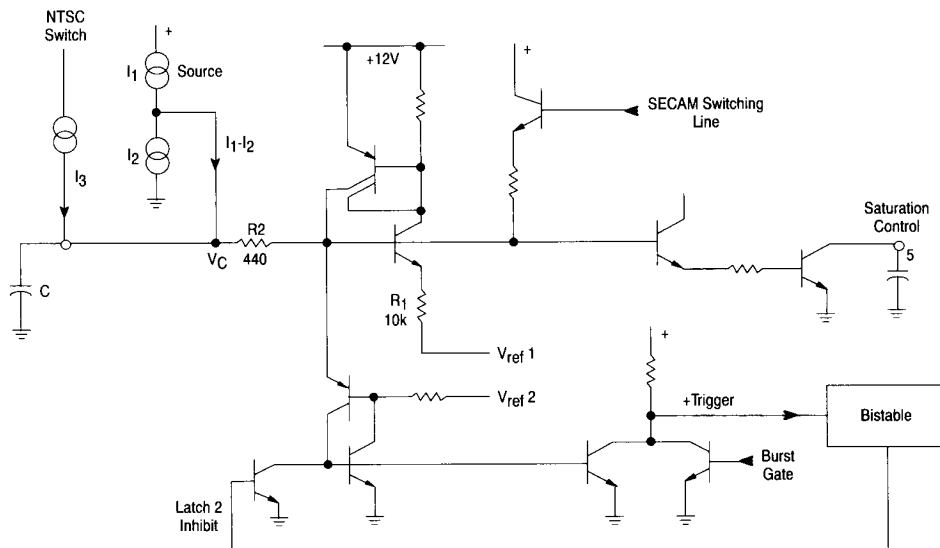
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Color Difference Matrixing, Color Killing, and Chroma Blanking

During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

The color difference matrixing is performed by two differential amplifiers, each with one side split to give the correct values of the −(B-Y) and −(R-Y) signals. These are added to give the (G-Y) signal.

The three color difference signals are then taken to the virtual grounds of the video output stages together with luminance signal.

Sandcastle Selection

The TDA3301B may be used with a two level sandcastle and a separate frame pulse to Pin 28, or with only a three level (super) sandcastle. In the latter case, a resistor of 1.0 MΩ is necessary from + 12 V to Pin 28 and a 470 pF capacitor from Pin 28 to ground.

Figure 12. Color Difference Stages

Figure 13. Timing Diagram

Frame Pulse F (V28)

Sandcastle L (V27)

Clock To A

Counter A Output

Counter B Output

CRT Sample Time S
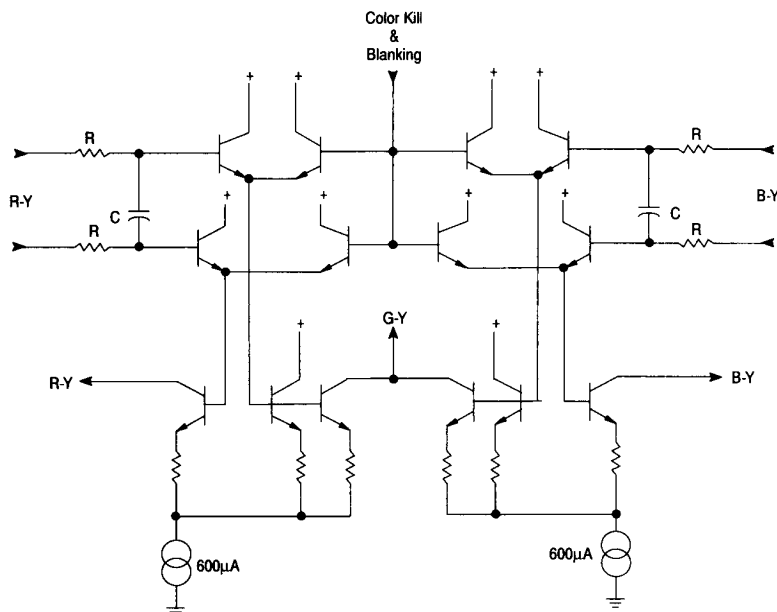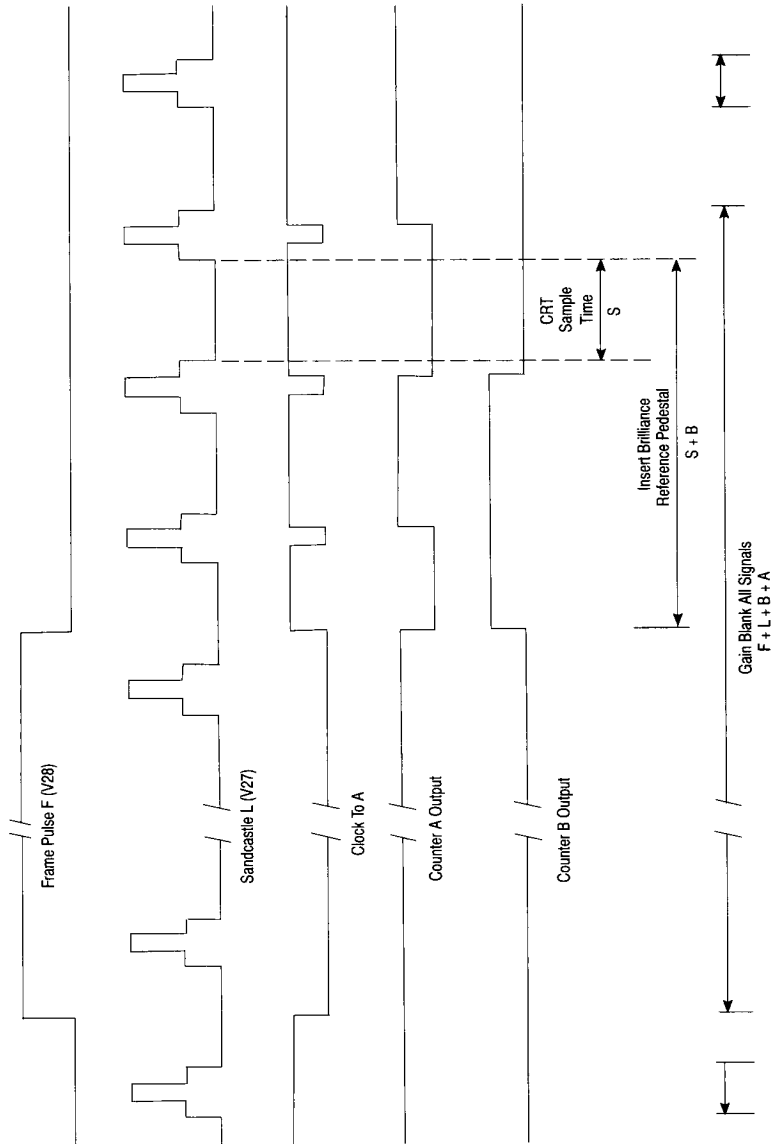
Insert Brilliance Reference Pedestal
S + B

Gain Blank All Signals
F + L + B + A

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Timing Counter for Sample Control

In order to control beam current sampling at the beginning of each frame scan, two edge triggered flip-flops are used.

The output $\overline{A}$ of the first flip-flop A is used to clock the second flip-flop B. Clocking of A by the burst gate is inhibited by a count of $A.\overline{B}$.

The count sequence can only be initiated by the trailing edge of the frame pulse. In order to provide control signals for:

Luma/Chroma blanking
Beam current sampling
On-screen display blanking
Brilliance control

The appropriate flip-flop outputs ar matrixed with sandcastle and frame signals by an emitter-follower matrix.

Figure 14. Timing Counter
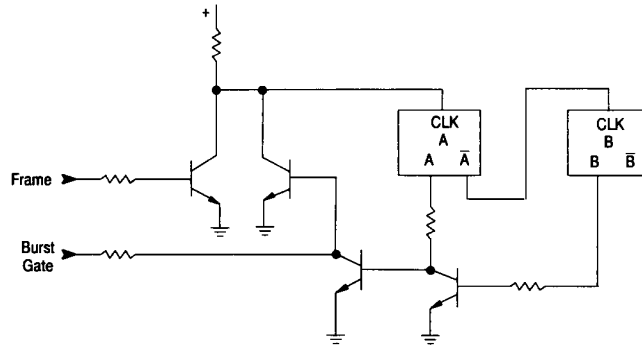
On-Screen Display Inputs

Each section of the OSD stages consists of a common emitter input stage feeding a diversion gate controlled by the contrast control. During burst gate time a feedback loop is activated which clamps the signal at the input coupling capacitor. This ensures that the current in the diversion gate is zero at black level and the OSD black level insensitive to contrast control, also the inputs ignore signals below black, e.g. sync, pulses.

Figure 15. OSD Stage
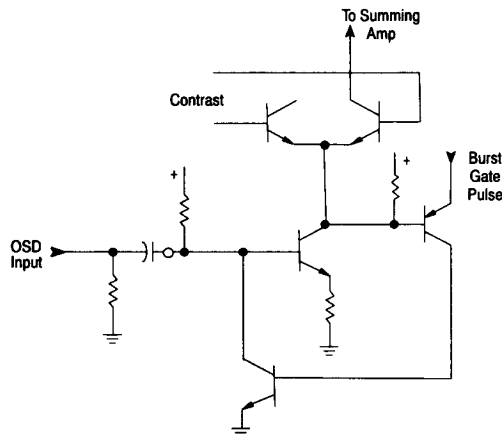
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Video Output Sections

Each video output stage consists of a feedback amplifier in which the input signal is a current drive to the virtual earth from the luminance, color difference and on-screen display stages.

A further drive current is used to control the DC operating point; this is derived from the sample and hold stage which samples the beam current after frame flyback.
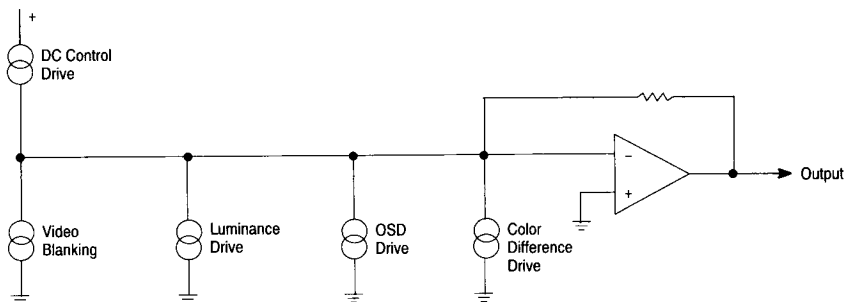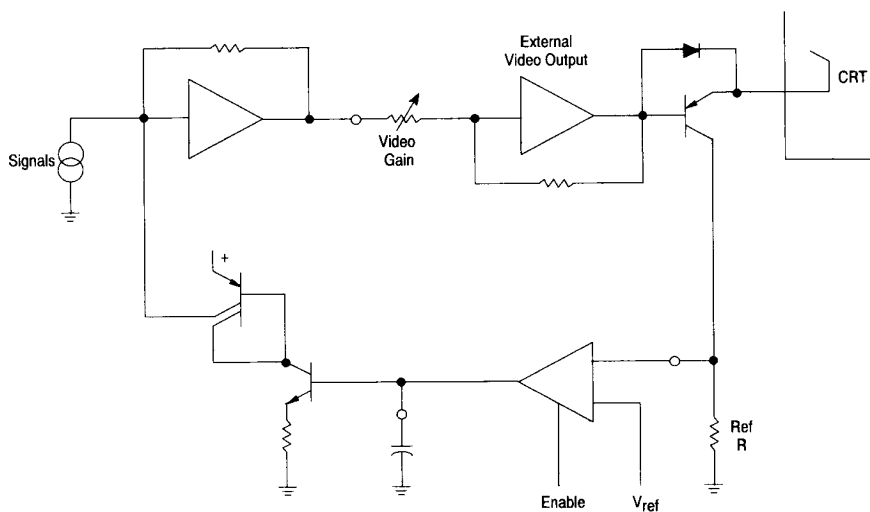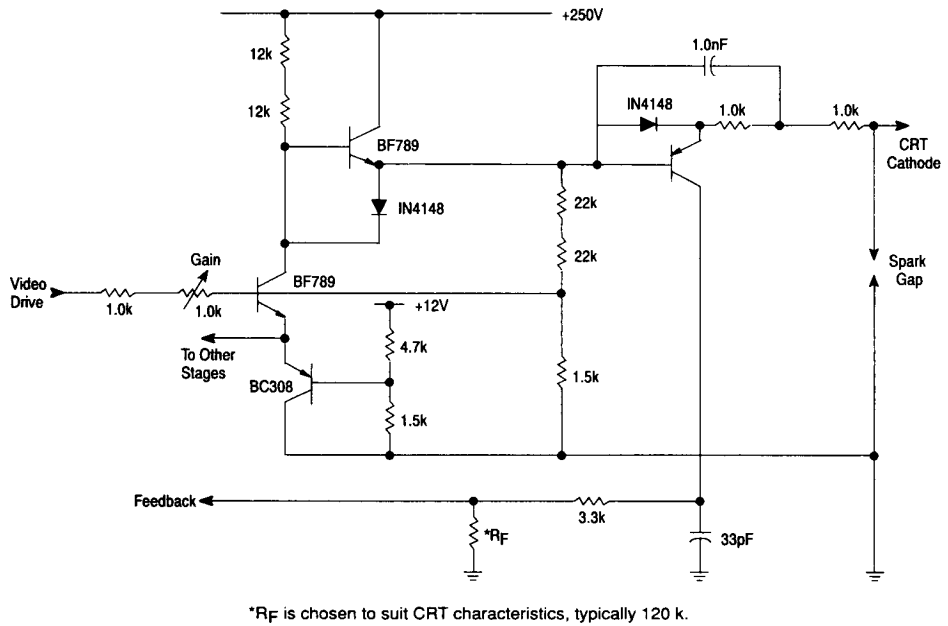
Figure 16. Video Output Section
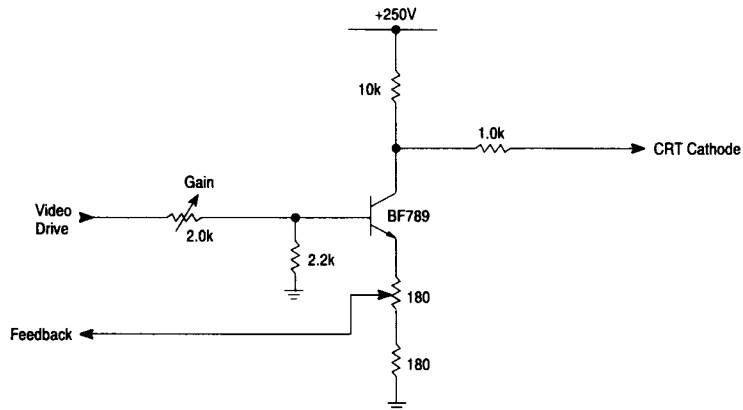

Figure 17. Complete Video Output Sections

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Figure 18. Typical Video Output Stage

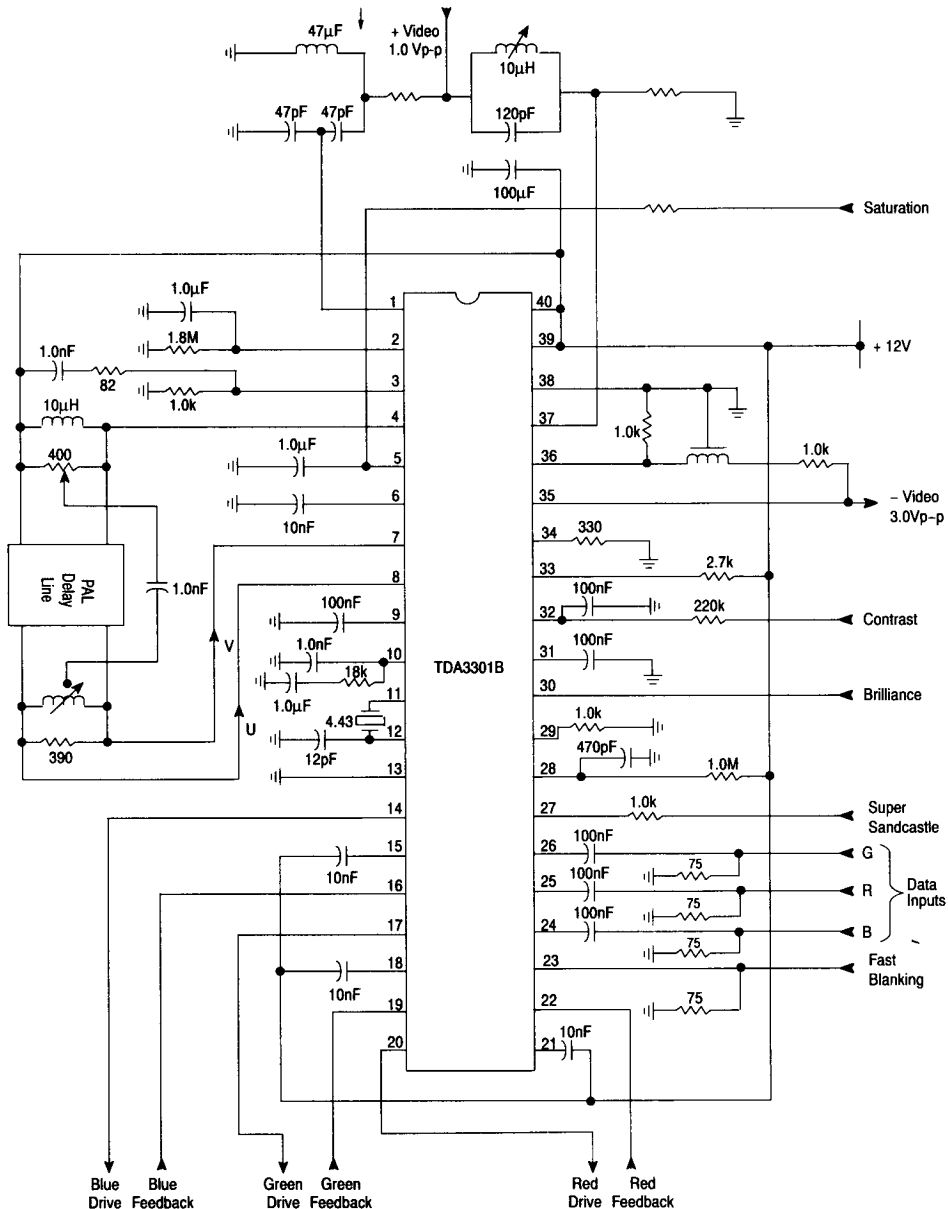*R_F is chosen to suit CRT characteristics, typically 120 k.

Figure 19. Class A Video Output Stage with Direct Feedback

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Figure 20. Typical PAL Application

NOTE: When not using Super Sandcastle a positive vertical blanking pulse must be applied to Pin 28.