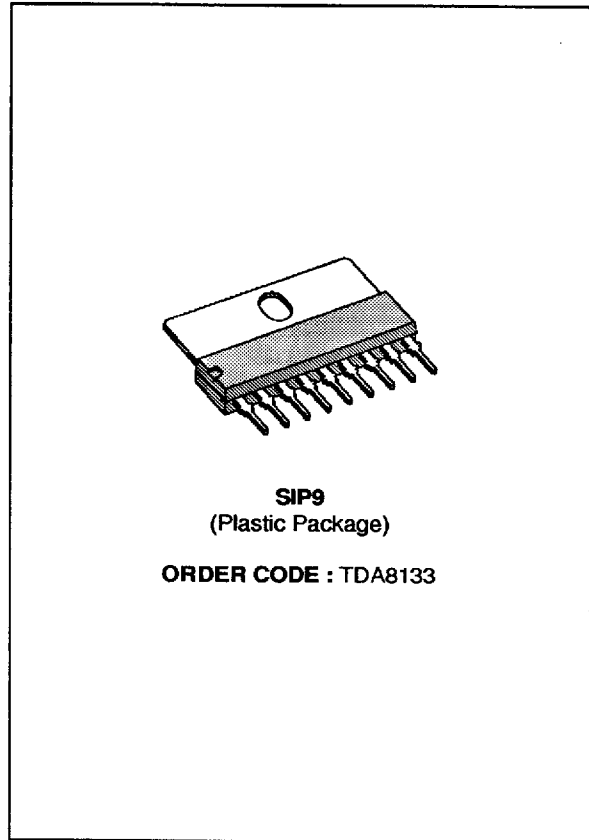


**5.1V +8V REGULATOR WITH DISABLE AND RESET**

ADVANCE DATA

- OUTPUT CURRENTS UP TO 0.75A
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 8V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE



**DESCRIPTION**

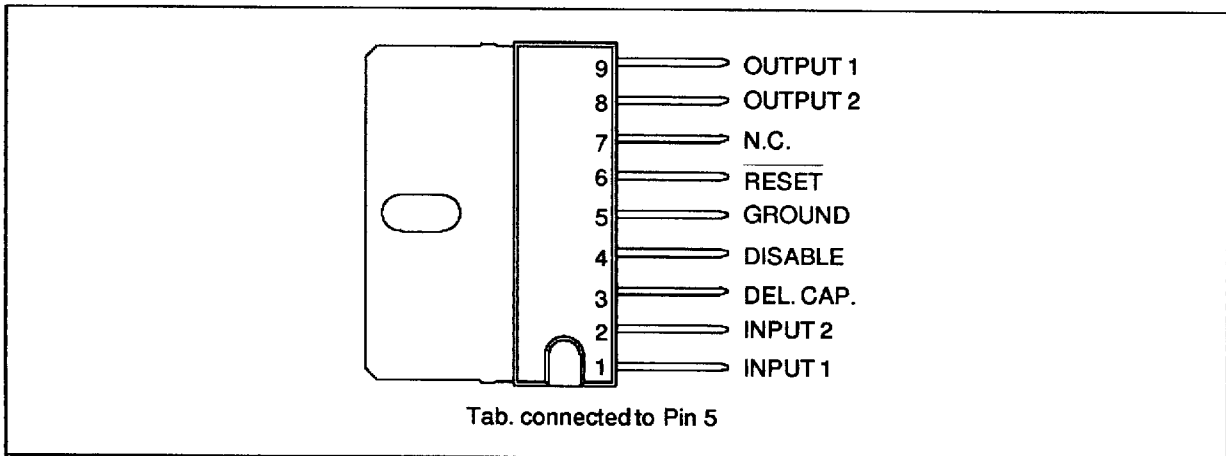
The TDA8133 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 8V at currents up to 0.75A.

An internal reset circuit generates a reset pulse when the output 1 decrease below the regulated voltage value.

Output 2 can be disabled by TTL input.

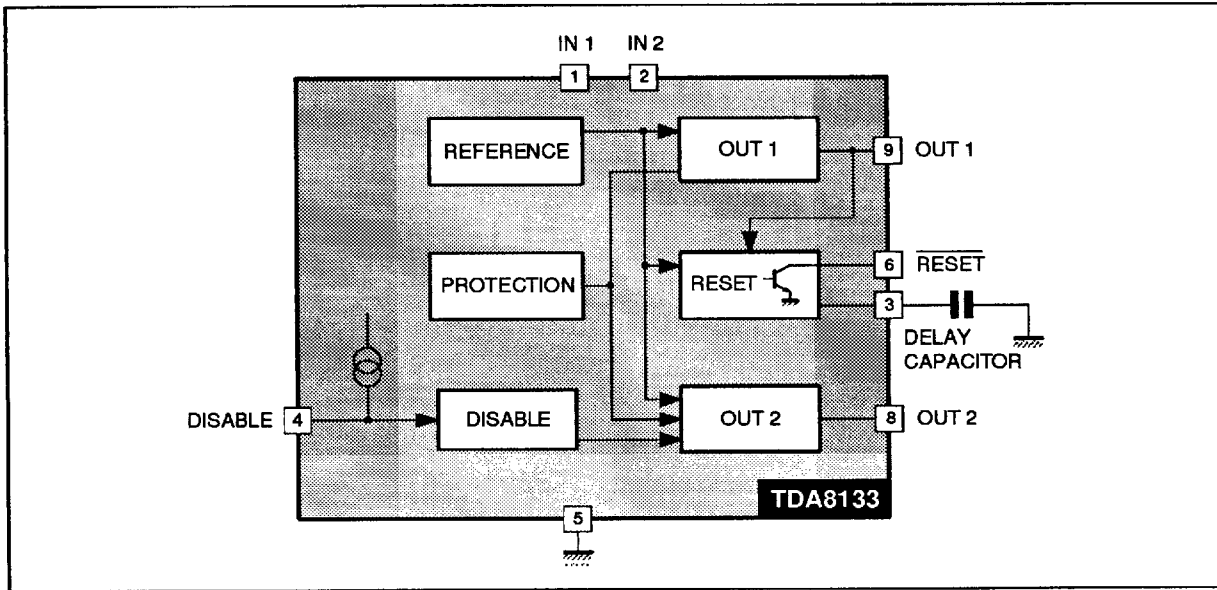
Short circuit and thermal protections are included in all the versions.

**PIN CONNECTIONS**



8133-01/EP8

**BLOCK DIAGRAM**



8133-02.EPS

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{IN}$	DC Input Voltage Pin 1	20	V
$V_{DIS}$	Disable Input Voltage	20	V
$V_{RST}$	Output Voltage at Pin 6	20	V
$I_{O1,2}$	Output Currents	Internally Limited	
$P_t$	Power Dissipation	Internally Limited	
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_j$	Junction Temperature	0 to +150	°C

8133-01.TEL

**THERMAL DATA**

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Maximum Thermal Resistance Junction-case	8	°C/W
$R_{th(j-a)}$	Maximum Thermal Resistance Junction-ambient	60	°C/W
$T_j$	Maximum Recommended Junction Temperature	130	°C

8133-02.TEL

**ELECTRICAL CHARACTERISTICS** ( $V_{IN1} = 7V$ ,  $V_{IN2} = 10V$ ,  $T_j = 25^\circ C$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{O1}$	Output Voltage	$I_{O1} = 10mA$	5	5.1	5.2	V
$V_{O2}$	Output Voltage	$I_{O2} = 10mA$	7.84	8	8.16	V
$V_{O1}$	Output Voltage	$7V < V_{IN1} < 14V$	4.9		5.3	V
$V_{O2}$	Output Voltage	$10V < V_{IN2} < 14V$ $5mA < I_{O1,2} < 750mA$	7.7		8.3	V
$V_{IO1,2}$	Dropout Voltage	$I_{O1,2} = 750mA$			1.4	V
$V_{O1,2LI}$	Line Regulation	$7V < V_{IN1} < 14V$ $10V < V_{IN2} < 14V$ $I_{O1,2} = 200mA$			50 80	mV mV
$V_{O1,2LO}$	Load Regulation	$5mA < I_{O1} < 0.6A$ $5mA < I_{O2} < 0.6A$			100 160	mV mV
$I_Q$	Quiescent Current	$I_{O1} = 10mA$ Output 2 Disabled			2	mA
$V_{O1RST}$	Reset Threshhold Voltage	$K = V_{O1}$	K - 0.4	K - 0.25	K - 0.1	V
$V_{RTH}$	Reset Threshhold Hysteresis	See circuit description	20	50	75	mV
$t_{RD}$	Reset Pulse Delay	$C_e = 100nF$ See circuit description		25		ms
$V_{RL}$	Saturation Voltage in Reset Condition	$I_S = 5mA$			0.4	V
$I_{RH}$	Leakage Current in Normal Condition at Pin 6	$V_5 = 10V$			10	$\mu A$
$K_{O1,2}$	Output Voltage Thermal Drift	$T_j = 0$ to $125^\circ C$ $K_O = \frac{\Delta V_O \cdot 10^6}{\Delta T \cdot V_O}$		100		ppm/ $^\circ C$
$I_{O1,2SC}$	Short Circuit Output Current	$V_{IN1} = 7V$ , $V_{IN2} = 10V$ $V_{IN1,2} = 16V$ (see Note)			1.6 1	A A
$V_{DISH}$	Disable Voltage High (out 2 active)		2			V
$V_{DISL}$	Disable Voltage Low (out 2 disabled)				0.8	V
$I_{DIS}$	Disable Bias Current	$0V < V_{DIS} < 7V$	-100		2	$\mu A$
$T_{jSD}$	Junction Temperature for Thermal Shut Down			145		$^\circ C$

8133-03.TBL

**Note** : Safe permanent short-circuit is only guaranteed for input voltages up to 16V.

**CIRCUIT DESCRIPTION**

The TDA8133 is a dual voltage regulator with Reset and Disable.

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.

Since the supply voltage of this last is connected at Pin 1 ( $V_{IN1}$ ), the regulator 2 will not work if Pin 1 is not supplied.

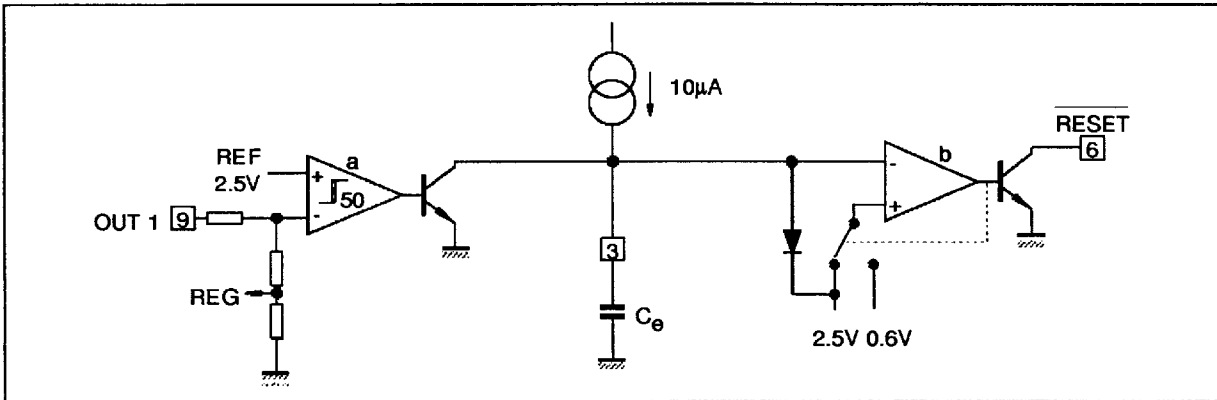
The outputs stage have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at Pin 4.

The Reset circuit checks the voltage at the output 1. If this one goes below  $V_{OUT} - 0.25V$  (4.85V typ.), the comparator "a" (see Figure 1) discharges rapidly the capacitor  $C_e$  and the reset output goes at once Low. When the voltage at the out1 rises above  $V_{OUT} - 0.2V$  (4.9V typ.), the voltage  $V_{C_e}$  increases linearly to 2.5V corresponding to a delay  $t_d$  following the law :  $t_1 = \frac{C_e \cdot 2.5V}{10\mu A}$  (see Figure 2),

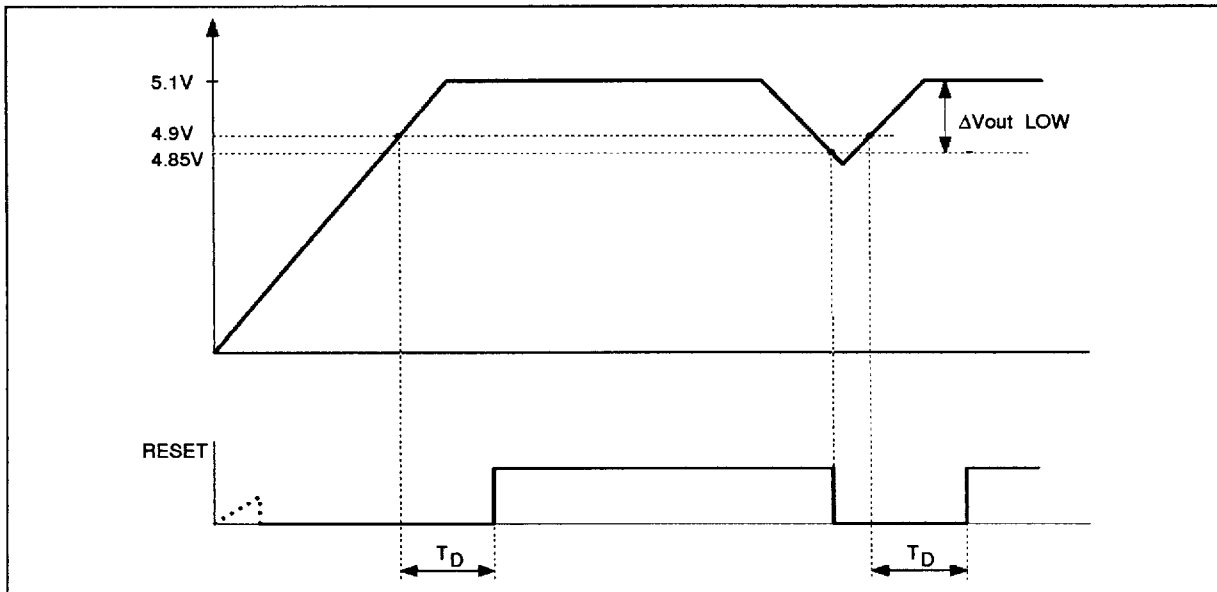
then the reset output goes high again. To avoid glitches in the reset output, the second comparator "b" has a large hysteresis (1.9V).

Figure 1



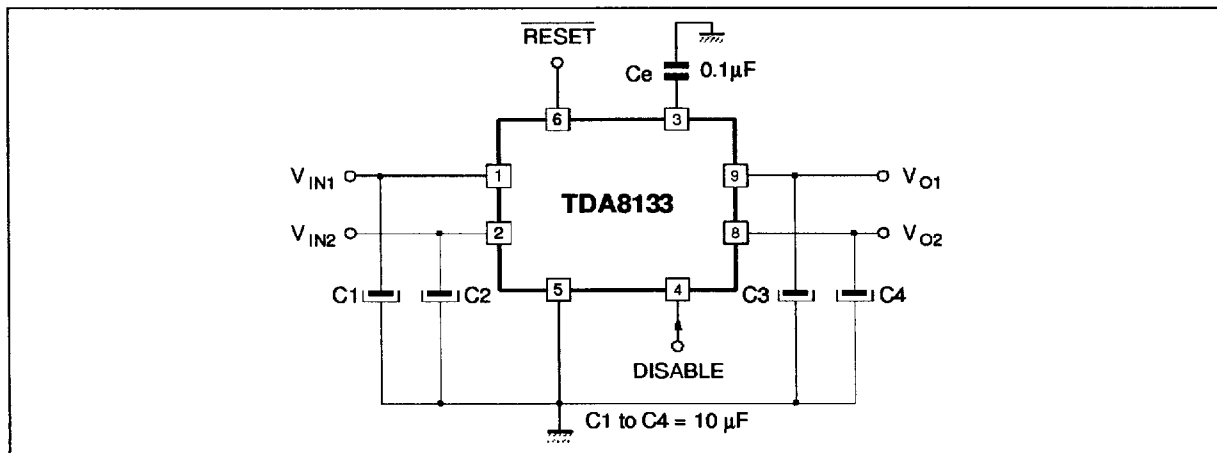
8133-03.EPS

Figure 2

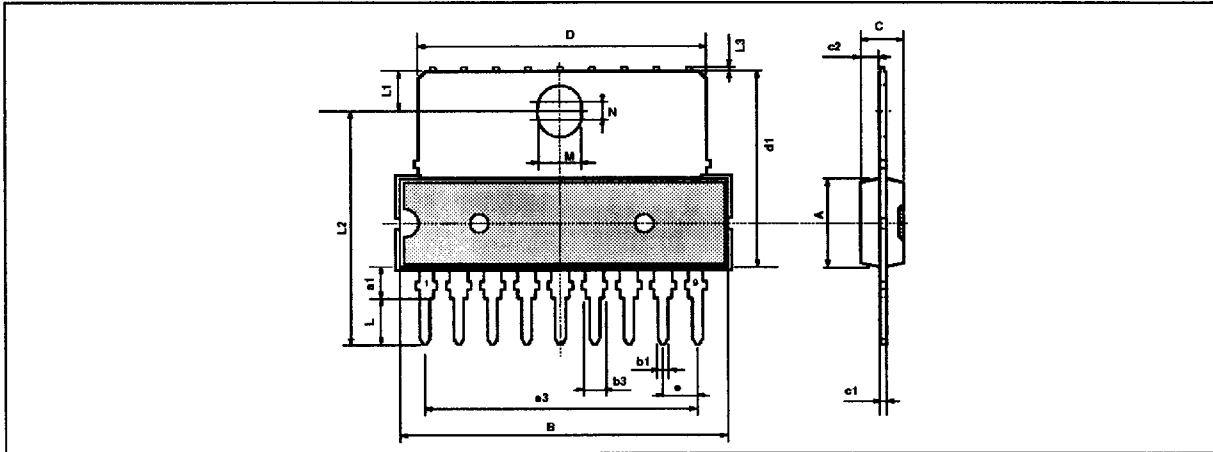


8133-04.EPS

TYPICAL APPLICATION



8133-05.EPS

**PACKAGE MECHANICAL DATA**  
**9 PINS - PLASTIC SIP**


PM-SIP9.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

SIP9.TEL

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