DATA SHEET

TDA9808
Single standard VIF-PLL with QSS-IF and FM-PLL demodulator

Product specification
Supersedes data of 1999 Jan 18
File under Integrated Circuits, IC02

1999 Jun 04

Philips
Semiconductors

PHILIPS

Single standard VIF-PLL with QSS-IF and FM-PLL demodulator

TDA9808

FEATURES

- 5 V supply voltage (9 V supply voltage for TDA9808 (DIP20) only)
- Applicable for IFs (Intermediate Frequencies) of 38.9 MHz, 45.75 MHz and 58.75 MHz
- Gain controlled wide band Video IF (VIF)-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Robustness for over-modulation better than 105% due to Phase Locked Loop (PLL)-bandwidth control at negative modulated standards
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector
- Tuner AGC with adjustable TakeOver Point (TOP)
- Automatic Frequency Control (AFC) detector without extra reference circuit
- AC-coupled limiter amplifier for sound intercarrier signal
- Alignment-free FM-PLL demodulator with high linearity
- Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier; single reference QSS mixer for high performance
- Electrostatic Discharge (ESD) protection for all pins.

GENERAL DESCRIPTION

The TDA9808 is an integrated circuit for single standard (negative modulated) vision IF signal processing and FM demodulation, with single reference QSS-IF in TV and VTR sets.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9808	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
TDA9808T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	V_P = 9 V for TDA9808 (DIP20) only	4.5	5	9.9	V
I_P	supply current		71	83	95	mA
$V_{i(VIF)(rms)}$	VIF input signal voltage sensitivity (RMS value)	−1 dB video at output	–	60	100	μV
$V_{o(video)(p-p)}$	video output signal voltage (peak-to-peak value)		1.2	1.35	1.5	V
B_{-3}	−3 dB video bandwidth on pin 9	C_L < 30 pF; R_L > 1.5 kΩ; AC load	7	8	–	MHz
$S/N_{W(video)}$	weighted signal-to-noise ratio for video		56	60	–	dB
$\alpha_{IM(0.92)}$	intermodulation attenuation at ‘blue’	f = 0.92 MHz	58	64	–	dB
$\alpha_{IM(2.76)}$	intermodulation attenuation at ‘blue’	f = 2.76 MHz	58	64	–	dB
$\alpha_{H(sup)}$	suppression of harmonics in video signal		35	40	–	dB
$V_{i(SIF)(rms)}$	sound IF input signal voltage sensitivity (RMS value)	−3 dB at intercarrier output	–	50	100	μV
$V_{o(rms)}$	audio output signal voltage for FM (RMS value)	M, N standard; 25 kHz modulation	0.4	0.5	0.6	V
THD	total harmonic distortion	25 kHz modulation	–	0.15	1.0	%
$S/N_{W(audio)}$	weighted signal-to-noise ratio	25 kHz modulation; τ = 75 μs	55	60	–	dB

BLOCK DIAGRAM

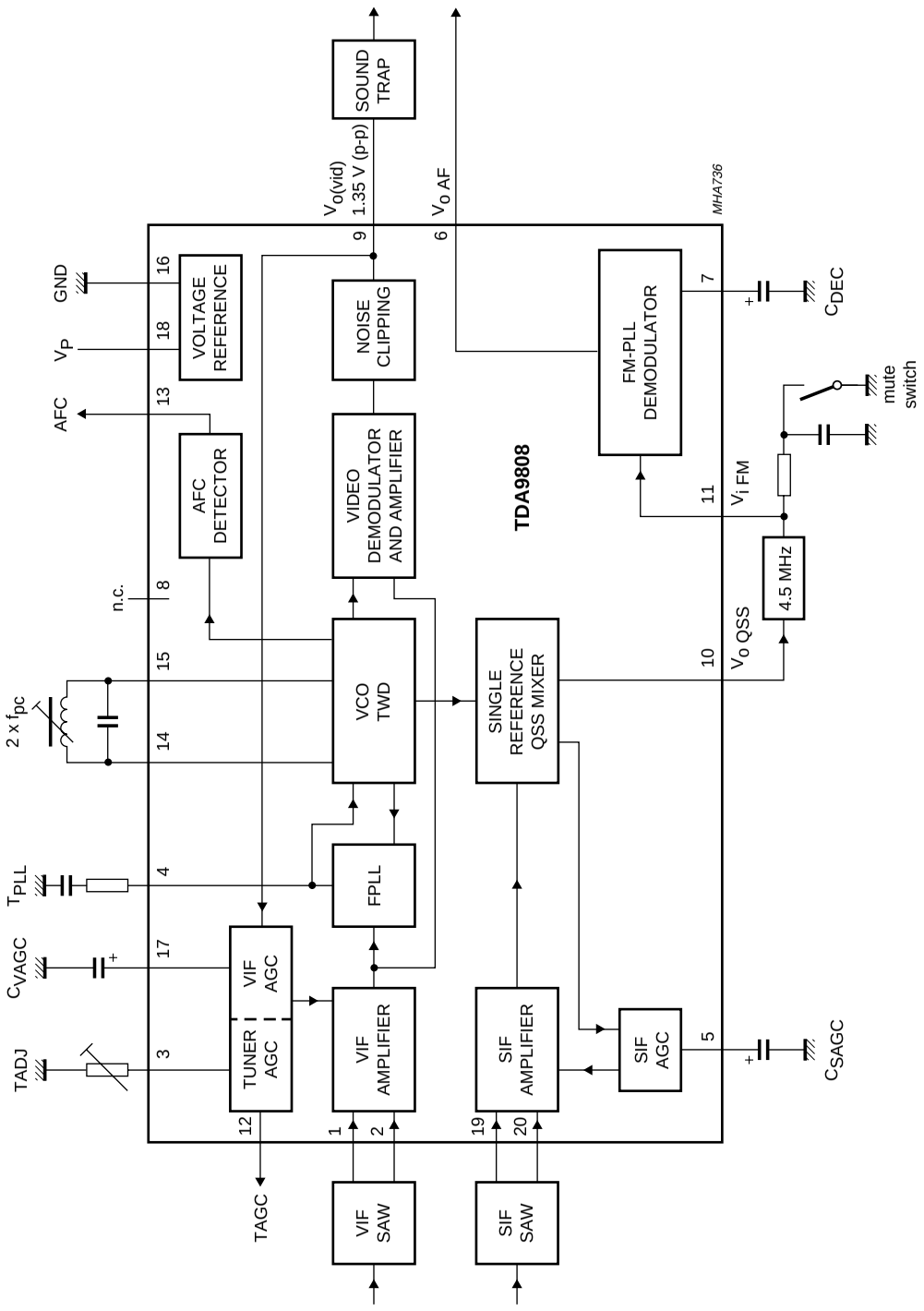


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ VIF1}$	1	VIF differential input signal voltage 1
$V_{i\ VIF2}$	2	VIF differential input signal voltage 2
TADJ	3	tuner AGC takeover point adjust
T_{PLL}	4	PLL loop filter
C_{SAGC}	5	SIF AGC capacitor
$V_{o\ AF}$	6	audio output
C_{DEC}	7	decoupling capacitor
n.c.	8	not connected
$V_{o(vid)}$	9	composite video output voltage
$V_{o\ QSS}$	10	single reference QSS output voltage

SYMBOL	PIN	DESCRIPTION
$V_{i\ FM}$	11	sound intercarrier input voltage
TAGC	12	tuner AGC output
AFC	13	AFC output
VCO1	14	VCO1 resonance circuit
VCO2	15	VCO2 resonance circuit
GND	16	ground
C_{VAGC}	17	VIF AGC capacitor
V_P	18	supply voltage
$V_{i\ SIF1}$	19	SIF differential input signal voltage 1
$V_{i\ SIF2}$	20	SIF differential input signal voltage 2

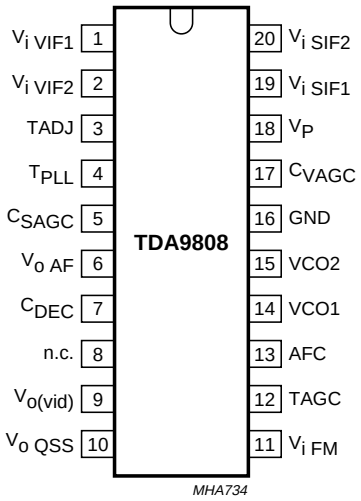


Fig.2 Pin configuration DIP20.

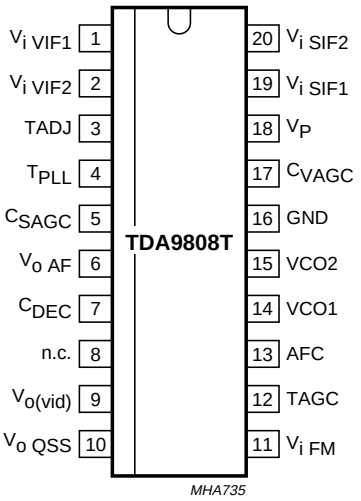


Fig.3 Pin configuration SO20.

FUNCTIONAL DESCRIPTION

The integrated circuit comprises the functional blocks as shown in Fig.1:

1. Vision IF amplifier and VIF AGC detector
2. Tuner AGC
3. Frequency Phase Locked Loop (FPLL) detector
4. Voltage Controlled Oscillator (VCO), Travelling Wave Divider (TWD) and AFC
5. Video demodulator and amplifier
6. SIF amplifier and SIF AGC
7. Single reference QSS mixer
8. FM-PLL demodulator
9. Audio Frequency (AF) signal processing
10. Internal voltage stabilizer.

Vision IF amplifier and VIF AGC detector

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration.

The AGC detector generates the required VIF gain control voltage for constant video output by charging/discharging the AGC capacitor. Therefore, for negative video modulation the synchronisation level of the video signal is detected.

Tuner AGC

The AGC capacitor voltage is converted to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current at pin TAGC (open-collector output). The tuner AGC takeover point can be adjusted at pin TADJ. This allows to match the tuner to the SAW filter in order to achieve the optimum IF input level.

Frequency Phase Locked Loop (FPLL) detector

The VIF-amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. The DC current of either the frequency detector or the phase detector is converted to a DC voltage via the loop filter, which controls the VCO frequency.

VCO, Travelling Wave Divider (TWD) and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the Picture Carrier (PC) frequency. The VCO is controlled by two integrated variable capacitors. The control voltage required to tune the VCO from its free-running frequency to double the PC frequency is generated by the frequency-phase detector of the FPLL and fed via the loop filter to the first variable capacitor. This control voltage is amplified and additionally converted into a current which represents the AFC output signal. At the centre frequency the AFC output current is equal to zero.

The oscillator signal is divided-by-two with a TWD which generates two differential output signals with a 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the ‘in phase’ signal of the travelling wave divider output.

The demodulator output signal is fed to the video amplifier via an integrated low-pass filter for attenuation of the carrier harmonics. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics. The video output signal at pin $V_{o(vid)}$ is 1.35 V (p-p) for nominal vision IF modulation. Noise clipping is provided.

SIF amplifier and SIF AGC

The sound IF amplifier consists of two AC-coupled differential amplifier stages. Each differential stage comprises a controlled feedback network provided by emitter degeneration.

The SIF AGC detector is related to the SIF input signal (average level of FM carrier) and controls the SIF amplifier to provide a constant SIF signal to the single reference QSS mixer.

Single reference QSS mixer

The single reference QSS mixer is realized by a multiplier. The SIF amplifier output signal is fed to the single reference QSS mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO). The mixer output signal is fed via a high-pass filter for attenuation of the video signal components to the output pin 10. With this system a high performance hi-fi stereo sound processing can be achieved.

FM-PLL demodulator

The FM-PLL demodulator consists of a limiter and an FM-PLL. The limiter provides the amplification and limitation of the FM sound intercarrier signal. The result is high sensitivity and AM suppression. The amplifier consists of 7 stages which are internally AC-coupled in order to minimize the DC offset.

Furthermore the AF output signal can be muted by connecting a resistor between the limiter input pin 11 and ground.

The FM-PLL consists of an integrated relaxation oscillator, an integrated loop filter and a phase detector. The oscillator is locked to the FM intercarrier signal, output from the limiter. As a result of locking, the oscillator frequency tracks with the modulation of the input signal and the oscillator control voltage is superimposed by the AF voltage. The FM-PLL operates as an FM demodulator.

AF signal processing

The AF amplifier consists of two parts:

1. The AF pre-amplifier for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by approximately 33 dB. The low-pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal pin 10. An additional DC control circuit is implemented to keep the DC level constant, independent of process spread.
2. The AF output amplifier (10 dB) provides the required output level by a rail-to-rail output stage. This amplifier makes use of an input selector for switching to FM or mute state, controlled by the mute switching voltage.

Internal voltage stabilizer

The bandgap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	note 1			
		$T_{j(max)}$ = 125 °C; TDA9808 (DIP20)	–	9.9	V
		$T_{j(max)}$ = 115 °C; TDA9808T (SO20)	–	5.5	V
V_i	voltage at pins 1, 2, 5, 13, 17, 19 and 20		0	V_P	V
$t_{s(max)}$	maximum short-circuit time to ground or V_P		–	10	s
V_{12}	tuner AGC output voltage		0	13.2	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C
V_{es}	electrostatic handling voltage	note 2	–300	+300	V

Notes

1. I_P = 95 mA; T_{amb} = 70 °C.
2. Machine model class B (L = 2.5 μH).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA9808 (DIP20)		62	K/W
	TDA9808T (SO20)		85	K/W

CHARACTERISTICS (9 V SUPPLY, TDA9808; DIP20 only)

V_P = 9 V; T_{amb} = 25 °C; see Table 1 for input frequencies and carrier ratios; input level $V_{i(VIF)(rms)}$ = 10 mV (pins 1 and 2) (sync-level); $V_{i(SIF)(rms)}$ = 4.5 mV (pins 19 and 20) (sound carrier); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier: 10%; video signal in accordance with *"NTC-7 Composite"*; measurements taken in Fig.13; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 18)						
V_P	supply voltage	note 1	4.5	5.0	9.9	V
I_P	supply current		72	85	98	mA
True synchronous video demodulator; note 2						
$V_{i(VIF)(rms)}$	VIF input signal voltage sensitivity (RMS value)	PLL still locked; maximum IF gain; note 3	–	60	90	μV
Composite video amplifier (pin 9; sound carrier off)						
$V_{o(video)(p-p)}$	video output signal voltage (peak-to-peak value)	see Fig.8	1.27	1.45	1.63	V
$S/N_{W(video)}$	weighted signal-to-noise ratio	see Fig.6 and note 4	56	60	–	dB
PSRR	power supply ripple rejection at pin 9	see Fig.11	25	30	–	dB
Tuner AGC (pin 12)						
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB
AFC circuit (pin 13); see Fig.10 and note 5						
S	control steepness $\Delta I_{13}/\Delta f$	note 6				
		f_{pc} = 38.9 MHz	0.35	0.55	0.75	μA/kHz
		f_{pc} = 45.75 MHz	0.35	0.55	0.75	μA/kHz
		f_{pc} = 58.75 MHz	0.35	0.55	0.75	μA/kHz
$\Delta f_{IF}/\Delta T$	frequency variation by temperature	I_{AFC} = 0; note 7	–	–	$\pm 20 \times 10^{-6}$	K^{-1}
FM-PLL sound demodulator and AF output (pin 6); note 8						
$V_{o(AF)(6)(rms)}$	AF output signal voltage (RMS value)	±25 kHz (50% FM deviation); see Fig.13	375	500	625	mV
$S/N_{W(audio)}$	weighted signal-to-noise ratio	*"CCIR 468-4"*; see Fig.13	55	60	–	dB
α_6	mute attenuation		70	75	–	dB
ΔV_5	DC jump voltage of AF output terminal	FM-PLL in lock mode	–	±50	±175	mV

Notes to the characteristics

1. Values of video and sound parameters are decreased at V_P = 4.5 V.
2. Loop bandwidth BL = 70 kHz (natural frequency f_n = 12 kHz; damping factor d ≈ 3; calculated with sync level within gain control range). Resonance circuit of VCO: Q_0 > 50; C_{ext}: see Table 3; C_{int} ≈ 8.5 pF (loop voltage approximately 2.7 V).
3. $V_{i(VIF)}$ signal for nominal video signal.
4. S/N is the ratio of black to white amplitude to the black level noise voltage (RMS value, pin 9). B = 5 MHz weighted in accordance with *"CCIR 567"* at a source impedance of 50 Ω.
5. To match the AFC output signal to different tuning systems a current source output is provided (Fig.10).
6. Depending on the ratio $\Delta C/C_0$ of the LC resonant circuit of VCO (Q_0 > 50; see note 2; $C_0 = C_{int} + C_{ext}$).
7. Temperature coefficient of external LC-circuit is equal to zero.
8. Input level for second IF from an external generator with 50 Ω source impedance. AC-coupled with 10 nF capacitor, f_{mod} = 1 kHz, 25 kHz (50% FM deviation) of audio reference. A VIF/SIF input signal is not permitted. Pin 17 has to be connected to positive supply voltage. S/N and THD measurements are taken at 50 µs (75 µs at M standard) de-emphasis.

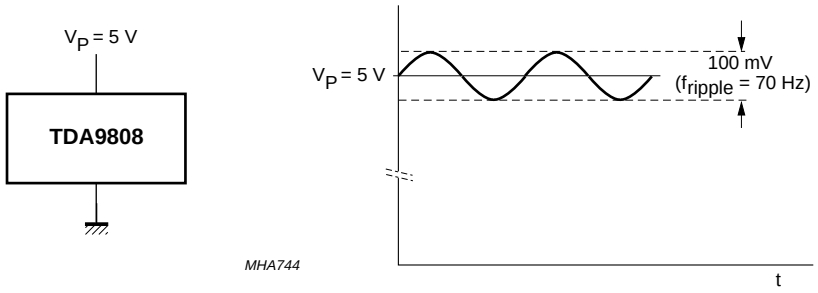
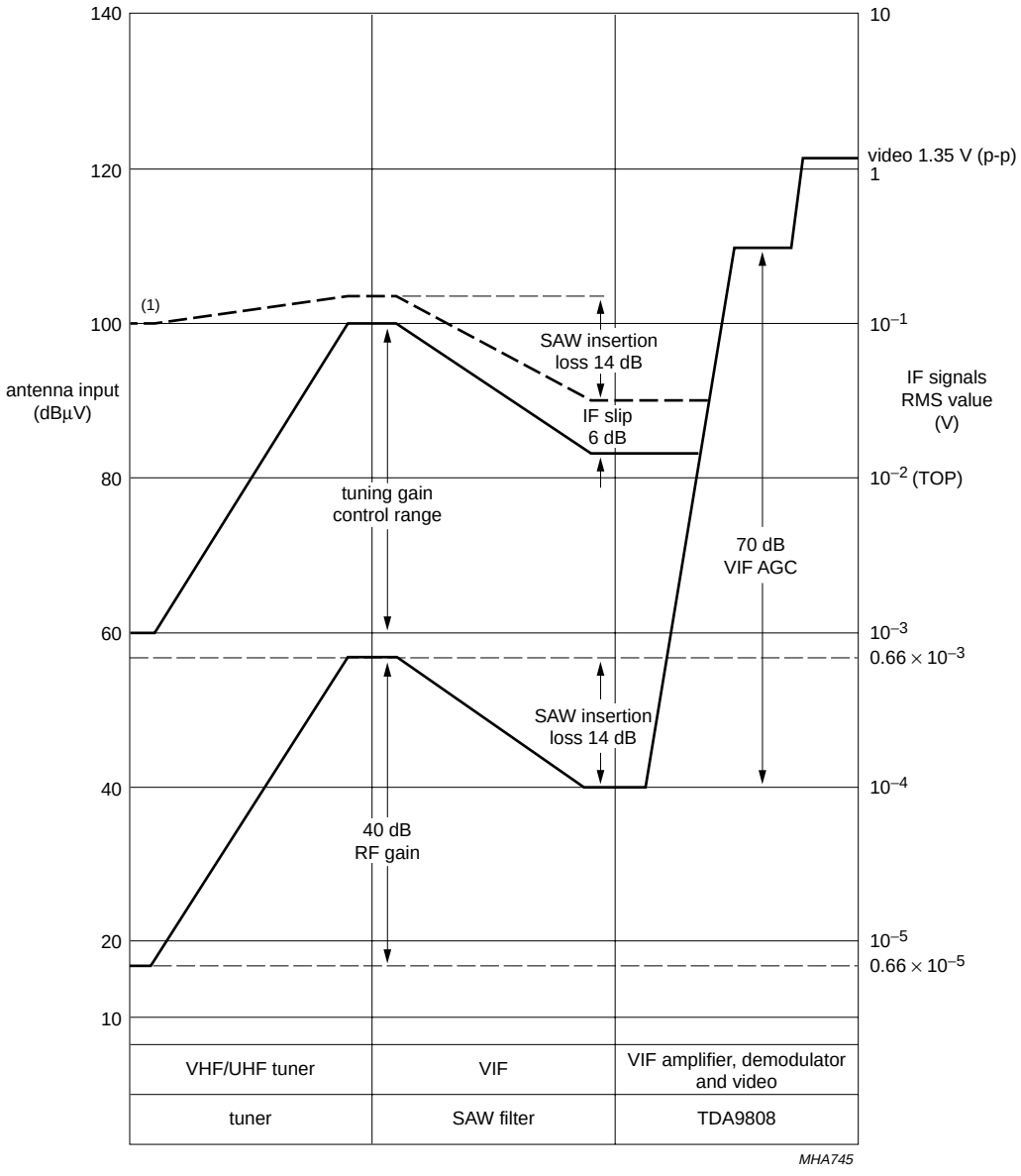


Fig.11 Ripple rejection condition.

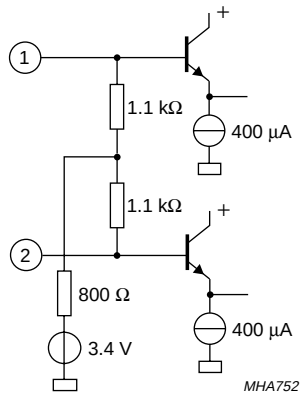
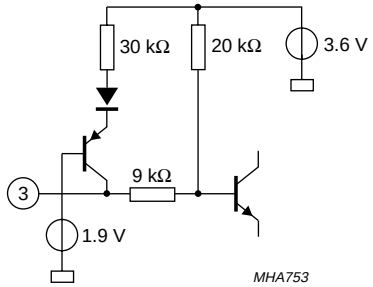
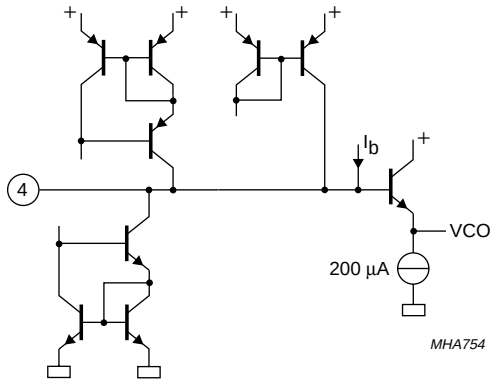


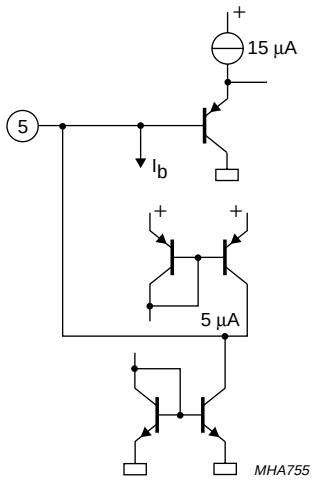
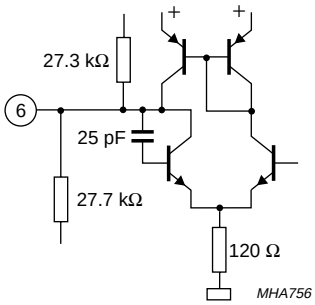
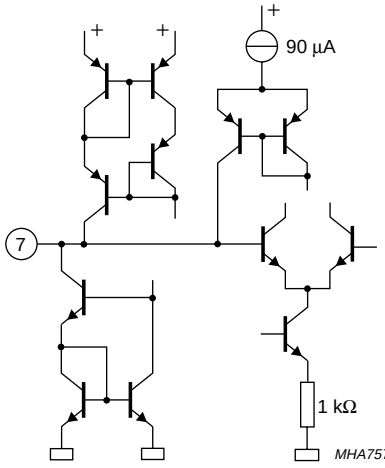
(1) Depends on TOP.

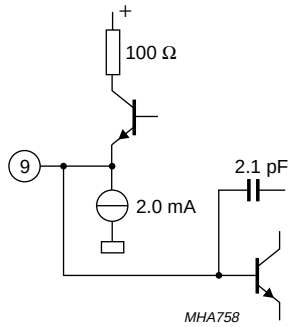
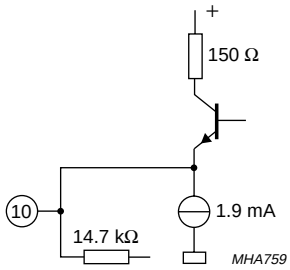
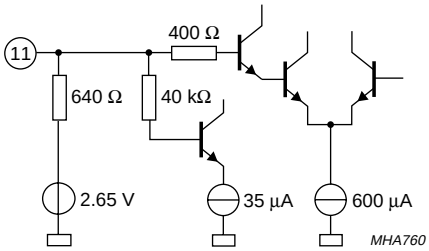
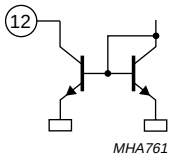
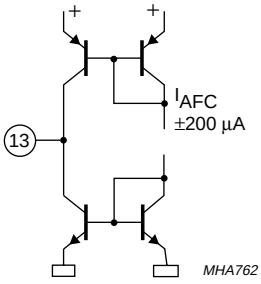
Fig.12 Front end level diagram.

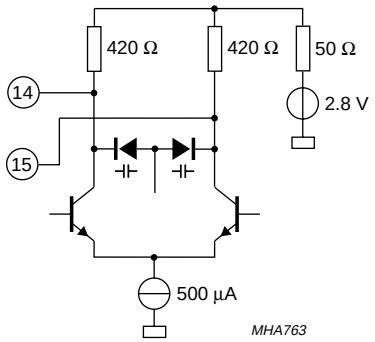
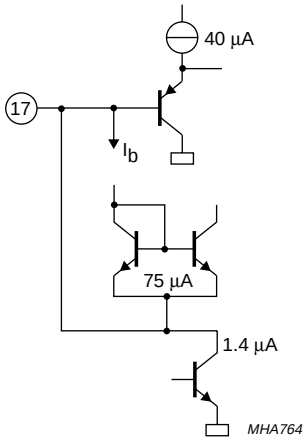
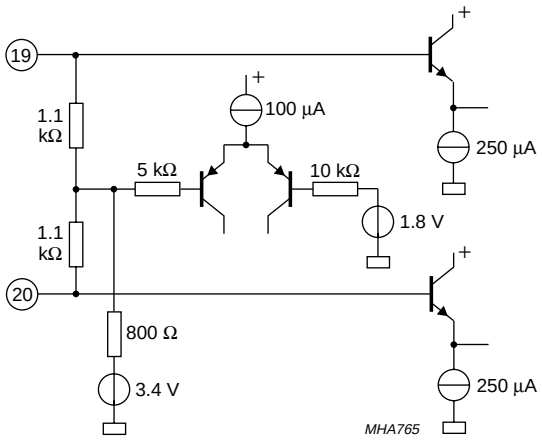
INTERNAL CIRCUITRY

Table 2 Equivalent pin circuits and pin voltages

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
1	$V_{i\ VIF1}$	3.4	
2	$V_{i\ VIF2}$	3.4	
3	TADJ (TOP)	0 to 1.9	
4	T_{PLL}	1.5 to 4.0	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
5	C_{SAGC}	1.5 to 4.0	
6	$V_{o\ AF}$	2.3	
7	C_{DEC}	1.2 to 3.0	
8	n.c.		

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
9	$V_{o(vid)}$	sync level: 1.5	
10	$V_{o\ QSS}$	2.0	
11	$V_{i\ FM}$	2.65	
12	TAGC	0 to 13.2	
13	AFC	0.3 to V_P – 0.3	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
14	VCO1	2.7	
15	VCO2	2.7	
16	GND	0	
17	C_{VAGC}	1.5 to 4.0	
18	V_P	V_P	
19	$V_{i\ SIF1}$	3.4	
20	$V_{i\ SIF2}$	3.4	

TEST AND APPLICATION INFORMATION

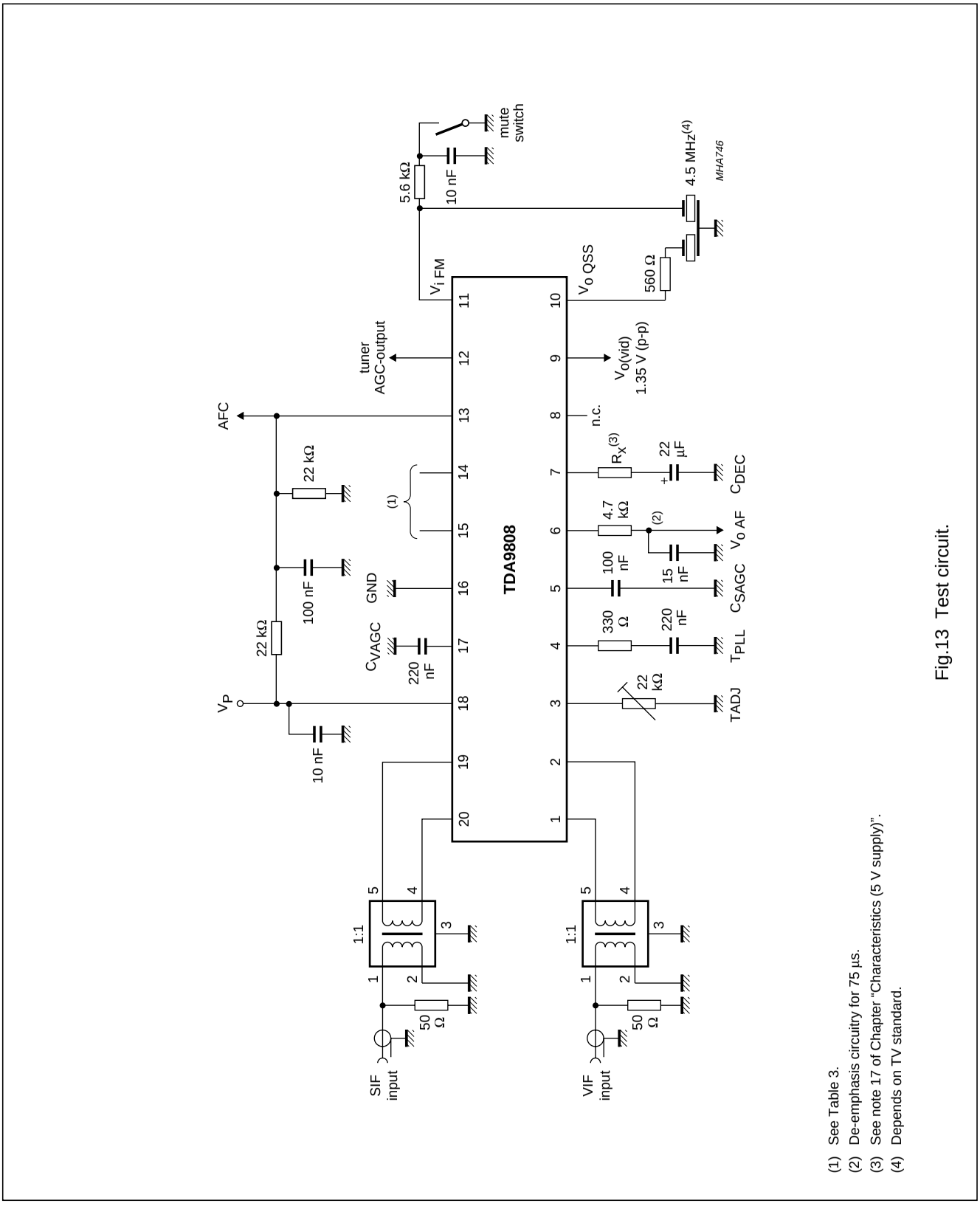


Fig.13 Test circuit.

(1) See Table 3.
(2) De-emphasis circuitry for 75 µs.
(3) See note 17 of Chapter "Characteristics (5 V supply)".
(4) Depends on TV standard.

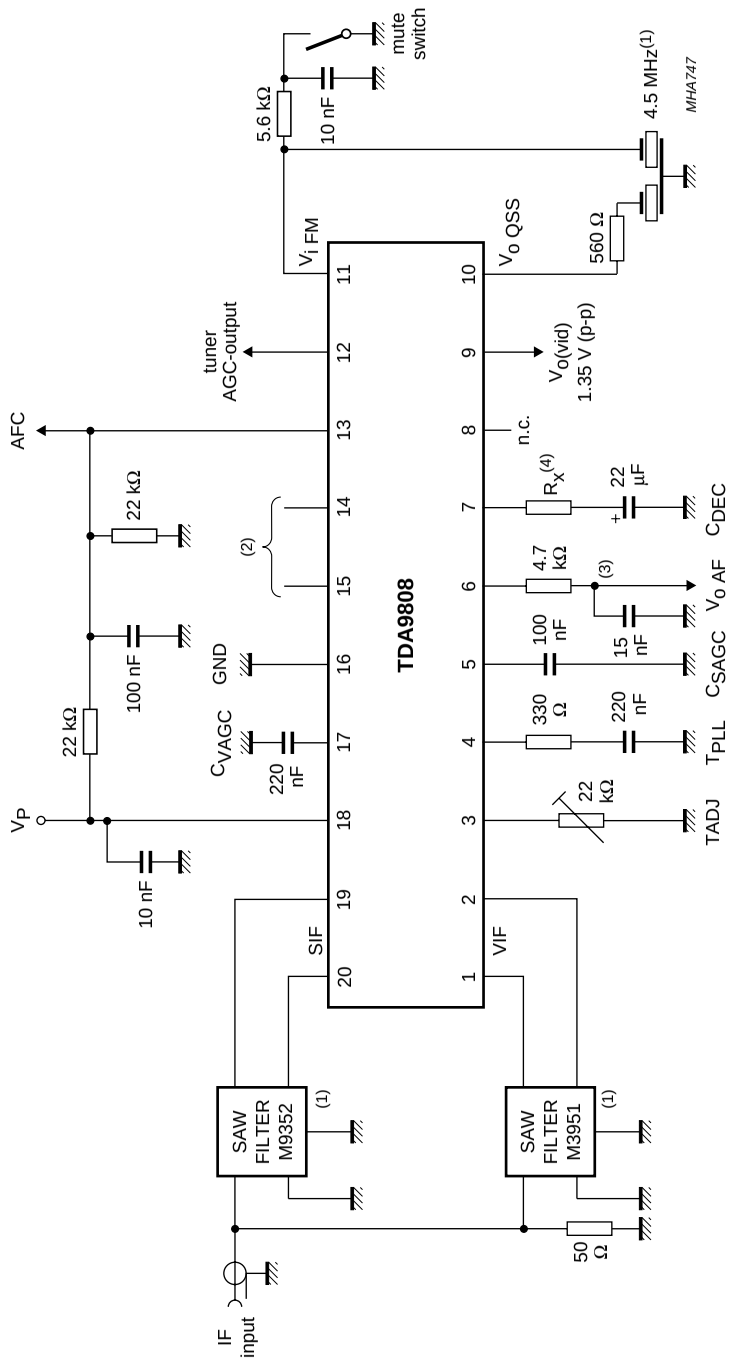
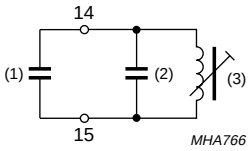
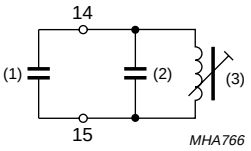
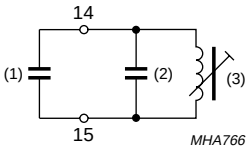


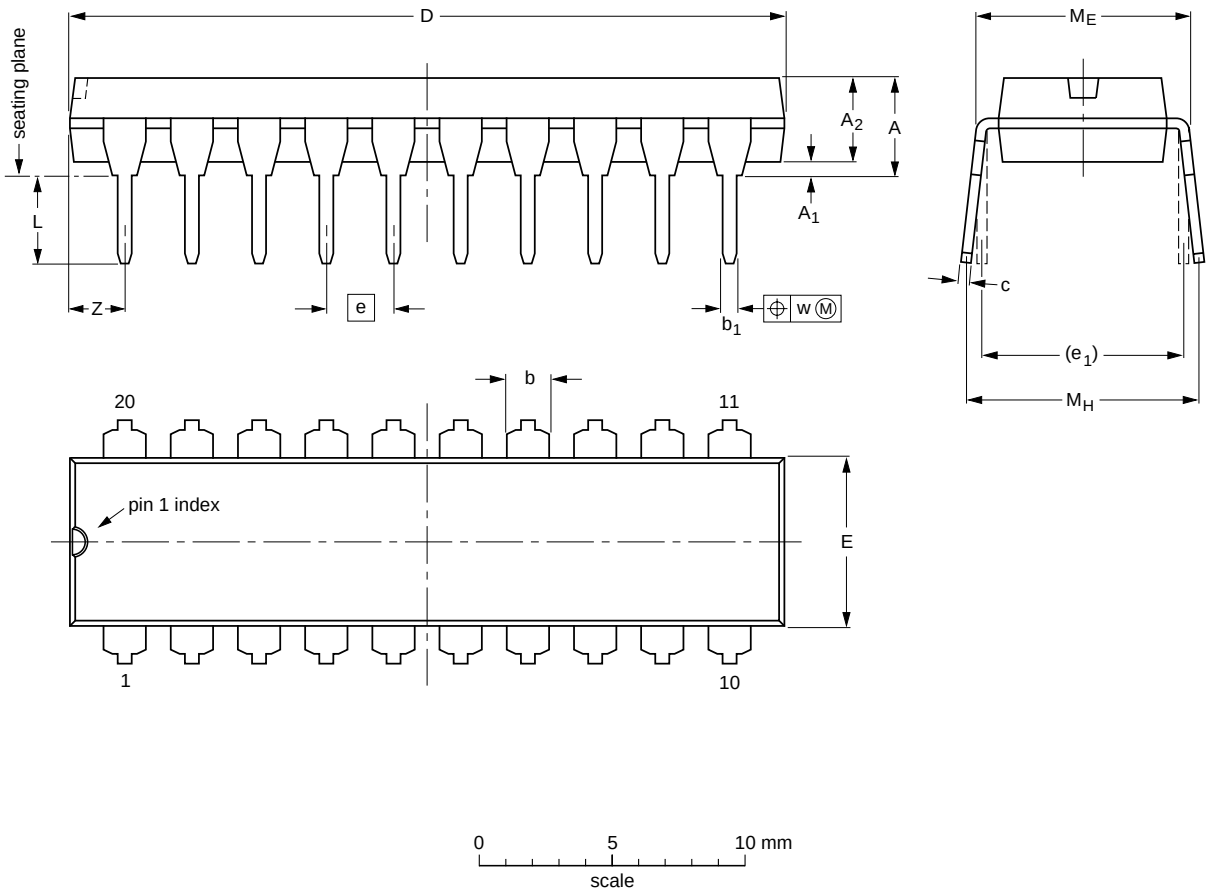
Fig.14 Application circuit.

Table 3 Oscillator circuit for the different TV standards

PARAMETER	EUROPE	USA	JAPAN
IF frequency	38.9 MHz	45.75 MHz	58.75 MHz
VCO frequency	77.8 MHz	91.5 MHz	117.5 MHz
Oscillator circuit	 (1) C_{VCO} = 8.5 pF. (2) C = 8.2 ±0.25 pF. (3) L = 251 nH.	 (1) C_{VCO} = 8.5 pF. (2) C = 10 ±0.25 pF. (3) L = 163 nH.	 (1) C_{VCO} = 8.5 pF. (2) C = 15 ±0.25 pF. (3) L = 78 nH.
e.g. Toko coil	5KM 369SNS-2010Z	5KMC V369SCS-2370Z	MC139 NE545SNAS100108
Philips ceramic capacitor	2222 632 51828	inside of coil	15 pF SMD; size = 0805

PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

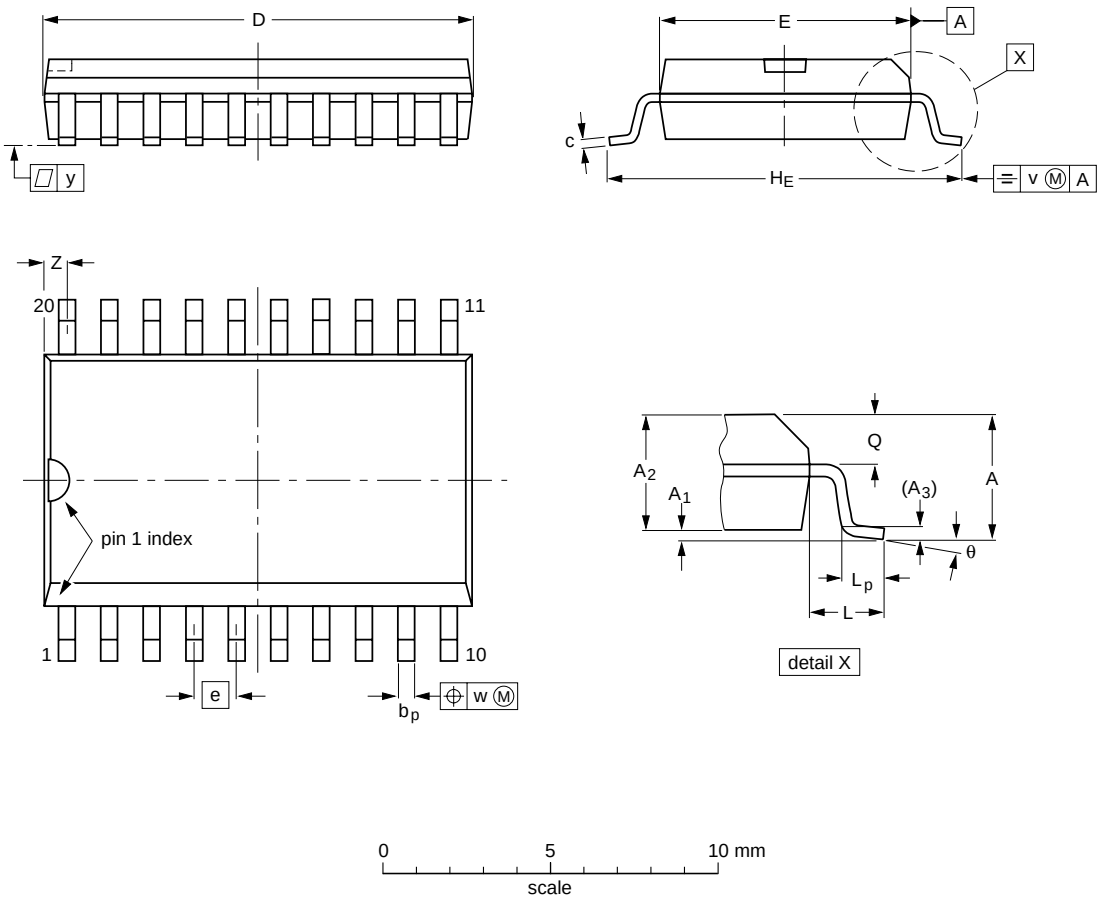
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW(1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(2)	–	suitable
Surface mount	BGA, SQFP	not suitable	suitable	–
	HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(3)	suitable	–
	PLCC(4), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(4)(5)	suitable	–
	SSOP, TSSOP, VSO	not recommended(6)	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 02 67 52 2531, Fax. +39 02 67 52 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 62 5344, Fax.+381 11 63 5777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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