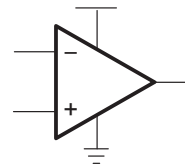


TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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- Rail-To-Rail Input/Output
- Wide Bandwidth . . . 3 MHz
- High Slew Rate . . . 2.4 V/ μ s
- Supply Voltage Range . . . 2.7 V to 16 V
- Supply Current . . . 550 μ A/Channel
- Low Power Shutdown Mode
 $I_{DD}(SHDN)$. . . 25 μ A/Channel
- Input Noise Voltage . . . 39 nV/ $\sqrt{\text{Hz}}$
- Input Bias Current . . . 1 pA
- Specified Temperature Range
 –40°C to 125°C . . . Industrial Grade
- Ultrasmall Packaging
 - 5 or 6 Pin SOT-23 (TLV2370/1)
 - 8 or 10 Pin MSOP (TLV2372/3)

Operational Amplifier



description

The TLV237x single supply operational amplifiers provide rail-to-rail input and output capability. The TLV237x takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range while adding the rail-to-rail output swing feature. The TLV237x also provides 3-MHz bandwidth from only 550 μ A. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from (± 8 V supplies down to ± 1.35 V) a variety of rechargeable cells.

The CMOS inputs enable use in high-impedance sensor interfaces, with the lower voltage operation making an ideal alternative for the TLC227x in battery-powered applications. The rail-to-rail input stage further increases its versatility. The TLV237x is the seventh member of a rapidly growing number of RRIO products available from TI, and it is the first to allow operation up to 16-V rails with good ac performance.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

The 2.7-V operation makes the TLV237x compatible with Li-Ion powered systems and the operating supply voltage range of many micro-power microcontrollers available today including TI's MSP430.

SELECTION OF SIGNAL AMPLIFIER PRODUCTS†

| DEVICE | V_{DD} (V) | V_{IO} (μ V) | $I_{q/Ch}$ (μ A) | I_{IB} (pA) | GBW (MHz) | SR (V/ μ s) | SHUTDOWN | RAIL-TO-RAIL | SINGLES/DUALS/QUADS |
|---------|--------------|---------------------|-----------------------|---------------|-----------|-----------------|----------|--------------|---------------------|
| TLV237x | 2.7–16 | 500 | 550 | 1 | 3 | 2.4 | Yes | I/O | S/D/Q |
| TLC227x | 4–16 | 300 | 1100 | 1 | 2.2 | 3.6 | — | O | D/Q |
| TLV27x | 2.7–16 | 500 | 550 | 1 | 3 | 2.4 | — | O | S/D/Q |
| TLC27x | 3–16 | 1100 | 675 | 1 | 1.7 | 3.6 | — | — | S/D/Q |
| TLV246x | 2.7–6 | 150 | 550 | 1300 | 6.4 | 1.6 | Yes | I/O | S/D/Q |
| TLV247x | 2.7–6 | 250 | 600 | 2 | 2.8 | 1.5 | Yes | I/O | S/D/Q |
| TLV244x | 2.7–10 | 300 | 725 | 1 | 1.8 | 1.4 | — | O | D/Q |

† Typical values measured at 5 V, 25°C



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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FAMILY PACKAGE TABLE

| DEVICE | NUMBER OF CHANNELS | PACKAGE TYPES | | | | | SHUTDOWN | UNIVERSAL EVM BOARD |
|---------|--------------------|---------------|------|--------|-------|------|----------|---|
| | | PDIP | SOIC | SOT-23 | TSSOP | MSOP | | |
| TLV2370 | 1 | 8 | 8 | 6 | — | — | Yes | Refer to the EVM Selection Guide (Lit# SLOU060) |
| TLV2371 | 1 | 8 | 8 | 5 | — | — | — | |
| TLV2372 | 2 | 8 | 8 | — | — | 8 | — | |
| TLV2373 | 2 | 14 | 14 | — | — | 10 | Yes | |
| TLV2374 | 4 | 14 | 14 | — | 14 | — | — | |
| TLV2375 | 4 | 16 | 16 | — | 16 | — | Yes | |

TLV2370 and TLV2371 AVAILABLE OPTIONS

| T _A | V _{IO} MAX AT 25°C | PACKAGED DEVICES | | | |
|----------------|-----------------------------|--------------------------------|----------------------------|--------------|------------------------|
| | | SMALL OUTLINE (D) [†] | SOT-23 | | PLASTIC DIP (P) |
| | | | (DBV) [‡] | SYMBOL | |
| -40°C to 125°C | 4.5 mV | TLV2370ID TLV2371ID | TLV2370IDBV TLV2371IDBV | VBFI VBGI | TLV2370IP TLV2371IP |

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2370IDR).

[‡] This package is only available taped and reeled. For standard quantities (3,000 pieces per reel), add an R suffix (e.g., TLV2370IDBVR). For smaller quantities (250 pieces per mini-reel), add a T suffix to the part number (e.g., TLV2370IDBVT).

TLV2372 AND TLV2373 AVAILABLE OPTIONS

| T _A | V _{IO} MAX AT 25°C | PACKAGED DEVICES | | | | | | |
|----------------|-----------------------------|--------------------------------|--------------------|----------|--------------------|----------|-----------------|-----------------|
| | | SMALL OUTLINE (D) [§] | MSOP | | | | PLASTIC DIP (N) | PLASTIC DIP (P) |
| | | | (DGK) [§] | SYMBOL | (DGS) [§] | SYMBOL | | |
| -40°C to 125°C | 4.5 mV | TLV2372ID TLV2373ID | TLV2372IDGK — | APG — | — TLV2373IDGS | — API | — TLV2373IN | TLV2372IP — |

[§] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2372IDR).

TLV2374 and TLV2375 AVAILABLE OPTIONS

| T _A | V _{IO} MAX AT 25°C | PACKAGED DEVICES | | |
|----------------|-----------------------------|--------------------------------|------------------------|--------------------------|
| | | SMALL OUTLINE (D) [¶] | PLASTIC DIP (N) | TSSOP (PW) [¶] |
| -40°C to 125°C | 4.5 mV | TLV2374ID TLV2375ID | TLV2374IN TLV2375IN | TLV2374IPW TLV2375IPW |

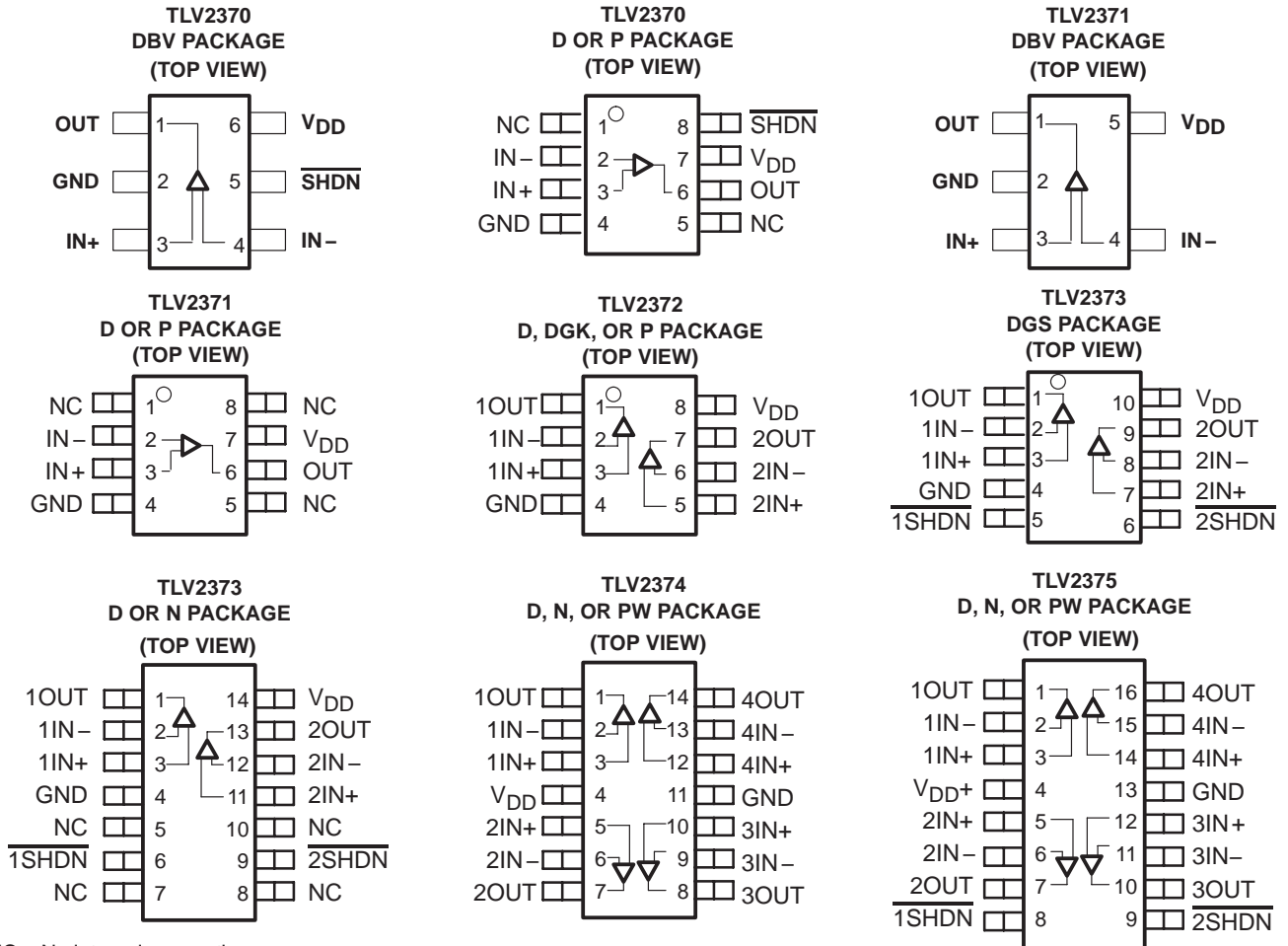
[¶] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2374IDR).



TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

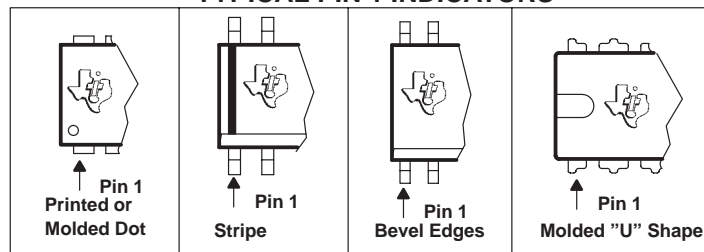
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TLV237x PACKAGE PINOUTS(1)



NC – No internal connection
 (1) SOT-23 may or may not be indicated

TYPICAL PIN 1 INDICATORS



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|------------------------------|
| Supply voltage, V_{DD} (see Note 1) | 16.5 V |
| Differential input voltage, V_{ID} | $\pm V_{DD}$ |
| Input voltage range, V_I (see Note 1) | -0.2 V to $V_{DD} + 0.2$ V |
| Input current range, I_I | ± 10 mA |
| Output current range, I_O | ± 100 mA |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A : I suffix | -40°C to 125°C |
| Maximum junction temperature, T_J | 150°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

| PACKAGE | θ_{JC} (°C/W) | θ_{JA} (°C/W) | $T_A \leq 25^\circ\text{C}$ POWER RATING |
|------------|-------------------------|-------------------------|---|
| D (8) | 38.3 | 176 | 710 mW |
| D (14) | 26.9 | 122.3 | 1022 mW |
| D (16) | 25.7 | 114.7 | 1090 mW |
| DBV (5) | 55 | 324.1 | 385 mW |
| DBV (6) | 55 | 294.3 | 425 mW |
| DGK (8) | 54.23 | 259.96 | 481 mW |
| DGS (10) | 54.1 | 257.71 | 485 mW |
| N (14, 16) | 32 | 78 | 1600 mW |
| P (8) | 41 | 104 | 1200 mW |
| PW (14) | 29.3 | 173.6 | 720 mW |
| PW (16) | 28.7 | 161.4 | 774 mW |

recommended operating conditions

| | | MIN | MAX | UNIT |
|--|---------------|------------|----------|------|
| Supply voltage, V_{DD} | Single supply | 2.7 | 16 | V |
| | Split supply | ± 1.35 | ± 8 | |
| Common-mode input voltage range, V_{ICR} | | 0 | V_{DD} | V |
| Operating free-air temperature, T_A | I-suffix | -40 | 125 | °C |
| Turnon voltage level, $V_{(ON)}$, relative to GND pin voltage | | | 2 | V |
| Turnoff voltage level, $V_{(OFF)}$, relative to GND pin voltage | | 0.8 | | V |



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electrical characteristics at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V , and 15 V (unless otherwise noted)

dc performance

| PARAMETER | | TEST CONDITIONS | | T_A | MIN | TYP | MAX | UNIT |
|----------------|---|--|-------------------------|------------|-----|-----|-----|------------------------------|
| V_{IO} | Input offset voltage | $V_{IC} = V_{DD}/2,$ $R_S = 50\ \Omega$ | $V_O = V_{DD}/2,$ | 25°C | | 2 | 4.5 | mV |
| | | | | Full range | | | 6 | |
| α_{VIO} | Offset voltage drift | | | 25°C | | 2 | | $\mu\text{V}/^\circ\text{C}$ |
| CMRR | Common-mode rejection ratio | $V_{IC} = 0\text{ to }V_{DD},$ $R_S = 50\ \Omega$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 50 | 68 | dB | |
| | | | | Full range | 49 | | | |
| | | $V_{IC} = 0\text{ to }V_{DD}-1.35\text{V},$ $R_S = 50\ \Omega$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 56 | 70 | | |
| | | | | Full range | 54 | | | |
| | | $V_{IC} = 0\text{ to }V_{DD},$ $R_S = 50\ \Omega,$ | $V_{DD} = 5\text{ V}$ | 25°C | 55 | 72 | | |
| | | | | Full range | 54 | | | |
| | | $V_{IC} = 0\text{ to }V_{DD}-1.35\text{V},$ $R_S = 50\ \Omega,$ | $V_{DD} = 5\text{ V}$ | 25°C | 67 | 80 | | |
| | | | | Full range | 64 | | | |
| | | $V_{IC} = 0\text{ to }V_{DD},$ $R_S = 50\ \Omega,$ | $V_{DD} = 15\text{ V}$ | 25°C | 64 | 82 | | |
| | | | | Full range | 63 | | | |
| | | $V_{IC} = 0\text{ to }V_{DD}-1.35\text{V},$ $R_S = 50\ \Omega,$ | $V_{DD} = 15\text{ V}$ | 25°C | 67 | 84 | | |
| | | | | Full range | 66 | | | |
| A_{VD} | Large-signal differential voltage amplification | $V_{O(PP)} = V_{DD}/2,$ $R_L = 10\ \text{k}\Omega$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 98 | 106 | dB | |
| | | | | Full range | 76 | | | |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | 100 | 110 | | |
| | | | | Full range | 86 | | | |
| | | | $V_{DD} = 15\text{ V}$ | 25°C | 81 | 83 | | |
| | | | | Full range | 79 | | | |

input characteristics

| PARAMETER | | TEST CONDITIONS | | T_A | MIN | TYP | MAX | UNIT |
|------------|-------------------------------|---|----------------------|-------|-----|------|------|------------|
| I_{IO} | Input offset current | $V_{DD} = 15\text{ V},$ $V_O = V_{DD}/2$ | $V_{IC} = V_{DD}/2,$ | 25°C | | 1 | 60 | pA |
| | | | | 70°C | | | 100 | |
| | | | | 125°C | | | 1000 | |
| I_{IB} | Input bias current | $V_{DD} = 15\text{ V},$ $V_O = V_{DD}/2$ | $V_{IC} = V_{DD}/2,$ | 25°C | | 1 | 60 | pA |
| | | | | 70°C | | | 100 | |
| | | | | 125°C | | | 1000 | |
| $r_{i(d)}$ | Differential input resistance | | | 25°C | | 1000 | | G Ω |
| C_{IC} | Common-mode input capacitance | $f = 21\ \text{kHz}$ | | 25°C | | 8 | | pF |



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FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT
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electrical characteristics at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V , and 15 V (unless otherwise noted) (continued)

output characteristics

| PARAMETER | TEST CONDITIONS | T_A | MIN | TYP | MAX | UNIT |
|------------------------------------|--|-------------------------|------------|-------|-------|------|
| V_{OH} High-level output voltage | $V_{IC} = V_{DD}/2$, $I_{OH} = -1\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 2.55 | 2.58 | V |
| | | | Full range | 2.48 | | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | 4.9 | 4.93 | |
| | | | Full range | 4.85 | | |
| | | $V_{DD} = 15\text{ V}$ | 25°C | 14.92 | 14.96 | |
| | | | Full range | 14.9 | | |
| | $V_{IC} = V_{DD}/2$, $I_{OH} = -5\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 1.9 | 2 | |
| | | | Full range | 1.6 | | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | 4.6 | 4.68 | |
| | | | Full range | 4.5 | | |
| | | $V_{DD} = 15\text{ V}$ | 25°C | 14.7 | 14.8 | |
| | | | Full range | 14.6 | | |
| V_{OL} Low-level output voltage | $V_{IC} = V_{DD}/2$, $I_{OL} = 1\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 0.1 | 0.15 | V |
| | | | Full range | | 0.22 | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | 0.05 | 0.1 | |
| | | | Full range | | 0.15 | |
| | | $V_{DD} = 15\text{ V}$ | 25°C | 0.05 | 0.08 | |
| | | | Full range | | 0.1 | |
| | $V_{IC} = V_{DD}/2$, $I_{OL} = 5\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 0.52 | 0.7 | |
| | | | Full range | | 1.1 | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | 0.28 | 0.4 | |
| | | | Full range | | 0.5 | |
| | | $V_{DD} = 15\text{ V}$ | 25°C | 0.19 | 0.3 | |
| | | | Full range | | 0.35 | |
| I_O Output current | $V_{DD} = 2.7\text{ V}$, $V_O = 0.5\text{ V}$ from rail | Positive rail | 25°C | 4 | mA | |
| | | Negative rail | 25°C | 5 | | |
| | $V_{DD} = 5\text{ V}$, $V_O = 0.5\text{ V}$ from rail | Positive rail | 25°C | 7 | | |
| | | Negative rail | 25°C | 8 | | |
| | $V_{DD} = 15\text{ V}$, $V_O = 0.5\text{ V}$ from rail | Positive rail | 25°C | 16 | | |
| | | Negative rail | 25°C | 15 | | |

power supply

| PARAMETER | TEST CONDITIONS | T_A | MIN | TYP | MAX | UNIT |
|---|---|-------------------------|------------|-----|------|---------------|
| I_{DD} Supply current (per channel) | $V_O = V_{DD}/2$, | $V_{DD} = 2.7\text{ V}$ | 25°C | 470 | 560 | μA |
| | | $V_{DD} = 5\text{ V}$ | 25°C | 550 | 660 | |
| | | $V_{DD} = 15\text{ V}$ | 25°C | 750 | 900 | |
| | | | Full range | | 1200 | |
| PSRR Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$) | $V_{DD} = 2.7\text{ V}$ to 15 V , No load | $V_{IC} = V_{DD}/2$, | 25°C | 70 | 80 | dB |
| | | Full range | | 65 | | |



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electrical characteristics at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V , and 15 V (unless otherwise noted) (continued)

dynamic performance

| PARAMETER | | TEST CONDITIONS | | T_A | MIN | TYP | MAX | UNIT |
|-----------|-------------------------|--|---|--------------------|------|-----|-----|------------------------|
| UGBW | Unity gain bandwidth | $R_L = 2\text{ k}\Omega$, $C_L = 10\text{ pF}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 2.4 | | 3 | MHz |
| | | | $V_{DD} = 5\text{ V to }15\text{ V}$ | 25°C | | | | |
| SR | Slew rate at unity gain | $V_{O(PP)} = V_{DD}/2$, $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 1.4 | 2 | 1 | $\text{V}/\mu\text{s}$ |
| | | | | Full range | | | | |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | 1.6 | 2.4 | 1.2 | $\text{V}/\mu\text{s}$ |
| | | | | Full range | | | | |
| | | | $V_{DD} = 15\text{ V}$ | 25°C | 1.9 | 2.1 | 1.4 | $\text{V}/\mu\text{s}$ |
| | | | | Full range | | | | |
| ϕ_m | Phase margin | $R_L = 2\text{ k}\Omega$, | $C_L = 100\text{ pF}$ | 25°C | 65° | | | |
| | Gain margin | $R_L = 2\text{ k}\Omega$, | $C_L = 10\text{ pF}$ | 25°C | 18 | | dB | |
| t_s | Settling time | $V_{DD} = 2.7\text{ V}$, $V_{(STEP)PP} = 1\text{ V}$, $A_V = -1$, $C_L = 10\text{ pF}$, $R_L = 2\text{ k}\Omega$ | 0.1% | 25°C | 2.9 | | 2 | μs |
| | | | $V_{DD} = 5\text{ V}, 15\text{ V}$, $V_{(STEP)PP} = 1\text{ V}$, $A_V = -1$, $C_L = 47\text{ pF}$, $R_L = 2\text{ k}\Omega$ | | 0.1% | | | |

noise/distortion performance

| PARAMETER | | TEST CONDITIONS | | T_A | MIN | TYP | MAX | UNIT |
|-----------|--------------------------------------|---|-------------|--------------------|-------|-----|------------------------------|------|
| THD + N | Total harmonic distortion plus noise | $V_{DD} = 2.7\text{ V}$, $V_{O(PP)} = V_{DD}/2\text{ V}$, $R_L = 2\text{ k}\Omega$, $f = 10\text{ kHz}$ | $A_V = 1$ | 25°C | 0.02% | | | |
| | | | $A_V = 10$ | | 0.05% | | | |
| | | | $A_V = 100$ | | 0.18% | | | |
| | | $V_{DD} = 5\text{ V}, 15\text{ V}$, $V_{O(PP)} = V_{DD}/2\text{ V}$, $R_L = 2\text{ k}\Omega$, $f = 10\text{ kHz}$ | $A_V = 1$ | 25°C | 0.02% | | | |
| | | | $A_V = 10$ | | 0.09% | | | |
| | | | $A_V = 100$ | | 0.5% | | | |
| V_n | Equivalent input noise voltage | $f = 1\text{ kHz}$ | | 25°C | 39 | | $\text{nV}/\sqrt{\text{Hz}}$ | |
| | | $f = 10\text{ kHz}$ | | | 35 | | | |
| I_n | Equivalent input noise current | $f = 1\text{ kHz}$ | | 25°C | 0.6 | | $\text{fA}/\sqrt{\text{Hz}}$ | |

shutdown characteristics

| PARAMETER | | TEST CONDITIONS | T_A | MIN | TYP | MAX | UNIT |
|----------------|---|---|--------------------|-----|-----|---------------|---------------|
| $I_{DD(SHDN)}$ | Supply current in shutdown mode (TLV2370, TLV2373, TLV2375) (per channel) | $V_{DD} = 2.7\text{ V}, 5\text{ V}$, SHDN = 0 V | 25°C | 25 | 30 | 35 | μA |
| | | | Full range | | | | |
| | | $V_{DD} = 15\text{ V}$, SHDN = 0 V | 25°C | 40 | 45 | 50 | μA |
| | | | Full range | | | | |
| $t_{(on)}$ | Amplifier turnon time (see Note 2) | $R_L = 2\text{ k}\Omega$ | 25°C | 0.8 | | μs | |
| $t_{(off)}$ | Amplifier turnoff time (see Note 2) | | 25°C | 1 | | μs | |

NOTE 2: Disable time and enable time are defined as the interval between application of the logic signal to the SHDN terminal and the point at which the supply current has reached one half of its final value.



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TYPICAL CHARACTERISTICS

Table of Graphs

| | | | FIGURE |
|----------------|--|------------------------------|---------------|
| V_{IO} | Input offset voltage | vs Common-mode input voltage | 1, 2, 3 |
| CMRR | Common-mode rejection ratio | vs Frequency | 4 |
| | Input bias and offset current | vs Free-air temperature | 5 |
| V_{OL} | Low-level output voltage | vs Low-level output current | 6, 8, 10 |
| V_{OH} | High-level output voltage | vs High-level output current | 7, 9, 11 |
| $V_{O(PP)}$ | Peak-to-peak output voltage | vs Frequency | 12 |
| I_{DD} | Supply current | vs Supply voltage | 13 |
| PSRR | Power supply rejection ratio | vs Frequency | 14 |
| A_{VD} | Differential voltage gain & phase | vs Frequency | 15 |
| | Gain-bandwidth product | vs Free-air temperature | 16 |
| SR | Slew rate | vs Supply voltage | 17 |
| | | vs Free-air temperature | 18 |
| ϕ_m | Phase margin | vs Capacitive load | 19 |
| V_n | Equivalent input noise voltage | vs Frequency | 20 |
| | Voltage-follower large-signal pulse response | | 21, 22 |
| | Voltage-follower small-signal pulse response | | 23 |
| | Inverting large-signal response | | 24, 25 |
| | Inverting small-signal response | | 26 |
| | Crosstalk | vs Frequency | 27 |
| | Shutdown forward & reverse isolation | vs Frequency | 28 |
| $I_{DD(SHDN)}$ | Shutdown supply current | vs Supply voltage | 29 |
| $I_{DD(SHDN)}$ | Shutdown pin leakage current | vs Shutdown pin voltage | 30 |
| $I_{DD(SHDN)}$ | Shutdown supply current/output voltage | vs Time | 31, 32 |



TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

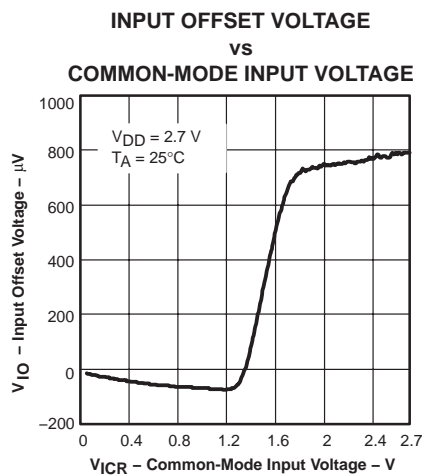


Figure 1

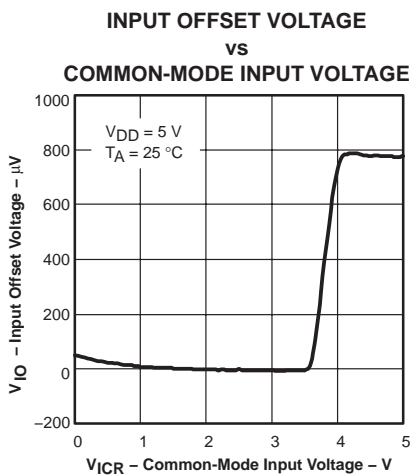


Figure 2

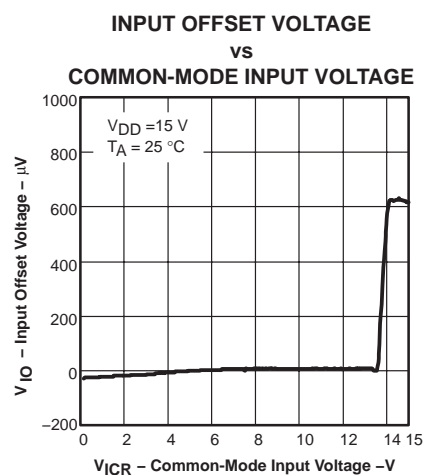


Figure 3

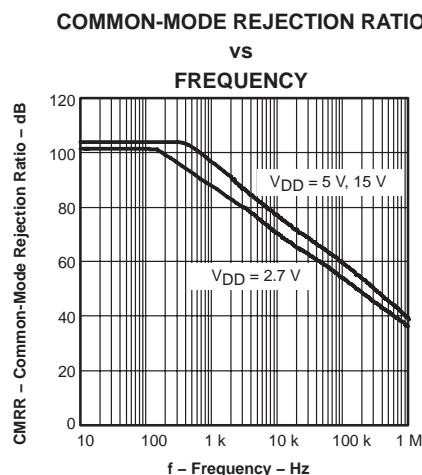


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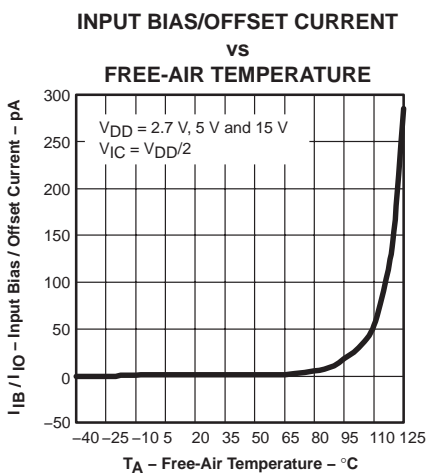


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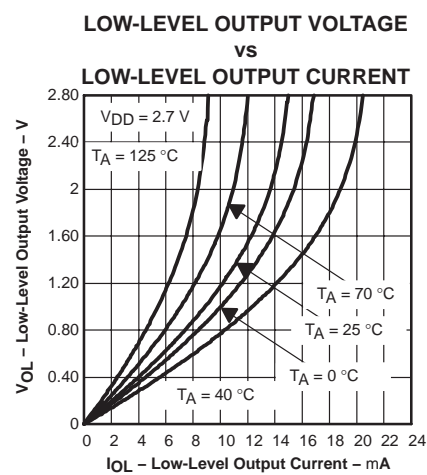


Figure 6

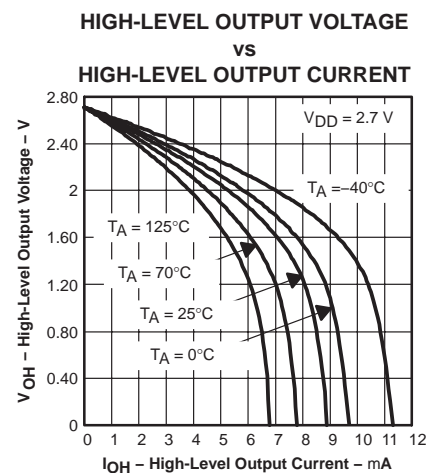


Figure 7

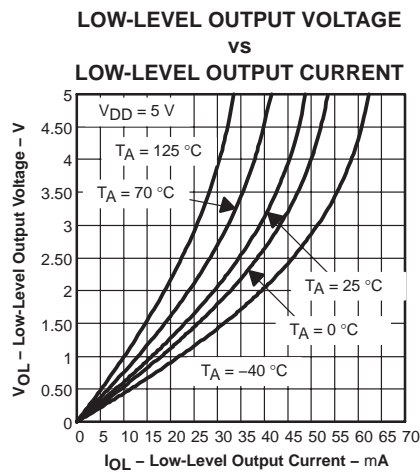


Figure 8

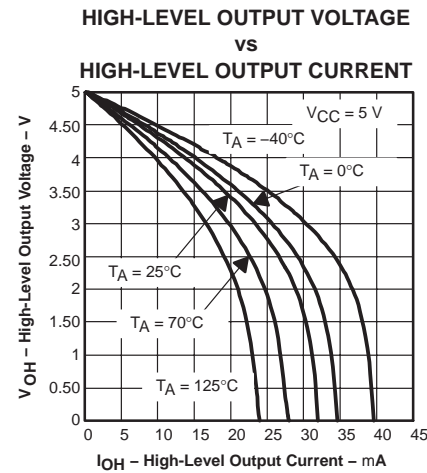


Figure 9

TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

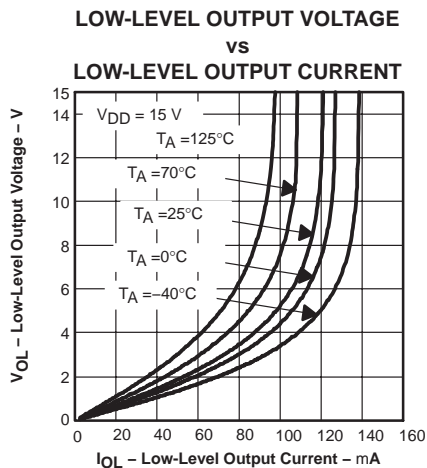


Figure 10

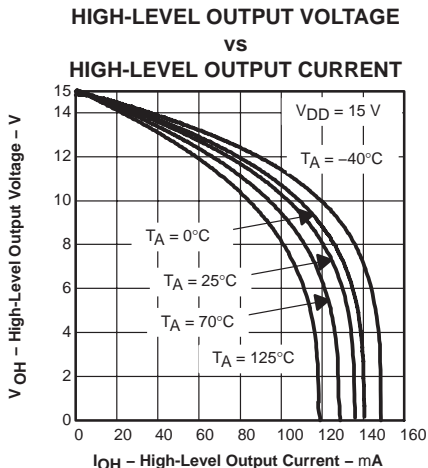


Figure 11

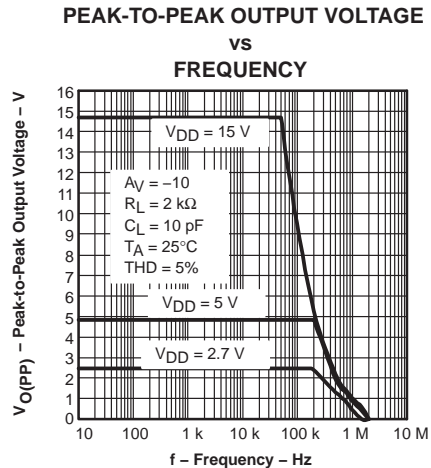


Figure 12

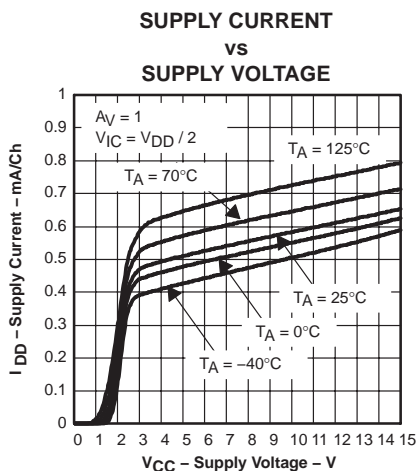


Figure 13

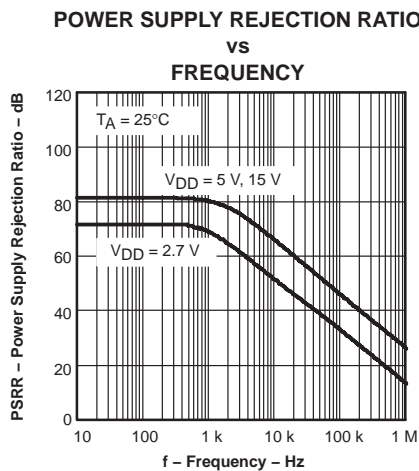


Figure 14

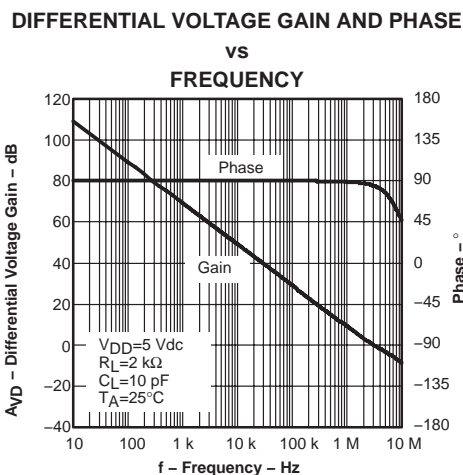


Figure 15

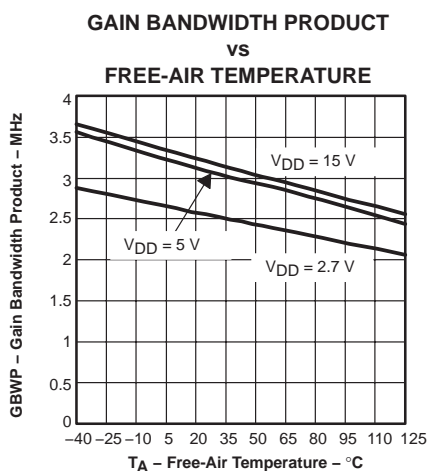


Figure 16



TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

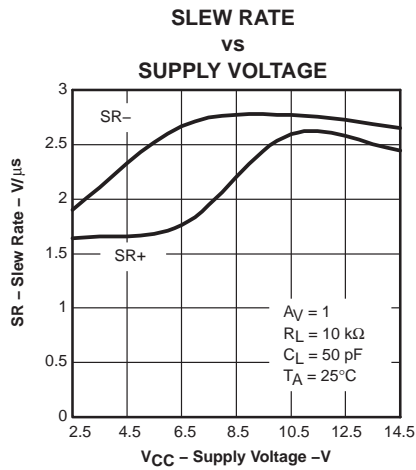


Figure 17

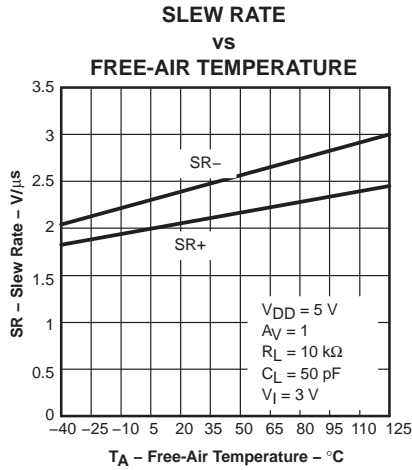


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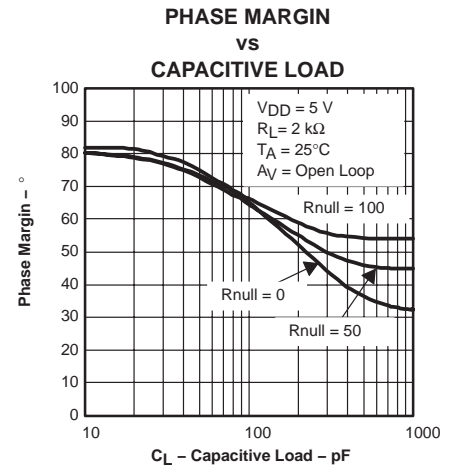


Figure 19

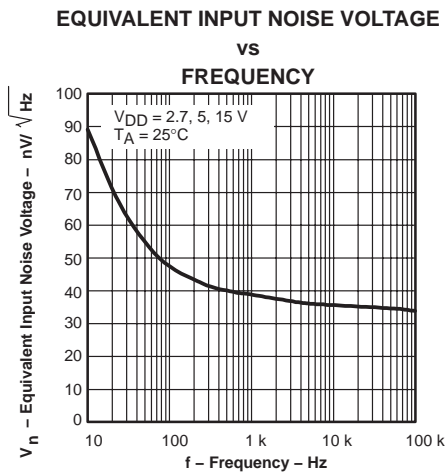


Figure 20

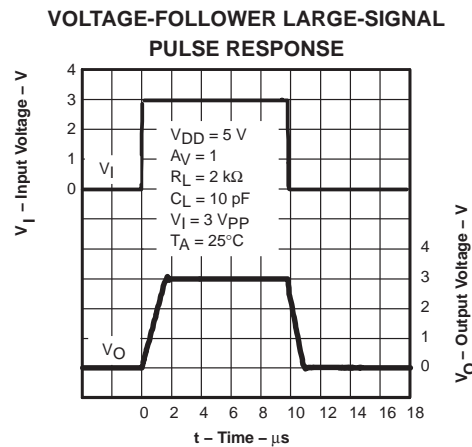


Figure 21

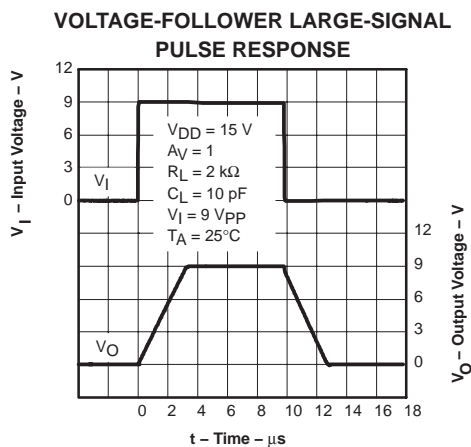


Figure 22

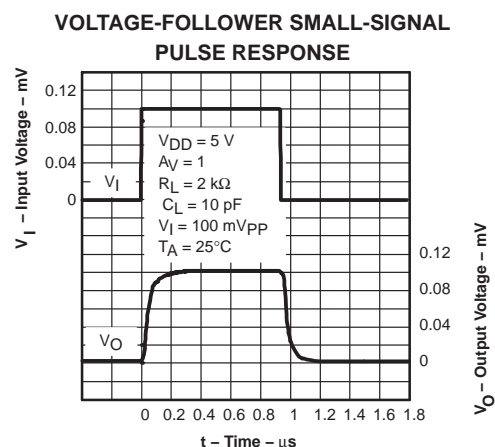


Figure 23

TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

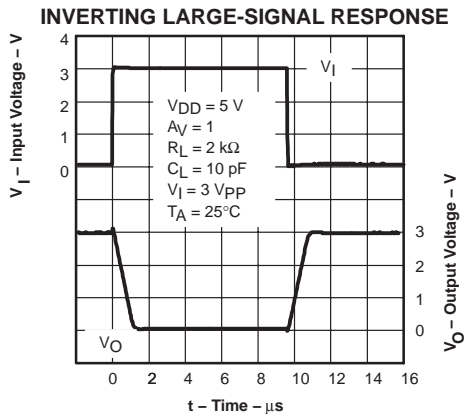


Figure 24

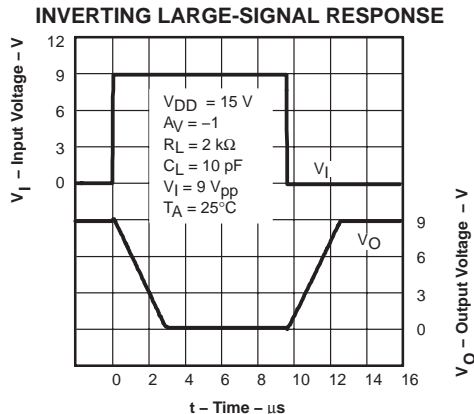


Figure 25

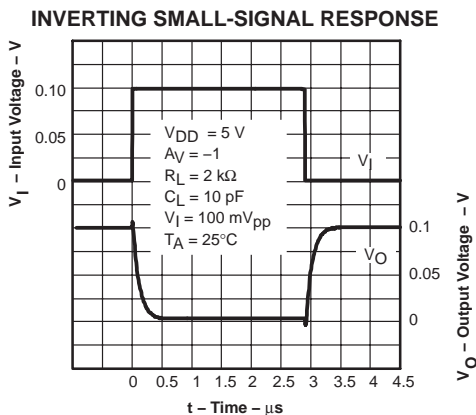


Figure 26

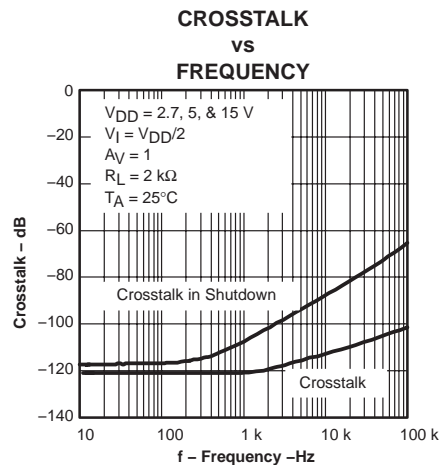


Figure 27

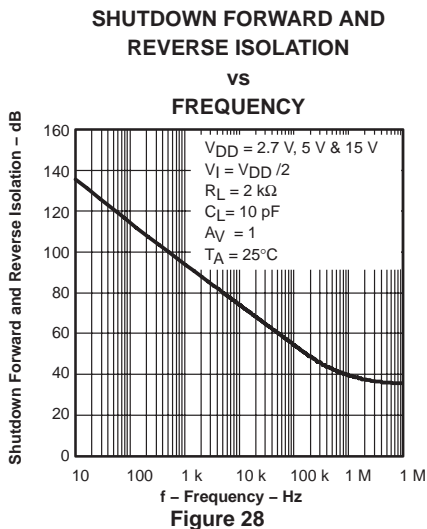


Figure 28

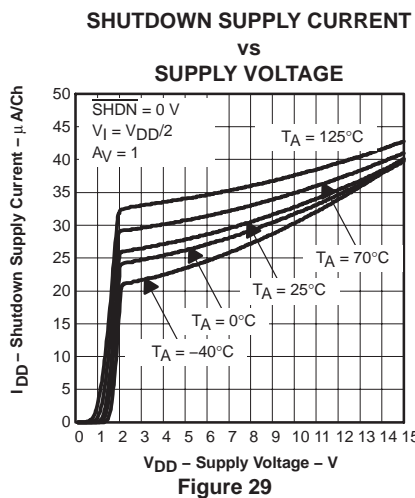


Figure 29

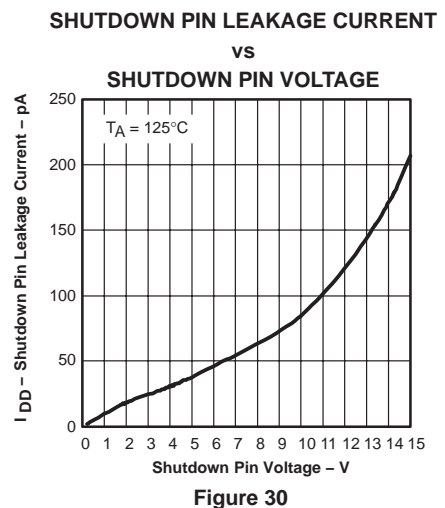


Figure 30



TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375
 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

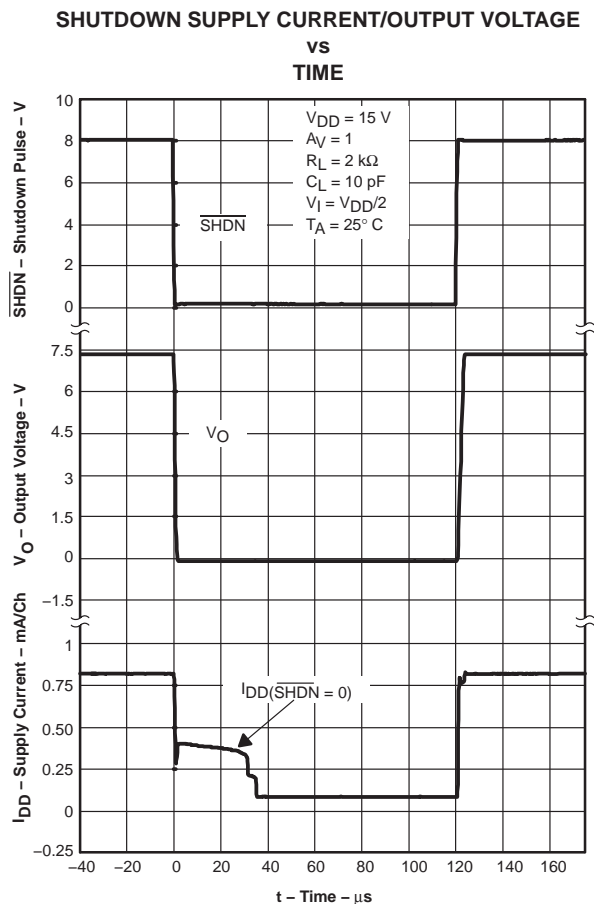


Figure 31

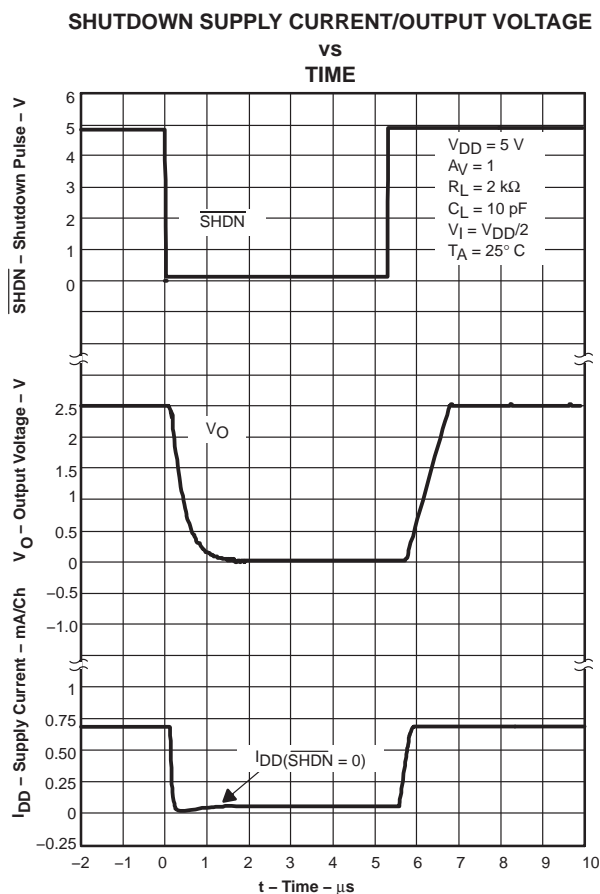


Figure 32

TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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APPLICATION INFORMATION

rail-to-rail input operation

The TLV237x input stage consists of two differential transistor pairs, NMOS and PMOS, that operate together to achieve rail-to-rail input operation. The transition point between these two pairs can be seen in Figures 1, 2, and 3 for a 2.7-V, 5-V, and 15-V supply. As the common-mode input voltage approaches the positive supply rail, the input pair switches from the PMOS differential pair to the NMOS differential pair. This transition occurs approximately 1.35 V from the positive rail and results in a change in offset voltage due to different device characteristics between the NMOS and PMOS pairs. If the input signal to the device is large enough to swing between both rails, this transition results in a reduction in common-mode rejection ratio (CMRR). If the input signal does not swing between both rails, it is best to bias the signal in the region where only one input pair is active. This is the region in Figures 1 through 3 where the offset voltage varies slightly across the input range and optimal CMRR can be achieved. This has the greatest impact when operating from a 2.7-V supply voltage.

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 33. A minimum value of 20 Ω should work well for most applications.

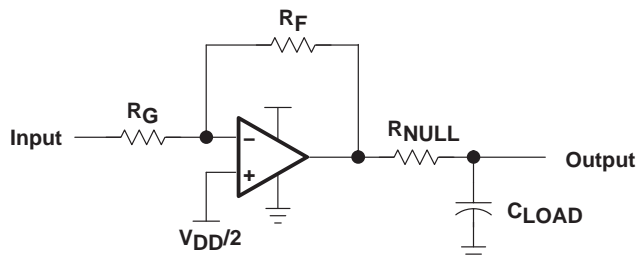


Figure 33. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

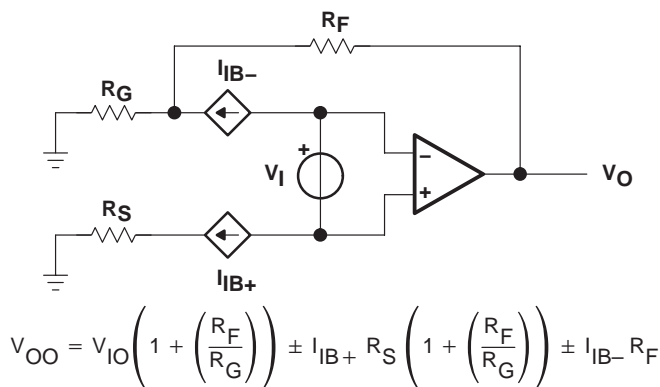


Figure 34. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 35).

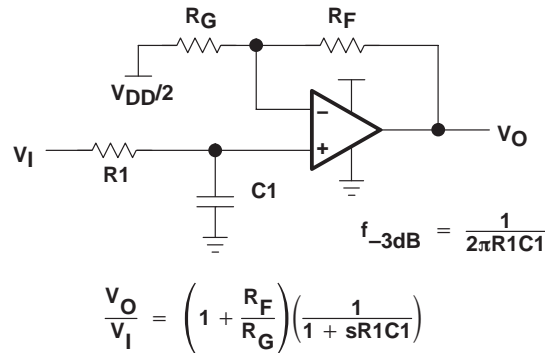


Figure 35. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

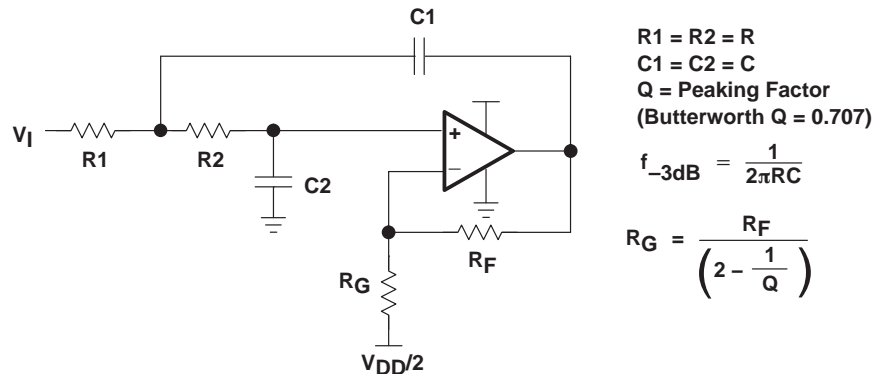


Figure 36. 2-Pole Low-Pass Sallen-Key Filter

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APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV237x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

shutdown function

Three members of the TLV237x family (TLV2370/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 25 μ A/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown.



TLV2370, TLV2371, TLV2372, TLV2373, TLV2374, TLV2375
FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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APPLICATION INFORMATION

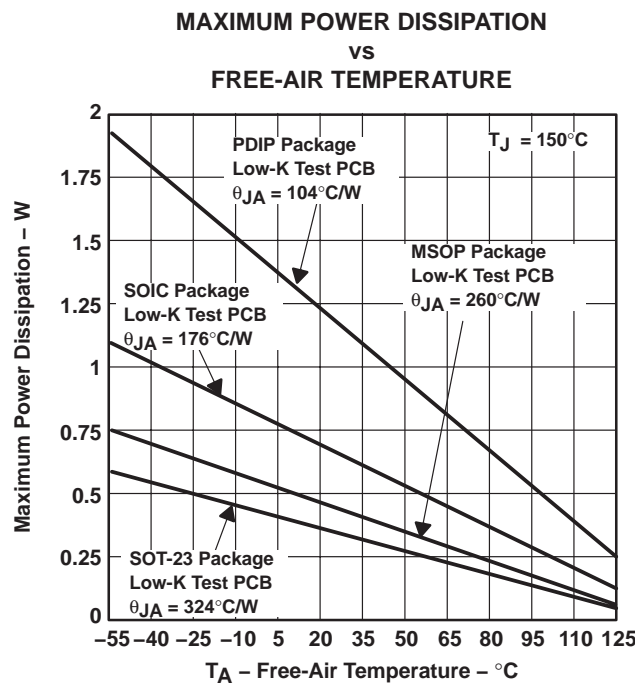
general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 37 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- P_D = Maximum power dissipation of TLV237x IC (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Free-ambient air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} = Thermal coefficient from junction to case
- θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 37. Maximum Power Dissipation vs Free-Air Temperature

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

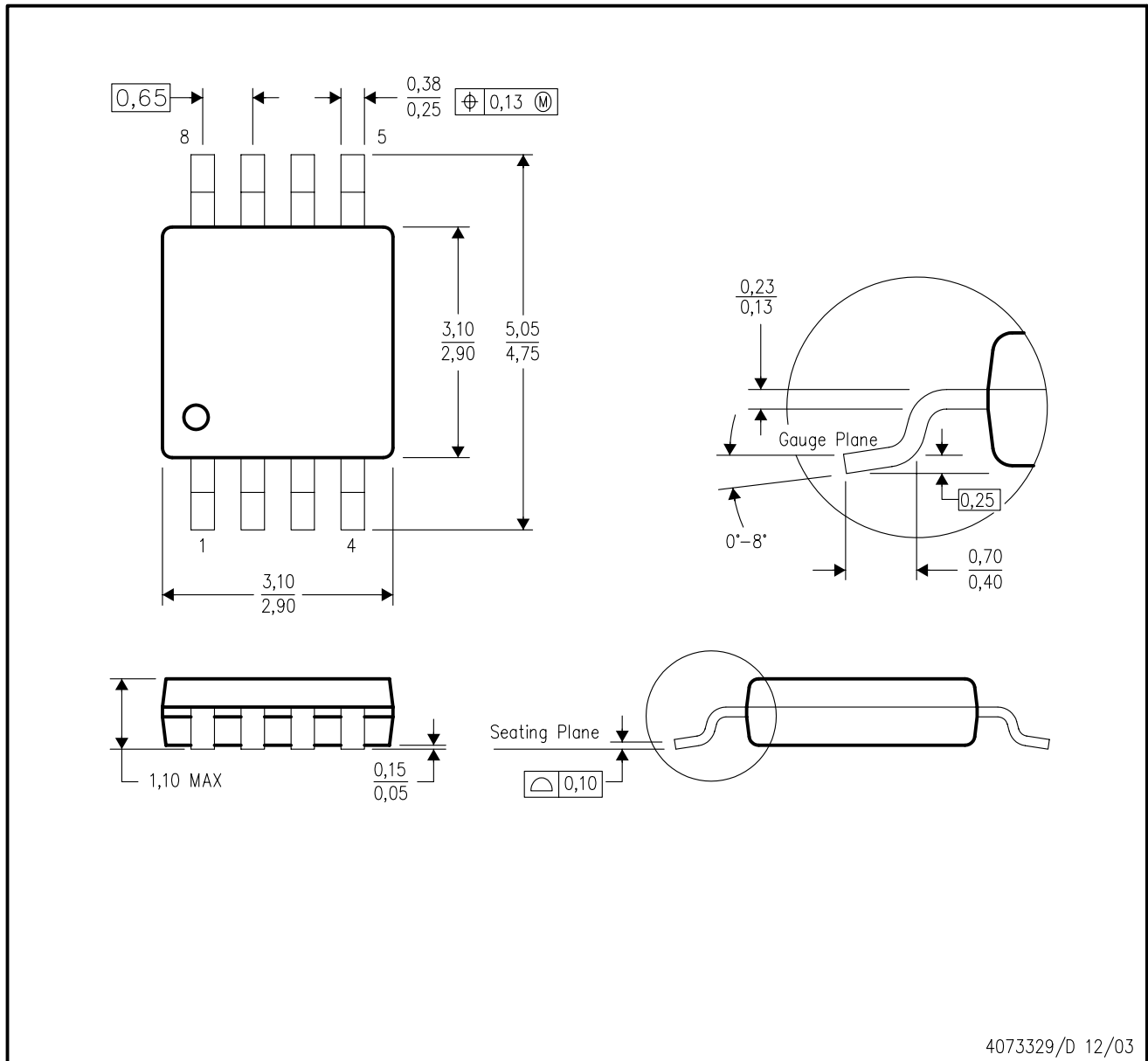


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation AA.

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation BA.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



4040047/E 09/01

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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