

TPS60150 5V/140mA Charge Pump Device

FEATURES

- 2.7V to 5.5V Input Voltage Range
- Fixed Output Voltage of 5.0V
- X2 Charge Pump
- 1.5 MHz Switching Frequency
- Maximum Output Current : 140mA
- 2X2 QFN With 0.8mm Height
- Typical 90 μ A Quiescent Current at no Load Condition (Skip mode)
- Hardware En/Disable Function
- Built-in Soft Start
- Built-in Under Voltage Lock Out Protection
- Thermal and Over Current Protection

APPLICATIONS

- USB OTG
- HDMI
- Portable Communication Devices
- Personal Digital Assistance
- PCMCIA Cards
- Cellular Phones
- Handheld Meters

DESCRIPTION

The TPS60150 is a switched capacitor voltage converter which produces a regulated, low noise, and low-ripple output voltage (5V) from an unregulated input voltage.

The 5V output can supply a minimum of 140mA current with a small 2X2 QFN package.

TPS60150 operates in *skip mode* when the load current falls below 8mA under typical condition. In skip mode operation, quiescent current is reduced to 90 μ A.

Only 3-external capacitors are needed to generate the output voltage, therefore saving PCB space.

Inrush current is limited by the soft start function during power on and power transient states.

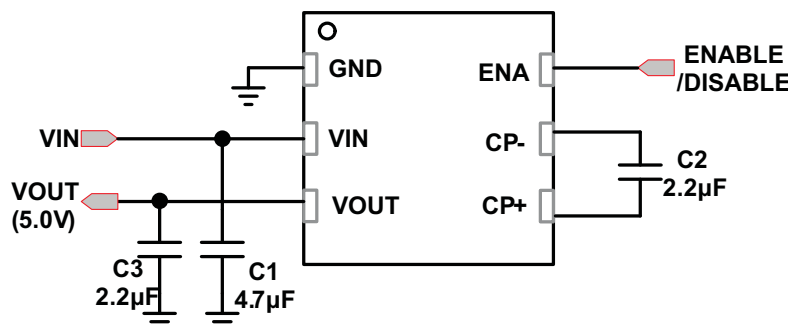


Figure 1. Typical Application Circuit

ORDERING INFORMATION

T _A	PART NUMBER ⁽¹⁾	OUTPUT VOLTAGE	PACKAGE ⁽²⁾	PACKAGE DESIGNATOR	ORDERING	PKG MARKING
–40°C to 85°C	TPS60150	5.0V	SON 2x2-6	DRV	TPS60150DRV	CGO

(1) The DRV (2-mm x 2-mm 6-terminal SON) package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel and T suffix to order quantities with 250 parts per reel.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		VALUE	UNIT
V _I	Input voltage range (all pins)	−0.3 to 7	V
	HBM ESD Rating ⁽²⁾	2	kV
	CDM ESD Rating ⁽³⁾	500	V
	MM ESD Rating ⁽⁴⁾	200	V
T _A	Operating temperature range	−40 to 85	°C
T _J	Maximum operating junction temperature	150	°C
T _{st}	Storage temperature	−55 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The Human body model (HBM) is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The testing is done according JEDECs EIA/JESD22-A114.
- (3) Charged Device Model
- (4) Machine Model (MM) is a 200pF capacitor discharged through a 500nH inductor with no series resistor into each pin. The testing is done according JEDECs EIA/JESD22-A115.

DISSIPATION RATINGS^{(1) (2)}

PACKAGE	THERMAL RESISTANCE RθJA	T _A = 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING
Low-K(1) DRV	140°C/W	715 mW	7.1 mW/°C	285 mW
High-K(2) DRV	65°C/W	1540 mW	15.4 mW/°C	615 mW

- (1) The JEDEC low-K (1s) board used to derive this data was a 3inx3in, two-layer board with 2-ounce copper traces on top of the board.
- (2) The JEDEC high-K (2s2p) board used to derive this data was a 3inx3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage range	2.7		5.5	V
T _A	Operating ambient temperature	−40		85	°C
T _J	Operating junction temperature	−40		125	°C
C _{in}	Input capacitor	2.2			μF
C _o	Output capacitor	2.2			μF
C _f	Flying capacitor	1.0			μF

ELECTRICAL CHARACTERISTICS

V_{IN}=3.6V, T_A = −40°C to 85°C, typical values are at T_A = 25°C, C1 = C3 = 2.2μF, C2 = 1.0μF (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
POWER STAGE							
V _{IN}	Input voltage range	2.7		5.5	V		
V _{UVLO}	Undervoltage lockout threshold		1.9	2.1			
I _Q	Operating quiescent current	I _{OUT} = 140 mA, Enable = V _{IN}		4.7	mA		
I _{Qskip}	Skip mode operating quiescent current	I _{OUT} = 0 mA, Enable=V _{IN} (No switching)		80	μA		
		I _{OUT} = 0 mA, Enable = V _{IN} (Minimum switching)		90	μA		
I _{SD}	Shut down current	2.7 V ≤ V _{IN} ≤ 5.5 V, Enable = 0 V		1	μA		
V _{OUT}	Output voltage ⁽¹⁾	I _{OUT} ≤ 50 mA, 2.7 V ≤ V _{IN} < 5.5V		4.8	5.0	5.2	V
V _{OUT(skip)}	Skip mode output voltage	I _{OUT} = 0 mA, 2.7 V ≤ V _{IN} ≤ 5.5 V		V _{OUT} +0.1		V	
F _{SW}	Switching frequency		1.5		MHz		

- (1) When in skip mode, Output voltage can exceed V_{OUT} spec because V_{OUT(skip)}=V_{OUT}+0.1.

ELECTRICAL CHARACTERISTICS (continued)

$V_{IN}=3.6V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$, typical values are at $T_A = 25^{\circ}C$, $C1 = C3 = 2.2\mu F$, $C2 = 1.0\mu F$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SS _{TIME}	Soft-start time	From the rising edge of enable to 90% output		150	μs
OUTPUT CURRENT					
I_{OUT_nom}	Maximum output current	V_{OUT} remains between 4.8 V and 5.2 V, $3.1 V \leq V_{IN} \leq 5.5 V$		120	mA
		$3.3 V < V_{IN} < 5.5 V$		140	
I_{OUT_short}	Short circuit current ⁽²⁾	$V_{OUT} = 0 V$		80	mA
RIPPLE VOLTAGE					
V_R	Output ripple voltage	$I_{OUT} = 140 mA$		30	mV
ENABLE CONTROL					
V_{HI}	Logic high input voltage	$2.7 V \leq V_{IN} \leq 5.5 V$		1.3	V_{IN} V
V_{LI}	Logic low input voltage			-0.2	0.4 V
I_{HI}	Logic high input current			1	μA
I_{LI}	Logic low input current			1	μA
THERMAL SHUTDOWN					
T_{SD}	Shutdown temperature			160	$^{\circ}C$
T_{RC}	Shutdown recovery			140	$^{\circ}C$

(2) TPS60150 has internal protection circuit to protect IC when V_{OUT} shorted to GND.

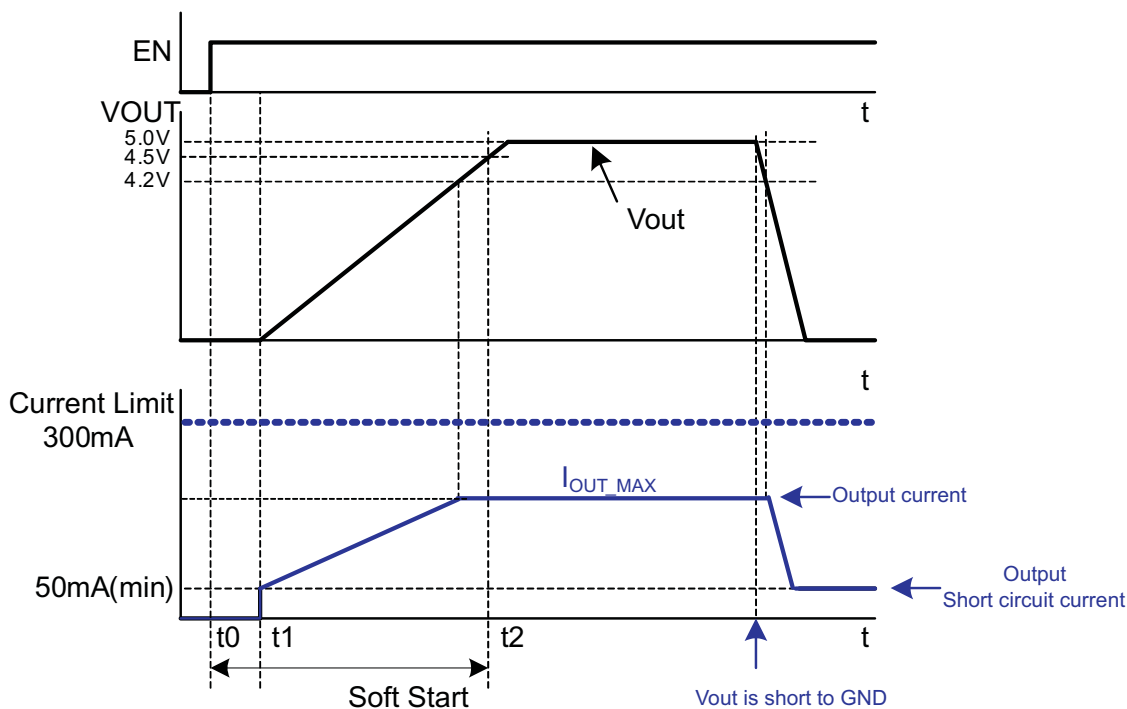
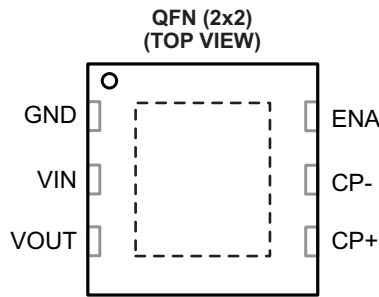


Figure 2. Maximum Output Current Capability and Short Circuit protection

DEVICE INFORMATION

PIN ASSIGNMENTS (TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	–	Ground
VIN	2	I	Supply voltage input
VOUT	3	O	Output, Connect to the output capacitor
CP+	4	–	Connect to the flying capacitor
CP–	5	–	Connect to the flying capacitor
ENA	6	I	Hardware Enable/Disable Pin (High = Enable)

FUNCTIONAL BLOCK DIAGRAM

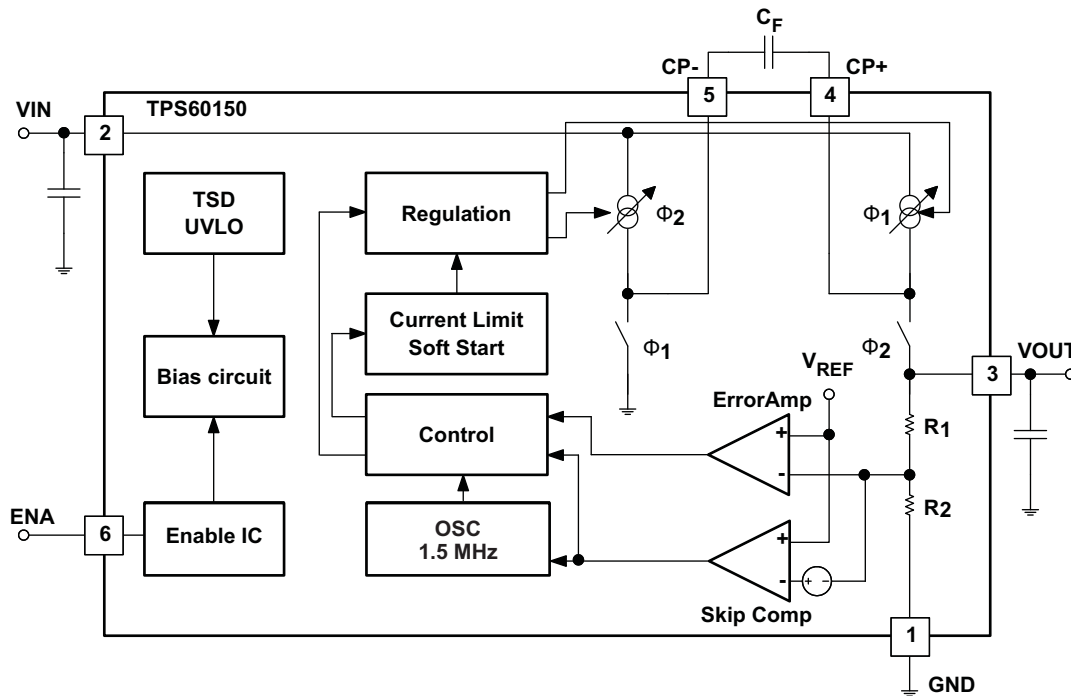


Figure 3. Functional Block Diagram

TYPICAL CHARACTERISTICS

Table of Graphs

TITLE	DESCRIPTION	FIGURE
Load Regulation Curve	Output voltage vs output current, V_{IN} = Variable, I_{OUT} = Sweep, Temperature = 25°C	Figure 4
Line Regulation Curve	Output voltage vs input voltage, V_{IN} = Sweep, I_{OUT} = Variable, Temperature = 25°C	Figure 5
Efficiency Curve	Efficiency vs input voltage, V_{IN} = Sweep, I_{OUT} = Variable, Temperature = 25°C	Figure 6
Quiescent Current Curve	Quiescent current vs input voltage, V_{IN} = Sweep, I_{OUT} = 0, Temperature = Variable	Figure 7
Maximum Output Current Curve	Maximum output current vs input voltage, V_{IN} = Sweep, Temperature = Variable	Figure 8
Load Transient Curve	Output voltage vs load current	Figure 9
		Figure 10
Output Ripple	Output ripple voltage (Skip mode)	Figure 11
		Figure 12
	Output ripple voltage (Normal mode)	Figure 13
		Figure 14
Power ON	Power on start up	Figure 15
		Figure 16
Enable / Disable	Soft start when enable	Figure 17
		Figure 18
TSD Operation	$V_{IN} = 5.5V$, $R_{LOAD} = 20\Omega$	Figure 19

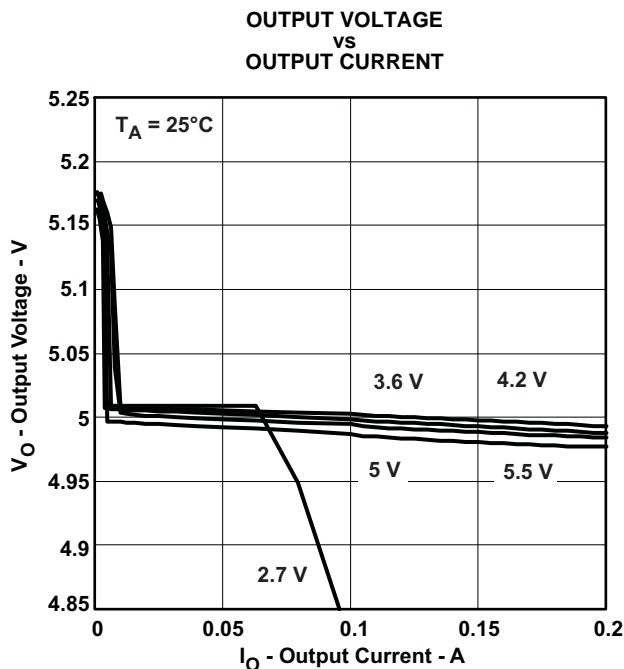


Figure 4.

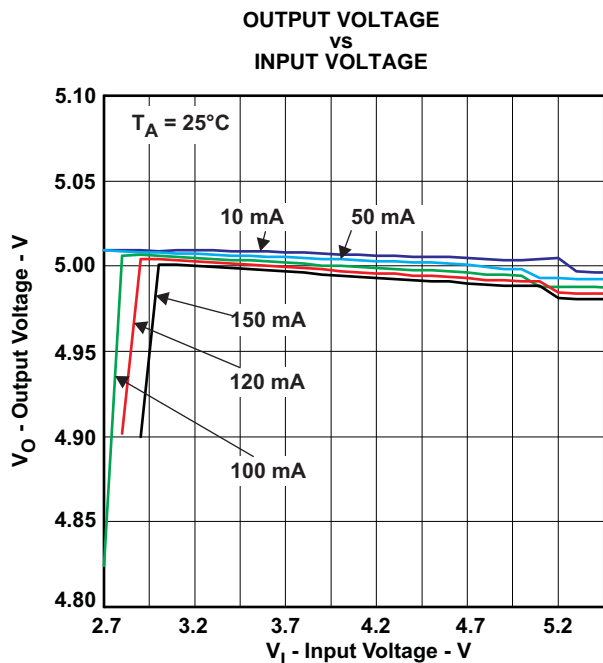


Figure 5.

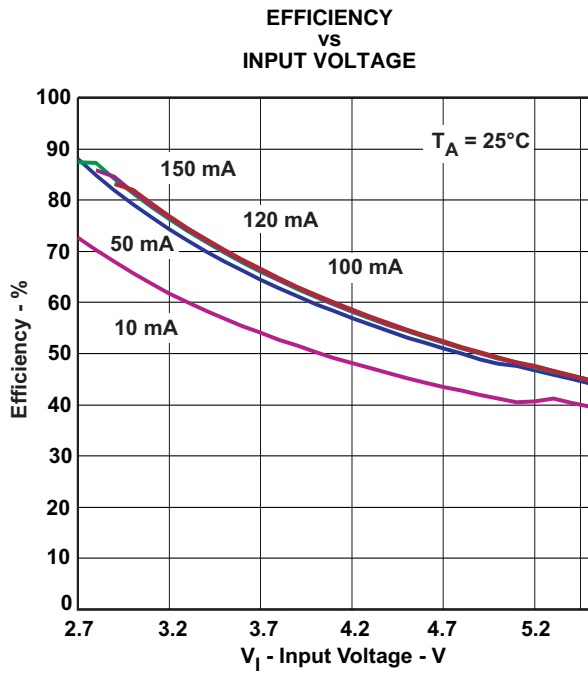


Figure 6.

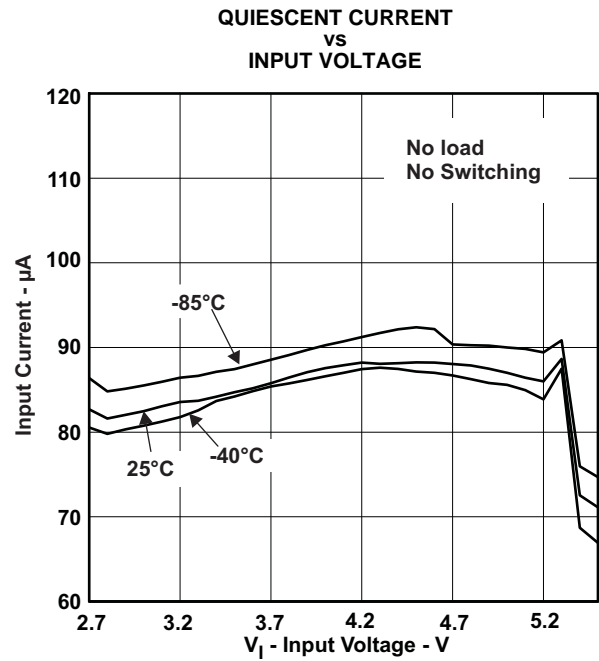


Figure 7.

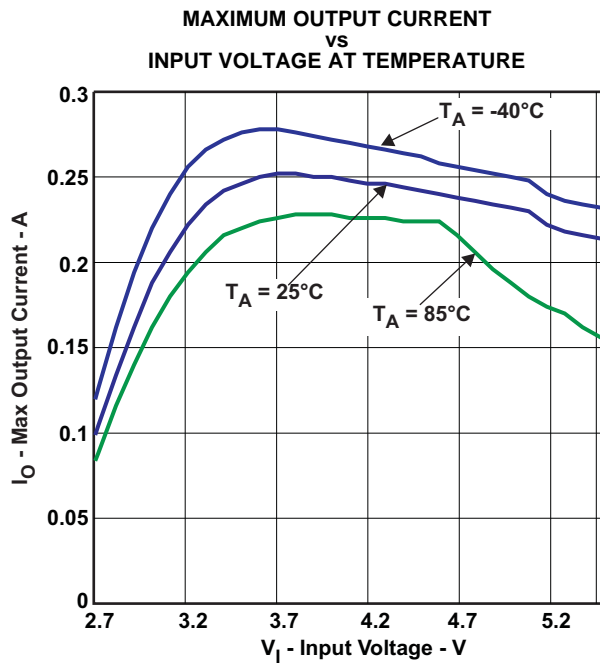
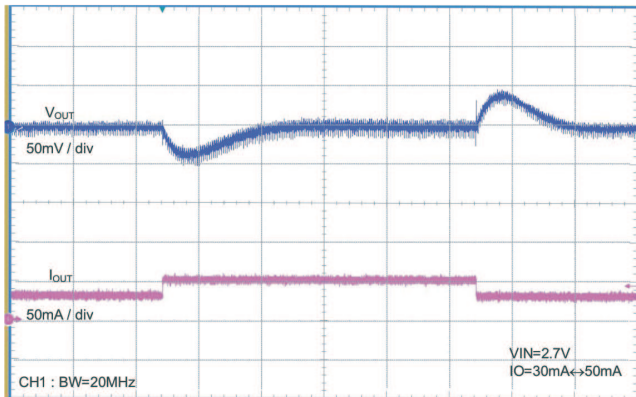


Figure 8.

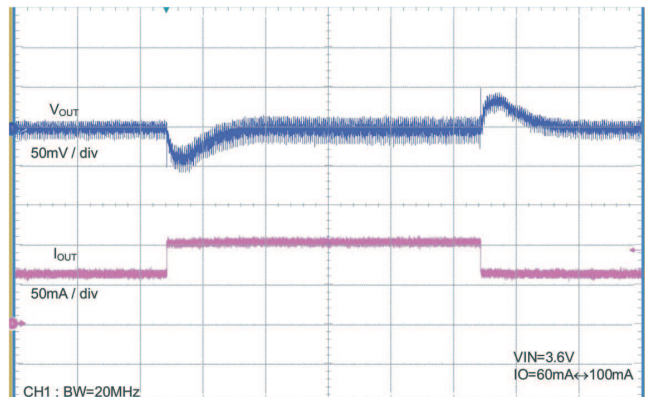
LOAD TRANSIENT RESPONSE
 $V_{IN} = 2.7\text{ V}$, $I_O = 30\text{ mA}$ to 50 mA



20 $\mu\text{s}/\text{div}$

Figure 9.

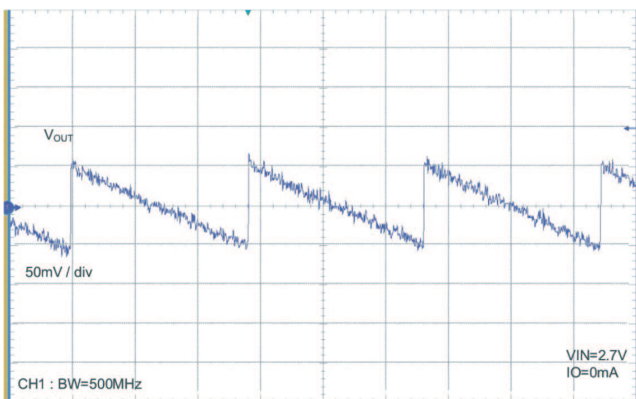
LOAD TRANSIENT RESPONSE
 $V_{IN} = 3.6\text{ V}$, $I_O = 60\text{ mA}$ to 100 mA



20 $\mu\text{s}/\text{div}$

Figure 10.

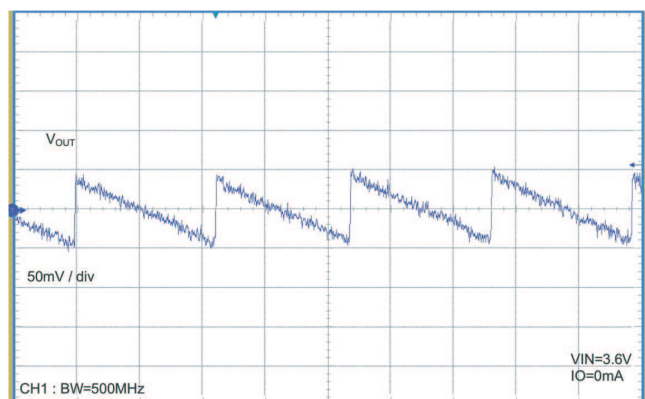
OUTPUT RIPPLE VOLTAGE (SKIP MODE)
 $V_{IN} = 2.7\text{ V}$, $I_O = 0\text{ mA}$



5 ms/div

Figure 11.

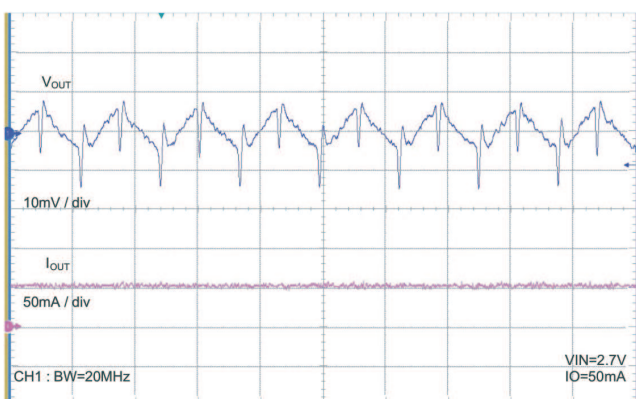
OUTPUT RIPPLE VOLTAGE (SKIP MODE)
 $V_{IN} = 3.6\text{ V}$, $I_O = 0\text{ mA}$



5 ms/div

Figure 12.

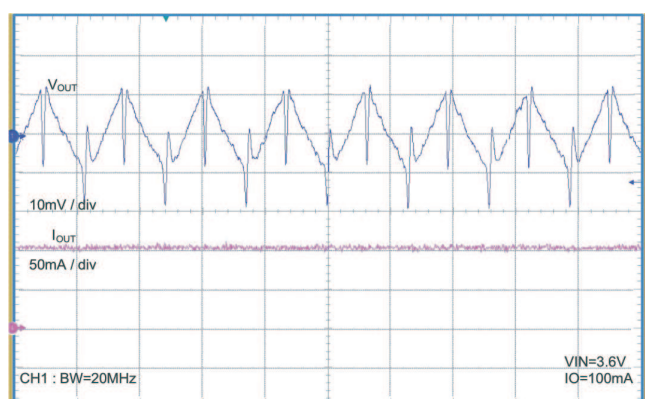
OUTPUT RIPPLE VOLTAGE (NORMAL MODE)
 $V_{IN} = 2.7\text{ V}$, $I_O = 50\text{ mA}$



500 ns/div

Figure 13.

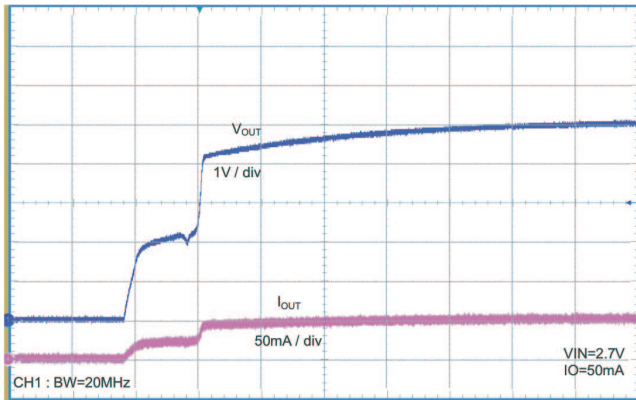
OUTPUT RIPPLE (NORMAL MODE)
 $V_{IN} = 3.6\text{ V}$, $I_O = 100\text{ mA}$



500 ns/div

Figure 14.

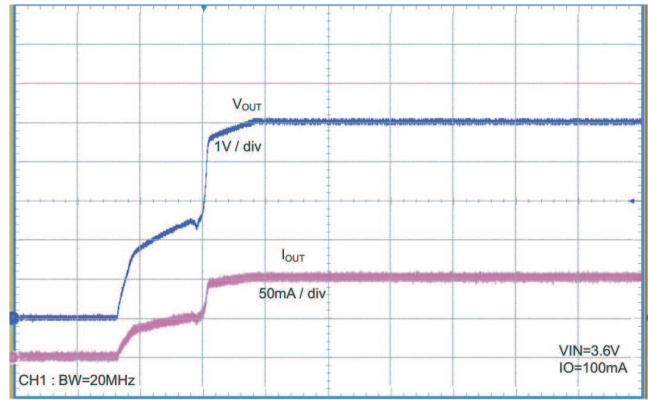
POWER ON
 $V_{IN} = 2.7\text{ V}$, $I_o = 50\text{ mA}$



1 ms/div

Figure 15.

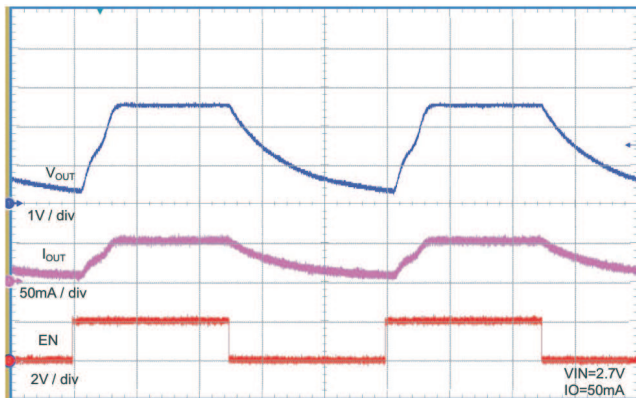
POWER ON
 $V_{IN} = 3.6\text{ V}$, $I_o = 100\text{ mA}$



1 ms/div

Figure 16.

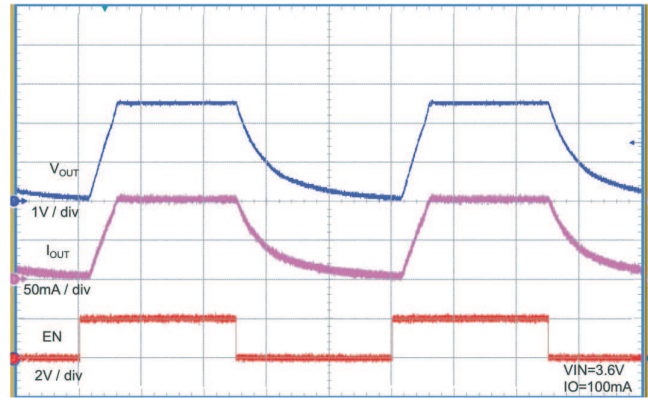
ENABLE / DISABLE
 $V_{IN} = 2.7\text{ V}$, $I_o = 50\text{ mA}$



200 $\mu\text{s}/\text{div}$

Figure 17.

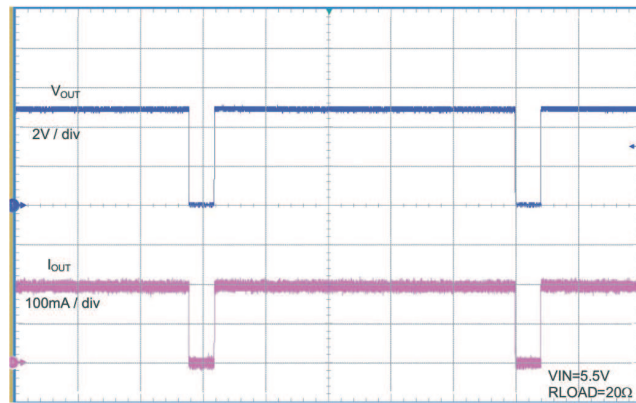
ENABLE / DISABLE
 $V_{IN} = 3.6\text{ V}$, $I_o = 100\text{ mA}$



200 $\mu\text{s}/\text{div}$

Figure 18.

THERMAL SHUT DOWN OPERATION
 $V_{IN} = 5.5\text{ V}$, $R_{LOAD} = 20\Omega$



50 ms/div

Figure 19.

APPLICATION INFORMATION

APPLICATION OVERVIEW

Most of today's battery-powered portable electronics allow and/or require data transfer with a PC. One of the fastest data transfer protocols is via USB On the Go (OTG). As Figure 20 shows, the USB OTG circuitry in the portable device requires a 5-V power rail and up to 140mA of current. The TPS60150 may be utilized to provide a 5-V power rail in a battery powered system.

Alternatively, low-cost portable electronics with small LCD displays require a low-cost solution for providing the WLED backlight. As shown in Figure 21, the TPS60150 can also be used to drive several WLEDs in parallel, with the help of ballast resistors.

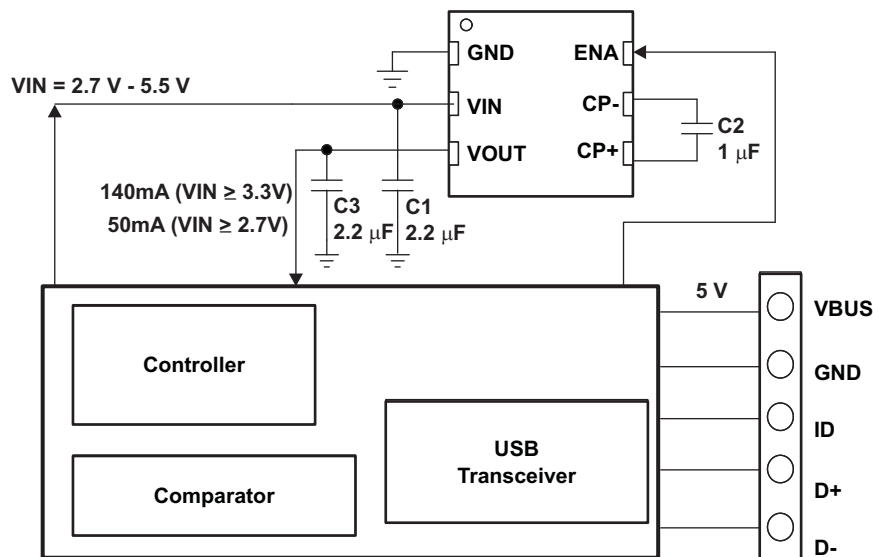


Figure 20. Application Circuit for OTG System

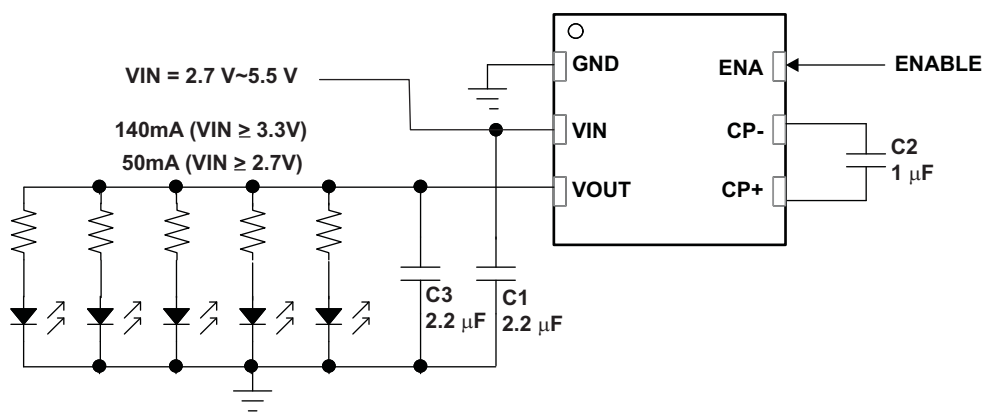


Figure 21. Application Circuit for Driving White LEDs

BASIC OPERATION PRINCIPLE

The TPS60150, regulated charge pump, provides a regulated output voltage for various input voltages. The TPS60150 regulates the voltage across the flying capacitor to 2.5V and controls the voltage drop of Q1 and Q2 while a conversion clock with 50% duty cycle drives the FETs.

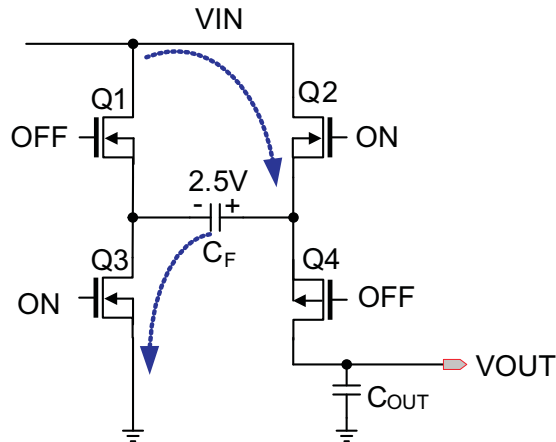


Figure 22. Charging Mode

During the first half cycle, Q2 and Q3 transistors are turned on and flying capacitor, C_F , will be charged to 2.5V ideally.

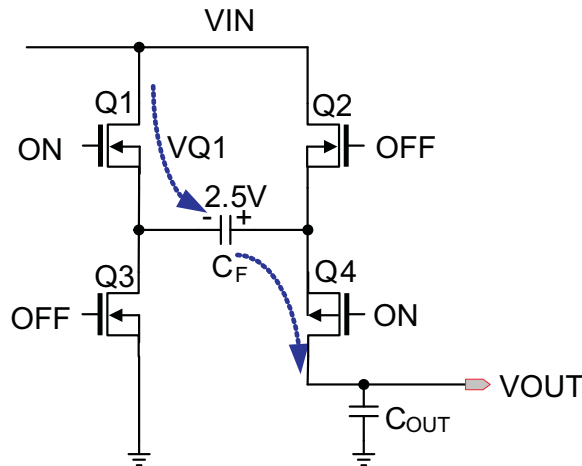


Figure 23. Discharging Mode

During the second half cycle, Q1 and Q4 transistors are turned on. Capacitor C_F will then be discharged to output.

The output voltage can be calculated as follows:

$$V_{out} = V_{IN} - V_{Q1} + V(C_F) - V_{Q4} = V_{IN} - V_{Q1} + 2.5V - V_{Q4} = 5V. \text{ (Ideal)}$$

The output voltage is regulated by output feedback and an internally compensated voltage control loop.

NORMAL MODE AND SKIP MODE OPERATION

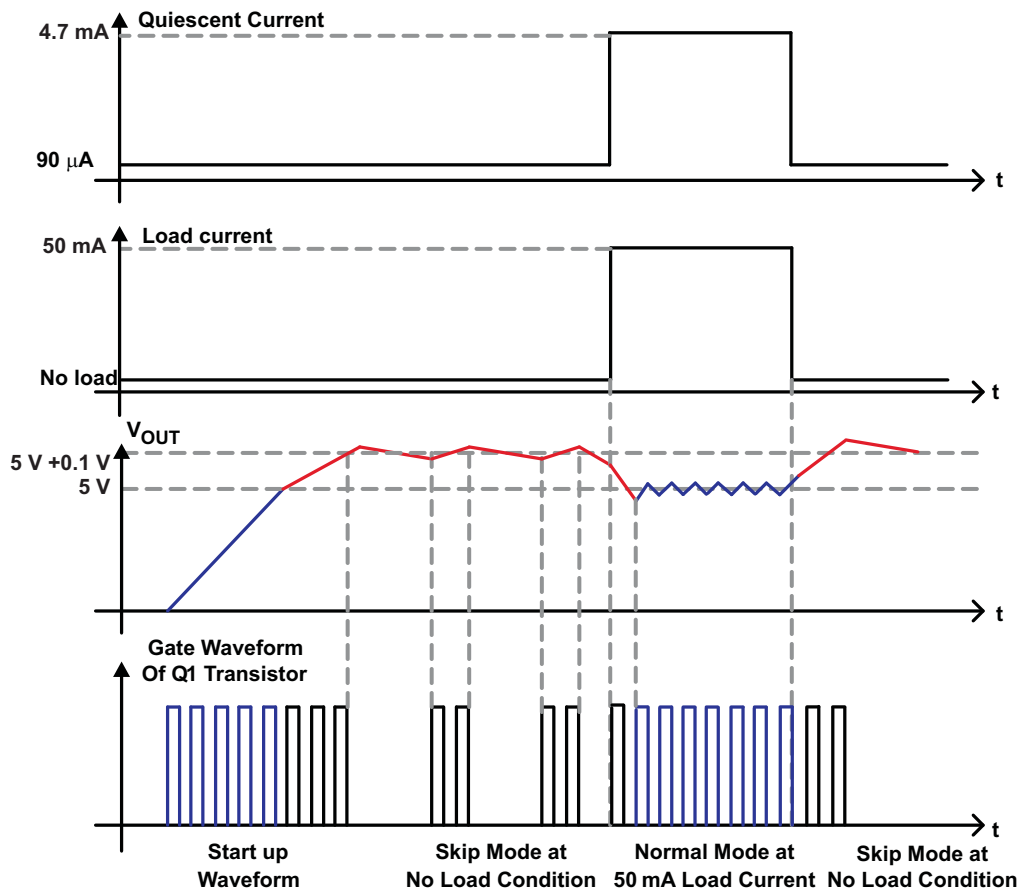


Figure 24. Normal Mode and Skip Mode Operation

The TPS60150 has skip mode operation as shown in [Figure 24](#). The TPS60150 enters skip mode if the output voltage reaches $5V+0.1V$ and the load current is below $8mA$ (typ). In Skip Mode, the TPS60150 disables the oscillator and decreases the pre_bias current of the output stage to reduce the power consumption. Once the output voltage dips below threshold voltage, $5V+0.1V$, the TPS60150 begins switching to increase output voltage until the output reaches $5V+0.1V$. When the output voltage dips below $5V$, the TPS60150 returns to normal PWM mode; thereby re-enabling the oscillator and increasing the pre_bias current of the output stage to supply output current.

The skip threshold voltage and current depend on input voltage and output current conditions.

SHORT CIRCUIT PROTECTION

The TPS60150 has internal short circuit protection to protect the IC when the output is shorted to ground. To avoid damage when output is shorted to ground, the short circuit protection circuitry senses output voltage and clamps the maximum output current to $80mA$ (typ).

THERMAL SHUT DOWN PROTECTION

The regulator has thermal shutdown circuitry that protects it from damage caused by overload conditions. The thermal protection circuitry disables the output when the junction temperature reached approximately $160^{\circ}C$, allowing the device to cool. When the junction temperature cools to approximately $140^{\circ}C$, the output circuitry is automatically re-enabled. Continuously running the regulator into thermal shutdown can degrade reliability. The regulator also provides current limit to protect itself and the load.

SHUTDOWN MODE

An enable pin on the regulator may be used to place the device into an energy-saving shutdown mode. In this mode, the output is disconnected from the input and the input quiescent current is reduced to 1µA maximum.

CAPACITOR SELECTION

For minimum output voltage ripple, the output capacitor (C_{OUT}) should be a surface-mount ceramic capacitor. Tantalum capacitors generally have a higher Effective Series Resistance (ESR) and may contribute to higher output voltage ripple. Leaded capacitors also increase ripple due to the higher inductance of the package itself. To achieve the best operation with low input voltage and high load current, the input and flying capacitors (C_{IN} and C_F , respectively) should also be surface-mount ceramic types.

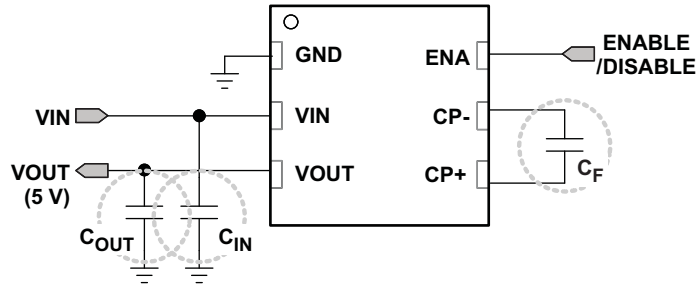


Figure 25. Capacitors

Generally, C_{FLY} can be calculated by simple equation as follows,

$$Q_{charging} = C \times v = C_{FLY} \times \Delta V_{CFLY},$$

$$Q_{discharging} = i_{discharge} \times t = 2 \times I_{LOAD(MAX)} \times \left(\frac{T}{2}\right), \text{ half duty.} \tag{1}$$

$$\therefore 2 \times I_{LOAD(MAX)} \times \left(\frac{T}{2}\right) = C_{FLY} \times \Delta V_{CFLY}$$

Both equation should be same,

$$\therefore C_{FLY} \geq \frac{2 \times I_{LOAD(MAX)} \times \left(\frac{T}{2}\right)}{\Delta V_{CFLY}} = \frac{I_{LOAD(MAX)}}{\Delta V_{CFLY} \times f} \tag{2}$$

If $I_{LOAD} = 140 \text{ mA}$, $f = 1.5\text{MHz}$, and $\Delta V_{CFLY} = 100\text{mV}$, the minimum value of the flying capacitor should be $1\mu\text{F}$.

Output capacitance, C_{OUT} , is also strongly related to output ripple voltage and loop stability,

$$V_{OUT(RIPPLE)} = \frac{I_{LOAD(MAX)}}{(2 \times f \times C_{OUT})} + 2I_{LOAD(MAX)} \times ESR_{COUT} \tag{3}$$

The minimum output capacitance for all output levels is $2.2\mu\text{F}$ due to control stability. Larger ceramic capacitors or low ESR capacitors can be used to lower the output ripple voltage.

Suggested Capacitors (Input / Output / Flying Capacitor)

Manufacturer	Part number	Value	Tolerance	Dielectric material	Package Size	Rated working voltage
		4.7µF 2.2µF		X7R		6.3V

The efficiency of the charge pump regulator varies with the output voltage, the applied input voltage and the load current.

The approximate efficiency in normal operating mode is given by:

$$\text{Efficiency(\%)} = \frac{\text{PD(out)}}{\text{PD(in)}} \times 100 = \frac{V_{\text{OUT}} \times I_{\text{OUT}}}{V_{\text{IN}} \times I_{\text{IN}}} \times 100, I_{\text{IN}} = 2 \times I_{\text{OUT}} + I_{\text{Q}} \quad (4)$$

$$\text{Efficiency(\%)} = \frac{V_{\text{OUT}}}{2 \times V_{\text{IN}}} \times 100 (I_{\text{IN}} = 2 \times I_{\text{OUT}}) \quad \text{Quiescent current was neglected.} \quad (5)$$

PCB LAYOUT

Large transient currents flow in the VIN, VOUT, and GND traces. To minimize both input and output ripple, keep the capacitors as close as possible to the regulator using short, direct circuit traces.

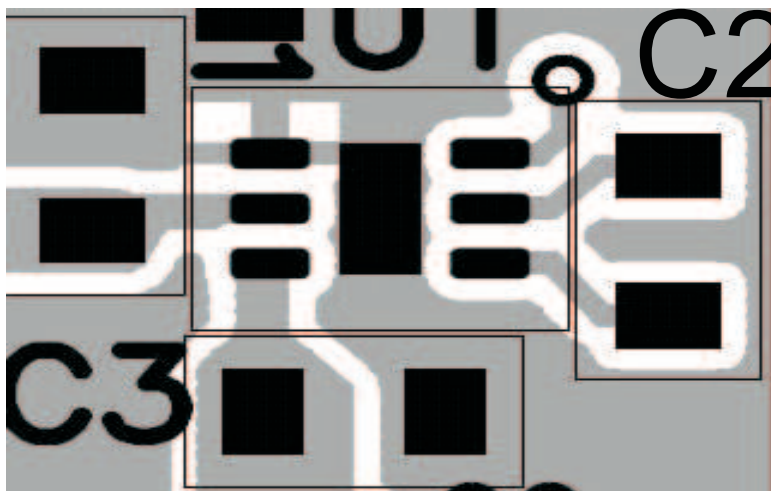


Figure 26. Recommended PCB Layout

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS60150DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS60150DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

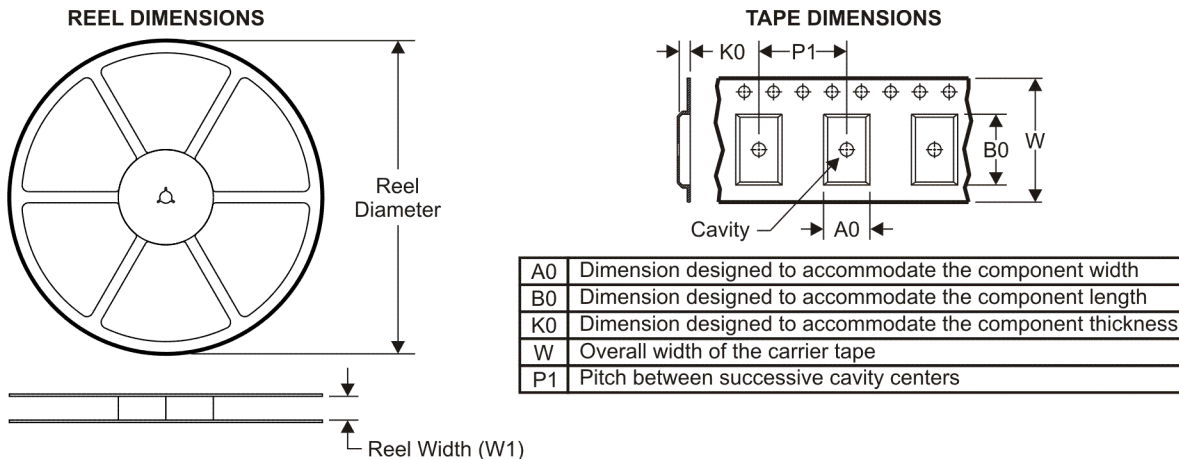
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

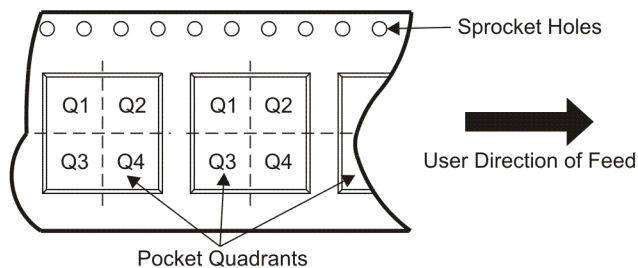
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60150DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
TPS60150DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2

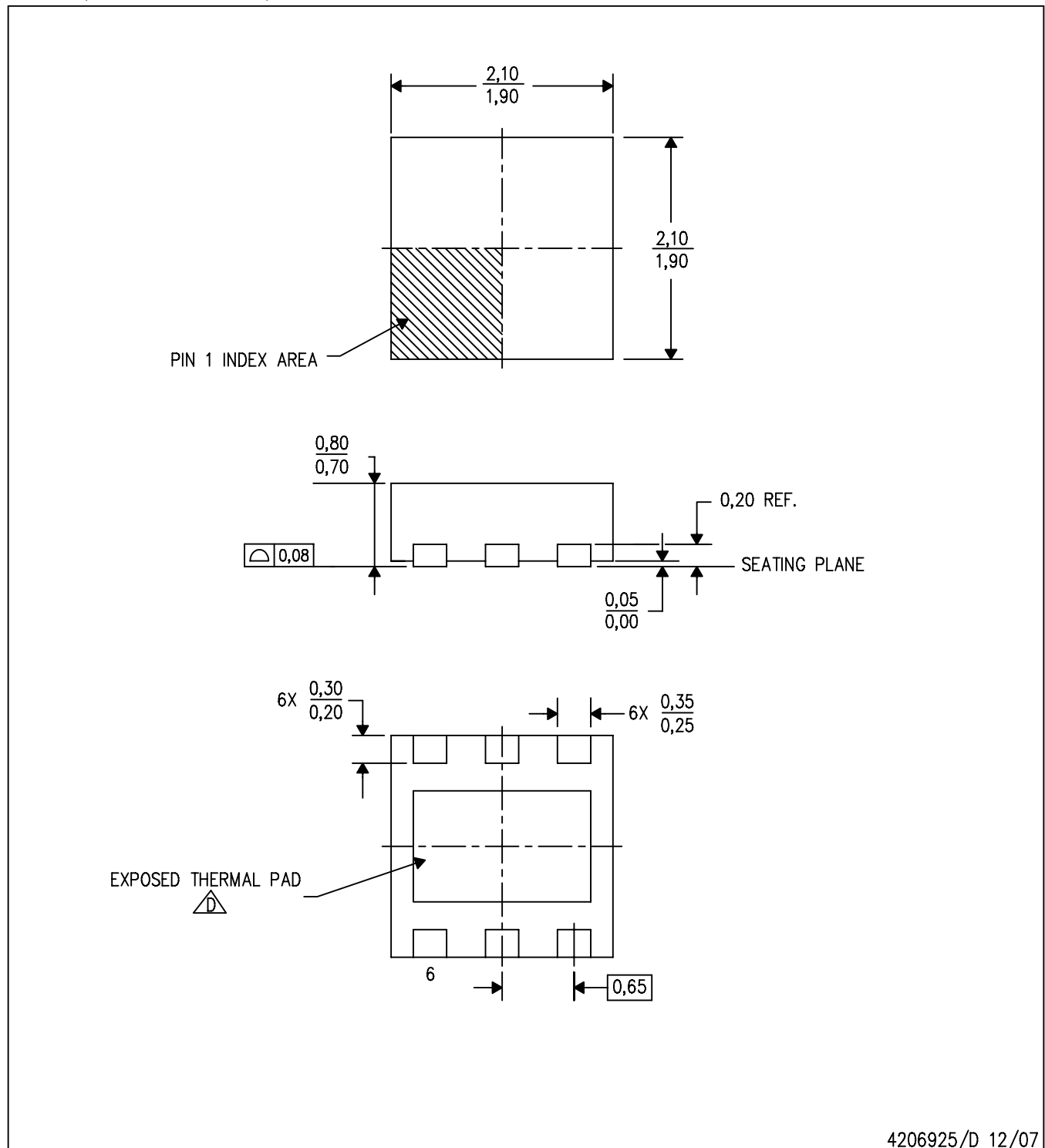
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60150DRVR	SON	DRV	6	3000	346.0	346.0	29.0
TPS60150DRVT	SON	DRV	6	250	190.5	212.7	31.8

DRV (S-PDSO-N6)

PLASTIC SMALL OUTLINE



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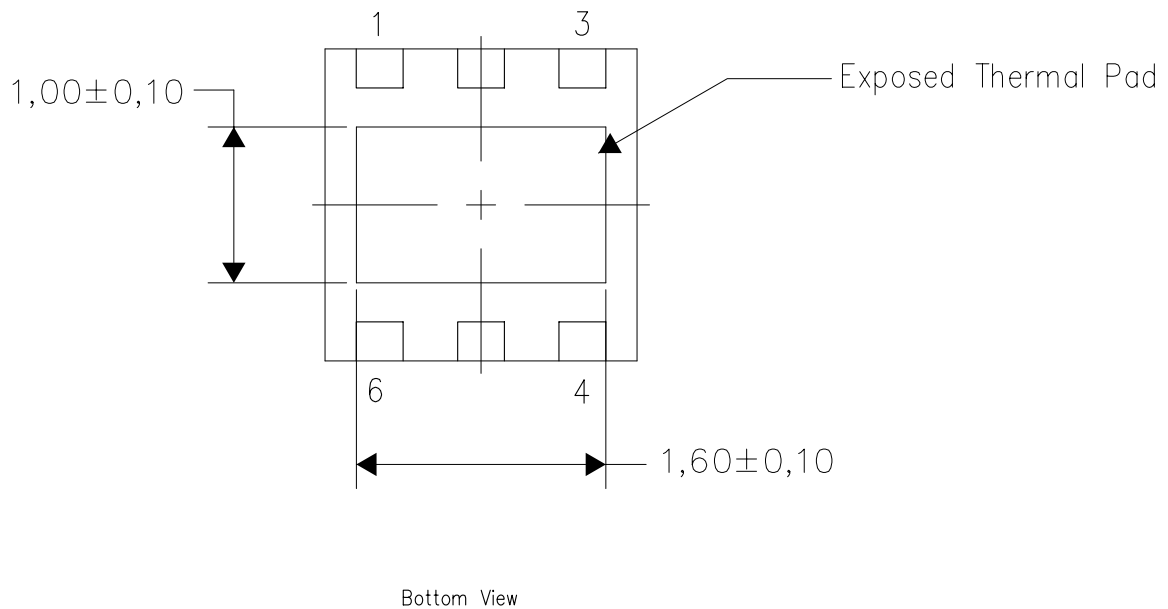
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
-  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

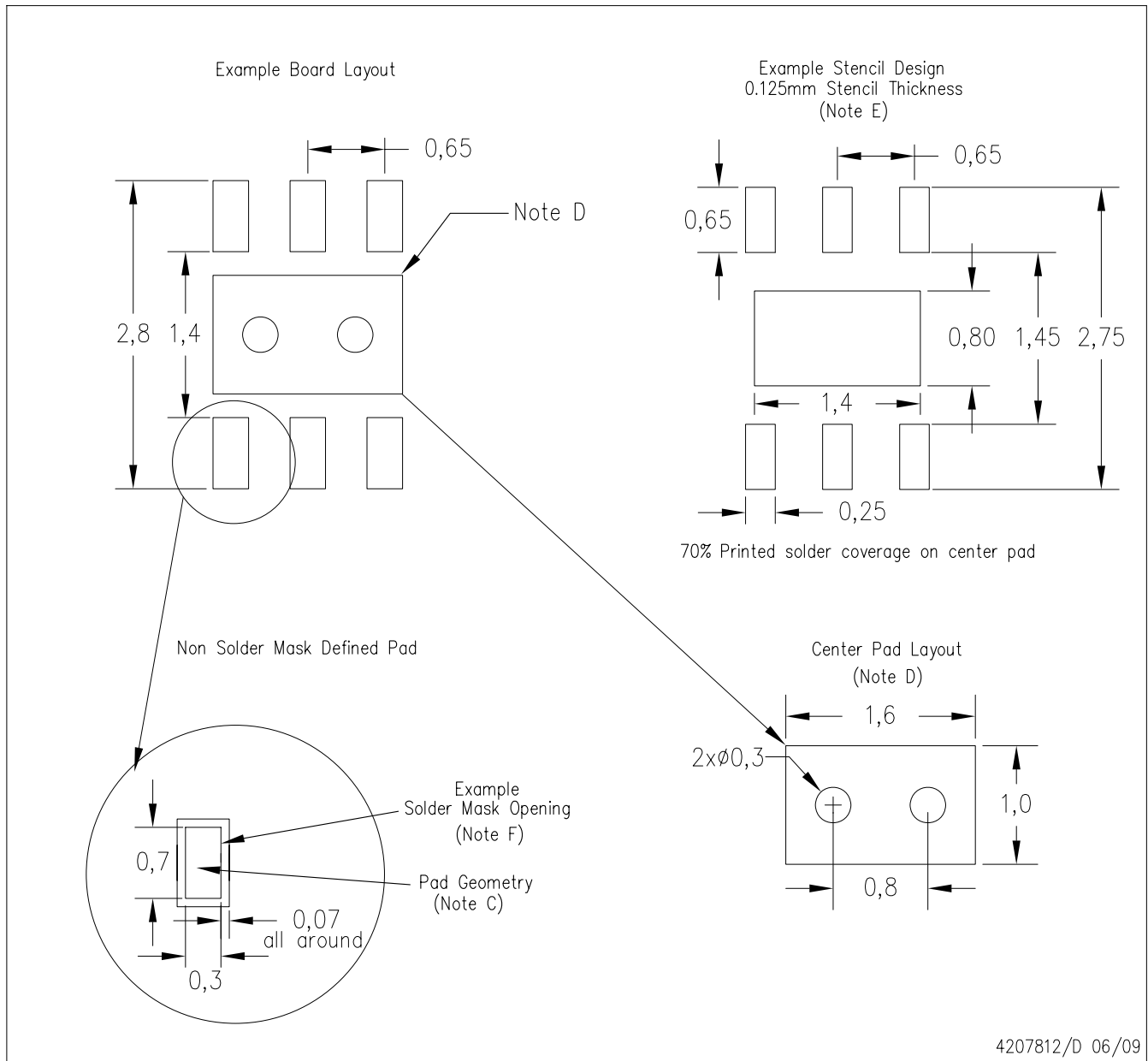
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRV (S-PWSON-N6)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for solder mask tolerances.

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