Qualified for Automotive Applications
ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
1-A Low-Dropout (LDO) Voltage Regulator
Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3-V, 3.3-V, 5-V Fixed-Output and Adjustable Versions
Dropout Voltage Down to 230 mV at 1 A (TPS76750)
Ultralow 85-µA Typical Quiescent Current
Fast Transient Response

2% Tolerance Over Specified Conditions for Fixed-Output Versions
Open Drain Power-On Reset With 200-ms Delay (See TPS768xx for PG Option)
20-Pin TSSOP PowerPAD™ (PWP) Package
Thermal Shutdown Protection

These devices are designed to have a fast transient response and be stable with 10-µF low ESR capacitors. This combination provides high performance at a reasonable cost.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 1 A for the TPS76750) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 µA over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This low-dropout (LDO) family also features a sleep mode; applying a TTL high signal to the enable (EN) input shuts down the regulator, reducing the quiescent current to 1 µA at T<sub>J</sub> = 25°C.

The RESET output of the TPS767xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS767xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

The TPS767xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3-V, 3.3-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS767xx family is available in a 20-pin PWP package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
† See application information section for capacitor selection details.

Figure 1. Typical Application Configuration (for Fixed Output Options)

functional block diagram—adjustable version

V_{\text{ref}} = 1.1834 \text{ V}
functional block diagram—fixed-voltage version

![Functional Block Diagram](image)

**Terminal Functions**

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>5</td>
<td>I</td>
<td>Enable</td>
</tr>
<tr>
<td>FB/NC</td>
<td>15</td>
<td>I</td>
<td>Feedback voltage for adjustable device (no connect for fixed options)</td>
</tr>
<tr>
<td>GND</td>
<td>3</td>
<td></td>
<td>Regulator ground</td>
</tr>
<tr>
<td>GND/HSINK</td>
<td>1, 2, 9, 10, 11, 12, 19, 20</td>
<td></td>
<td>Ground/heatsink</td>
</tr>
<tr>
<td>IN</td>
<td>6, 7</td>
<td>I</td>
<td>Input voltage</td>
</tr>
<tr>
<td>NC</td>
<td>4, 8, 17, 18</td>
<td></td>
<td>No connect</td>
</tr>
<tr>
<td>OUT</td>
<td>13, 14</td>
<td>O</td>
<td>Regulated output voltage</td>
</tr>
<tr>
<td>RESET</td>
<td>16</td>
<td>O</td>
<td>Reset</td>
</tr>
</tbody>
</table>

**v_{ref} = 1.1834 V**
† \( V_{\text{res}} \) is the minimum input voltage for a valid \textit{RESET}. The symbol \( V_{\text{res}} \) is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ \( V_{\text{IT}} \) -Trip voltage is typically 5% lower than the output voltage (95\%\( V_O \)) \( V_{\text{IT}} - \) to \( V_{\text{IT}} + \) is the hysteresis voltage.
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

- Input voltage range‡, \( V_I \) .......................................................... \(-0.3 \, \text{V} \) to \( 13.5 \, \text{V} \)
- Voltage range at \( EN \) .......................................................... \(-0.3 \, \text{V} \) to \( V_I + 0.3 \, \text{V} \)
- Maximum RESET voltage .................................................. \( 16.5 \, \text{V} \)
- Peak output current .......................................................... Internally limited
- Output voltage, \( V_O \) (OUT, FB) .................................................. \( 7 \, \text{V} \)
- Continuous total power dissipation .................................................. See dissipation rating tables
- Operating virtual junction temperature range, \( T_J \) .................................................. \(-40^\circ \text{C} \) to \( 125^\circ \text{C} \)
- Storage temperature range, \( T_{stg} \) .................................................. \(-65^\circ \text{C} \) to \( 150^\circ \text{C} \)
- ESD rating, Human-Body Model (HBM) ........................................ 2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network terminal ground.

**DISSIPATION RATING TABLE – FREE-AIR TEMPERATURES**

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>AIR FLOW (CFM)</th>
<th>( T_A &lt; 25^\circ \text{C} ) POWER RATING</th>
<th>DERATING FACTOR ABOVE ( T_A = 25^\circ \text{C} )</th>
<th>( T_A = 70^\circ \text{C} ) POWER RATING</th>
<th>( T_A = 85^\circ \text{C} ) POWER RATING</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWP§</td>
<td>0</td>
<td>2.9 W</td>
<td>23.5 mW/°C</td>
<td>1.9 W</td>
<td>1.5 W</td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>4.3 W</td>
<td>34.6 mW/°C</td>
<td>2.8 W</td>
<td>2.2 W</td>
</tr>
<tr>
<td>PWP¶</td>
<td>0</td>
<td>3 W</td>
<td>23.8 mW/°C</td>
<td>1.9 W</td>
<td>1.5 W</td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>7.2 W</td>
<td>57.9 mW/°C</td>
<td>4.6 W</td>
<td>3.8 W</td>
</tr>
</tbody>
</table>

§ This parameter is measured with the recommended copper heat-sink pattern on a 1-layer PCB, 5-in x 5-in PCB, 1-oz copper, 2-in x 2-in coverage (4 in²).
¶ This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in x 2-in PCB, 1-oz copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²). For more information, refer to TI technical brief SLMA002.

**recommended operating conditions**

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage, ( V_I )#</td>
<td>2.7</td>
<td>10</td>
<td>\text{V}</td>
</tr>
<tr>
<td>Output voltage range, ( V_O )</td>
<td>1.5</td>
<td>5.5</td>
<td>\text{V}</td>
</tr>
<tr>
<td>Output current, ( I_O ) (see Note 1)</td>
<td>0</td>
<td>1.0</td>
<td>\text{A}</td>
</tr>
<tr>
<td>Operating virtual junction temperature, ( T_J ) (see Note 1)</td>
<td>(-40 )</td>
<td>125</td>
<td>°\text{C}</td>
</tr>
</tbody>
</table>

# To calculate the minimum input voltage for your maximum output current, use the following equation: \( V_I(\text{min}) = V_O(\text{max}) + V_D(\text{max load}) \).

NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.
electrical characteristics over recommended operating free-air temperature range, $V_I = V_O(\text{typ}) + 1\, \text{V}$, $I_O = 1\, \text{mA}$, $EN = 0\, \text{V}$, $C_O = 10\, \mu\text{F}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage (10 $\mu\text{A}$ to 1 A load)</td>
<td>$1.5, \text{V} \leq V_O \leq 5.5, \text{V}$, $T_J = 25^\circ\text{C}$</td>
<td>$V_O$</td>
<td>$0.98V_O$</td>
<td>$1.02V_O$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$1.5, \text{V} \leq V_O \leq 5.5, \text{V}$, $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$</td>
<td>$V_O$</td>
<td>$1.470$</td>
<td>$1.530$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ\text{C}$, $2.7, \text{V} &lt; V_IN &lt; 10, \text{V}$</td>
<td>$1.5$</td>
<td>$1.02V_O$</td>
<td>$1.02V_O$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$, $2.7, \text{V} &lt; V_IN &lt; 10, \text{V}$</td>
<td>$1.764$</td>
<td>$1.836$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ\text{C}$, $3.5, \text{V} &lt; V_IN &lt; 10, \text{V}$</td>
<td>$2.450$</td>
<td>$2.550$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$, $3.5, \text{V} &lt; V_IN &lt; 10, \text{V}$</td>
<td>$2.646$</td>
<td>$2.754$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ\text{C}$, $3.7, \text{V} &lt; V_IN &lt; 10, \text{V}$</td>
<td>$2.7$</td>
<td>$2.754$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$, $3.7, \text{V} &lt; V_IN &lt; 10, \text{V}$</td>
<td>$2.940$</td>
<td>$3.060$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ\text{C}$, $4.0, \text{V} &lt; V_IN &lt; 10, \text{V}$</td>
<td>$3.0$</td>
<td>$3.060$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$, $4.0, \text{V} &lt; V_IN &lt; 10, \text{V}$</td>
<td>$3.234$</td>
<td>$3.366$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ\text{C}$, $4.3, \text{V} &lt; V_IN &lt; 10, \text{V}$</td>
<td>$3.3$</td>
<td>$3.366$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$, $4.3, \text{V} &lt; V_IN &lt; 10, \text{V}$</td>
<td>$3.244$</td>
<td>$3.366$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ\text{C}$, $6.0, \text{V} &lt; V_IN &lt; 10, \text{V}$</td>
<td>$5.0$</td>
<td>$5.100$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$, $6.0, \text{V} &lt; V_IN &lt; 10, \text{V}$</td>
<td>$4.900$</td>
<td>$5.100$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
2. Minimum IN operating voltage is $2.7\, \text{V}$ or $V_O(\text{typ}) + 1\, \text{V}$, whichever is greater. Maximum IN voltage 10 V.
3. If $V_O \leq 1.8\, \text{V}$ then $V_{I_{\text{max}}} = 10\, \text{V}$, $V_{I_{\text{min}}} = 2.7\, \text{V}$:

$$\text{Line Regulation (mV)} = \left(\%/\text{V}\right) \times \frac{V_O(V_{I_{\text{max}}} - 2.7\, \text{V})}{100} \times 1000$$

If $V_O \geq 2.5\, \text{V}$ then $V_{I_{\text{max}}} = 10\, \text{V}$, $V_{I_{\text{min}}} = V_O + 1\, \text{V}$:

$$\text{Line Regulation (mV)} = \left(\%/\text{V}\right) \times \frac{V_O(V_{I_{\text{max}}} - (V_O + 1\, \text{V}))}{100} \times 1000$$
electrical characteristics over recommended operating free-air temperature range, \( V_I = V_O(\text{typ}) + 1 \text{ V}, \; I_O = 1 \text{ mA}, \; EN = 0 \text{ V}, \; C_o = 10 \mu \text{F} \) (unless otherwise noted) (continued)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum input voltage for valid RESET</td>
<td>( I_O(\text{RESET}) = 300 \mu \text{A} )</td>
<td>1.1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Trip threshold voltage</td>
<td>( V_O ) decreasing</td>
<td>92</td>
<td>98</td>
<td></td>
<td>%V_O</td>
</tr>
<tr>
<td>Hysteresis voltage</td>
<td>Measured at ( V_O )</td>
<td>0.5</td>
<td>0.15</td>
<td>0.4</td>
<td>%V_O</td>
</tr>
<tr>
<td>Output low voltage</td>
<td>( V_I = 2.7 \text{ V}, ; I_O(\text{RESET}) = 1 \text{ mA} )</td>
<td>100</td>
<td>200</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Leakage current</td>
<td>( V(\text{RESET}) = 5 \text{ V} )</td>
<td>1</td>
<td>200</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>RESET time-out delay</td>
<td>EN = 0 V</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>ms</td>
</tr>
</tbody>
</table>

**Input current (EN)**

<table>
<thead>
<tr>
<th>Dropout voltage (see Note 4)</th>
<th>TPS76728</th>
<th>TPS76730</th>
<th>TPS76733</th>
<th>TPS76750</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_O = 1 \text{ A}, ; T_J = 25^\circ C )</td>
<td>500</td>
<td>450</td>
<td>350</td>
<td>230</td>
</tr>
<tr>
<td>( I_O = 1 \text{ A}, ; T_J = -40^\circ C \text{ to } 125^\circ C )</td>
<td>825</td>
<td>675</td>
<td>575</td>
<td>380</td>
</tr>
</tbody>
</table>

**NOTE 4:** \( EN \) voltage equals \( V_O(\text{typ}) - 100 \text{ mV} \); TPS76701 output voltage set to 3.3 \text{ V} nominal with external resistor divider. TPS76715, TPS76718, TPS76725, and TPS76727 dropout voltage limited by input voltage range limitations (i.e., TPS76730 input voltage needs to drop to 2.9 \text{ V} for purpose of this test).

**TYPICAL CHARACTERISTICS**

**Table of Graphs**

<table>
<thead>
<tr>
<th>( V_O )</th>
<th>Output voltage vs Output current</th>
<th>2, 3, 4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Output voltage vs Free-air temperature</td>
<td>5, 6, 7</td>
</tr>
<tr>
<td></td>
<td>Ground current vs Free-air temperature</td>
<td>8, 9</td>
</tr>
<tr>
<td></td>
<td>Power-supply ripple rejection vs Frequency</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Output spectral noise density vs Frequency</td>
<td>11</td>
</tr>
<tr>
<td></td>
<td>Input voltage (min) vs Output voltage</td>
<td>12</td>
</tr>
<tr>
<td>( Z_o )</td>
<td>Output impedance vs Frequency</td>
<td>13</td>
</tr>
<tr>
<td>( V_D0 )</td>
<td>Dropout voltage vs Free-air temperature</td>
<td>14</td>
</tr>
<tr>
<td></td>
<td>Line transient response vs Time</td>
<td>15, 17</td>
</tr>
<tr>
<td></td>
<td>Load transient response</td>
<td>16, 18</td>
</tr>
<tr>
<td>( V_O )</td>
<td>Output voltage vs Input voltage</td>
<td>19</td>
</tr>
<tr>
<td></td>
<td>Dropout voltage vs Output voltage</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>Equivalent series resistance (ESR) vs Output voltage</td>
<td>22–25</td>
</tr>
</tbody>
</table>
TYPICAL CHARACTERISTICS

**TPS76733**

**OUTPUT VOLTAGE vs OUTPUT CURRENT**

![Graph of TPS76733](image)

- $V_I = 4.3$ V
- $T_A = 25$ °C

**Figure 2**

**TPS76715**

**OUTPUT VOLTAGE vs OUTPUT CURRENT**

![Graph of TPS76715](image)

- $V_I = 2.7$ V
- $T_A = 25$ °C

**Figure 3**

**TPS76725**

**OUTPUT VOLTAGE vs OUTPUT CURRENT**

![Graph of TPS76725](image)

- $V_I = 3.5$ V
- $T_A = 25$ °C

**Figure 4**

**TPS76733**

**OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

![Graph of TPS76733](image)

- $V_I = 4.3$ V
- $I_O = 1$ A
- $I_O = 1$ mA

**Figure 5**
TYPICAL CHARACTERISTICS

TPS76715
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 6

TPS76725
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 7

TPS76733
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

Figure 8
TYPICAL CHARACTERISTICS

TPS76715
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

Figure 9

TPS76733
POWER-SUPPLY RIPPLE REJECTION
vs
FREQUENCY

Figure 10

TPS76733
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

Figure 11
TYPICAL CHARACTERISTICS

INPUT VOLTAGE (MIN) vs OUTPUT VOLTAGE

Figure 12

TPS76733
OUTPUT IMPEDANCE vs FREQUENCY

Figure 13

TPS76733
DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

Figure 14
TYPICAL CHARACTERISTICS

TPS76715 - LINE TRANSIENT RESPONSE

TPS76715 - LOAD TRANSIENT RESPONSE

TPS76733 - LINE TRANSIENT RESPONSE

TPS76733 - LOAD TRANSIENT RESPONSE
TYPICAL CHARACTERISTICS

**Figure 19**

TPS76733

**OUTPUT VOLTAGE vs TIME (AT STARTUP)**

- $C_o = 10 \, \mu F$
- $I_O = 1 \, A$
- $T_A = 25^\circ C$

**Figure 20**

TPS76701

**DROPOUT VOLTAGE vs INPUT VOLTAGE**

- $I_O = 1 \, A$
- $T_A = 25^\circ C$
- $T_A = 125^\circ C$
- $T_A = -40^\circ C$

**Figure 21**

Test Circuit for Typical Regions of Stability (Figures 22 Through 25) (Fixed-Output Options)
TYPICAL CHARACTERISTICS

Figure 22

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†

\[ \text{ESR} - \text{Equivalent Series Resistance} - \Omega \]

\[ 0.1 \quad 0.01 \quad 0 \]

\[ 10 \quad 1 \quad 0 \]

\[ 200 \quad 400 \quad 600 \quad 800 \quad 1000 \]

\[ \text{Region of Instability} \]

\[ \text{Region of Stability} \]

\[ \text{VO} = 3.3 \text{ V} \]
\[ C_0 = 4.7 \mu\text{F} \]
\[ V_I = 4.3 \text{ V} \]
\[ T_A = 25^\circ \text{C} \]

Figure 23

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†

\[ \text{ESR} - \text{Equivalent Series Resistance} - \Omega \]

\[ 0.1 \quad 0.01 \quad 0 \]

\[ 10 \quad 1 \quad 0 \]

\[ 200 \quad 400 \quad 600 \quad 800 \quad 1000 \]

\[ \text{Region of Instability} \]

\[ \text{Region of Stability} \]

\[ \text{VO} = 3.3 \text{ V} \]
\[ C_0 = 4.7 \mu\text{F} \]
\[ V_I = 4.3 \text{ V} \]
\[ T_J = 125^\circ \text{C} \]

Figure 24

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†

\[ \text{ESR} - \text{Equivalent Series Resistance} - \Omega \]

\[ 0.1 \quad 0.01 \quad 0 \]

\[ 10 \quad 1 \quad 0 \]

\[ 200 \quad 400 \quad 600 \quad 800 \quad 1000 \]

\[ \text{Region of Instability} \]

\[ \text{Region of Stability} \]

\[ \text{VO} = 3.3 \text{ V} \]
\[ C_0 = 22 \mu\text{F} \]
\[ V_I = 4.3 \text{ V} \]
\[ T_A = 25^\circ \text{C} \]

Figure 25

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†

\[ \text{ESR} - \text{Equivalent Series Resistance} - \Omega \]

\[ 0.1 \quad 0.01 \quad 0 \]

\[ 10 \quad 1 \quad 0 \]

\[ 200 \quad 400 \quad 600 \quad 800 \quad 1000 \]

\[ \text{Region of Instability} \]

\[ \text{Region of Stability} \]

\[ \text{VO} = 3.3 \text{ V} \]
\[ C_0 = 22 \mu\text{F} \]
\[ V_I = 4.3 \text{ V} \]
\[ T_J = 125^\circ \text{C} \]

†Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to \( C_0 \).
APPLICATION INFORMATION

The TPS767xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3 V, 3.3 V, and 5 V), and an adjustable regulator, the TPS76701 (adjustable from 1.5 V to 5.5 V).

device operation

The TPS767xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS767xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in $\beta$ forces an increase in $I_B$ to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS767xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS767xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 $\mu$A. If the shutdown feature is not used, EN should be tied to ground.

minimum load requirements

The TPS767xx family is stable even at zero load; no minimum load is required for operation.

FB—pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as shown in Figure 27. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 $\mu$F or larger) improves load transient response and noise rejection if the TPS767xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS767xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 $\mu$F and the equivalent series resistance (ESR) must be between 50 m$\Omega$ and 1.5 $\Omega$. Capacitor values 10 $\mu$F or larger are acceptable, provided the ESR is less than 1.5 $\Omega$. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 10-$\mu$F surface-mount ceramic capacitors, including devices from Sprague and Kemet, meet the ESR requirements stated above.
APPLICATION INFORMATION

external capacitor requirements (continued)

programming the TPS76701 adjustable LDO regulator

The output voltage of the TPS76701 adjustable regulator is programmed using an external resistor divider as shown in Figure 27. The output voltage is calculated using:

\[ V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \]  

(1)

Where:

\[ V_{ref} = 1.1834 \text{ V typ} \] (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose \( R2 = 30.1 \text{ kΩ} \) to set the divider current at 50 μA and then calculate R1 using:

\[ R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \]  

(2)

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<td>2.5 V</td>
<td>33.2</td>
</tr>
<tr>
<td>3.3 V</td>
<td>53.6</td>
</tr>
<tr>
<td>3.6 V</td>
<td>61.9</td>
</tr>
<tr>
<td>4.75 V</td>
<td>90.8</td>
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Figure 27. TPS76701 Adjustable LDO Regulator Programming
reset indicator

The TPS767xx features a RESET output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the RESET output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. RESET can be used to drive power-on reset circuitry or as a low-battery indicator. RESET does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to timing diagram for start-up sequence).

regulator protection

The TPS767xx PMOS pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS767xx also features internal current limiting and thermal protection. During normal operation, the TPS767xx limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C (typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, \( P_{D(\text{max})} \), and the actual dissipation, \( P_D \), which must be less than or equal to \( P_{D(\text{max})} \).

The maximum power dissipation limit is determined using the following equation:

\[
P_{D(\text{max})} = \frac{T_{J_{\text{max}}} - T_A}{R_{\theta JA}}
\]

Where:

- \( T_{J_{\text{max}}} \) is the maximum allowable junction temperature.
- \( R_{\theta JA} \) is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 32.6°C/W for the 20-terminal PWP with no airflow.
- \( T_A \) is the ambient temperature.

The regulator dissipation is calculated using:

\[
P_D = (V_I - V_O) \times I_O
\]

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.
## PACKAGING INFORMATION

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</tbody>
</table>

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TPS76701-Q1, TPS76715-Q1, TPS76718-Q1, TPS76725-Q1, TPS76733-Q1, TPS76750-Q1:

- Catalog: TPS76701, TPS76715, TPS76718, TPS76725, TPS76733, TPS76750


NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com.<http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-153

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THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

![Exposed Thermal Pad Dimensions Diagram]

Exposed Thermal Pad Dimensions

NOTE: A. All linear dimensions are in millimeters

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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