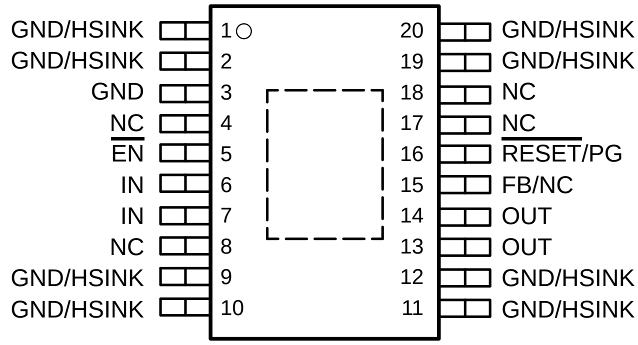
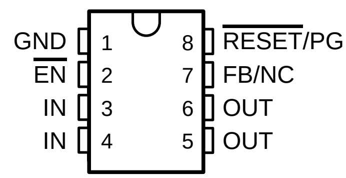
- **Open Drain Power-On Reset With 200-ms Delay (TPS775xx)**
- **Open Drain Power Good (TPS776xx)**
- **500-mA Low-Dropout Voltage Regulator**
- **Available in 1.5-V, 1.6-V (TPS77516 Only), 1.8-V, 2.5-V, 2.8-V (TPS77628 Only), 3.3-V Fixed Output and Adjustable Versions**
- **Dropout Voltage to 169 mV (Typ) at 500 mA (TPS77x33)**
- **Ultralow 85 μA Typical Quiescent Current**
- **Fast Transient Response**
- **2% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **8-Pin SOIC and 20-Pin TSSOP PowerPAD™ (PWP) Package**
- **Thermal Shutdown Protection**

PWP PACKAGE
(TOP VIEW)



NC – No internal connection

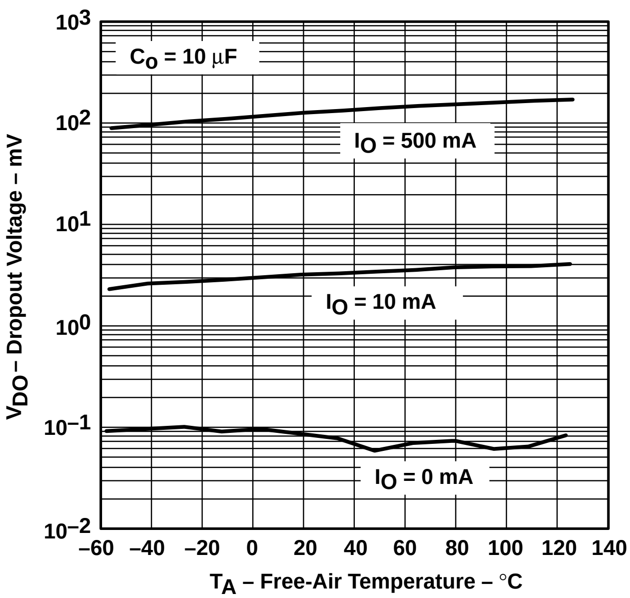
D PACKAGE
(TOP VIEW)



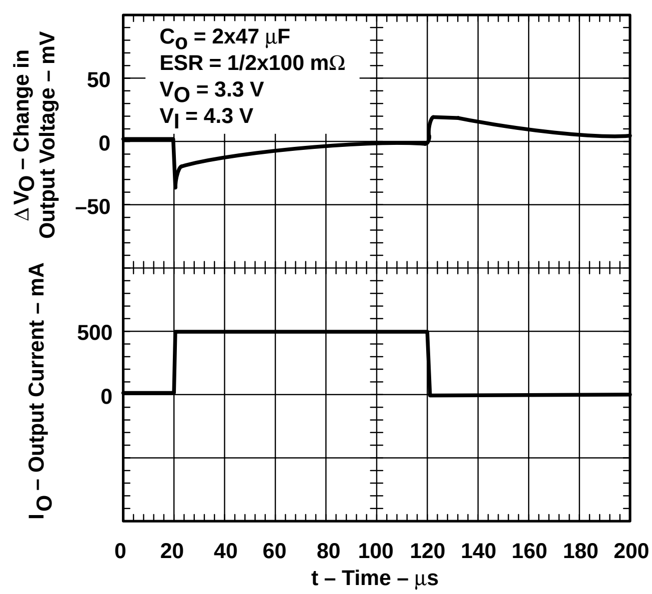
description

The TPS775xx and TPS776xx devices are designed to have a fast transient response and be stable with a 10-μF low ESR capacitors. This combination provides high performance at a reasonable cost.

TPS77x33
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE



TPS77x33
LOAD TRANSIENT RESPONSE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 169 mV at an output current of 500 mA for the TPS77x33) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μA over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to EN (enable) shuts down the regulator, reducing the quiescent current to 1 μA at T_J = 25°C.

The RESET output of the TPS775xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS775xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

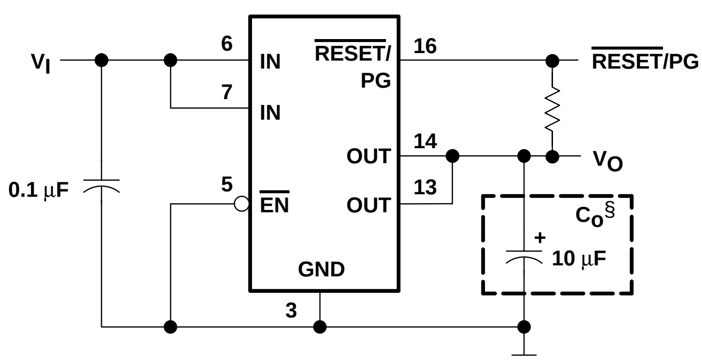
Power good (PG) of the TPS776xx is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS775xx and TPS776xx are offered in 1.5-V, 1.6-V (TPS77516 only), 1.8-V, 2.5-V, 2.8 V (TPS77628 only), and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V for TPS77501 option and 1.2 V to 5.5 V for TPS77601 option). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS775xx and TPS776xx families are available in 8 pin SOIC and 20 pin TSSOP packages.

AVAILABLE OPTIONS†

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES			
	TYP	TSSOP (PWP)		SOIC (D)	
–40°C to 125°C	3.3	TPS77533PWP	TPS77633PWP	TPS77533D	TPS77633D
	2.5	TPS77525PWP	TPS77625PWP	TPS77525D	TPS77625D
	2.8	—	TPS77628PWP	—	TPS77628D
	1.8	TPS77518PWP	TPS77618PWP	TPS77518D	TPS77618D
	1.6	TPS77516PWP	—	TPS77516D	—
	1.5	TPS77515PWP	TPS77615PWP	TPS77515D	TPS77615D
	Adjustable‡ 1.2 V to 5.5 V	—	TPS77601PWP	—	TPS77601D
	Adjustable‡ 1.5 V to 5.5 V	TPS77501PWP	—	TPS77501D	—

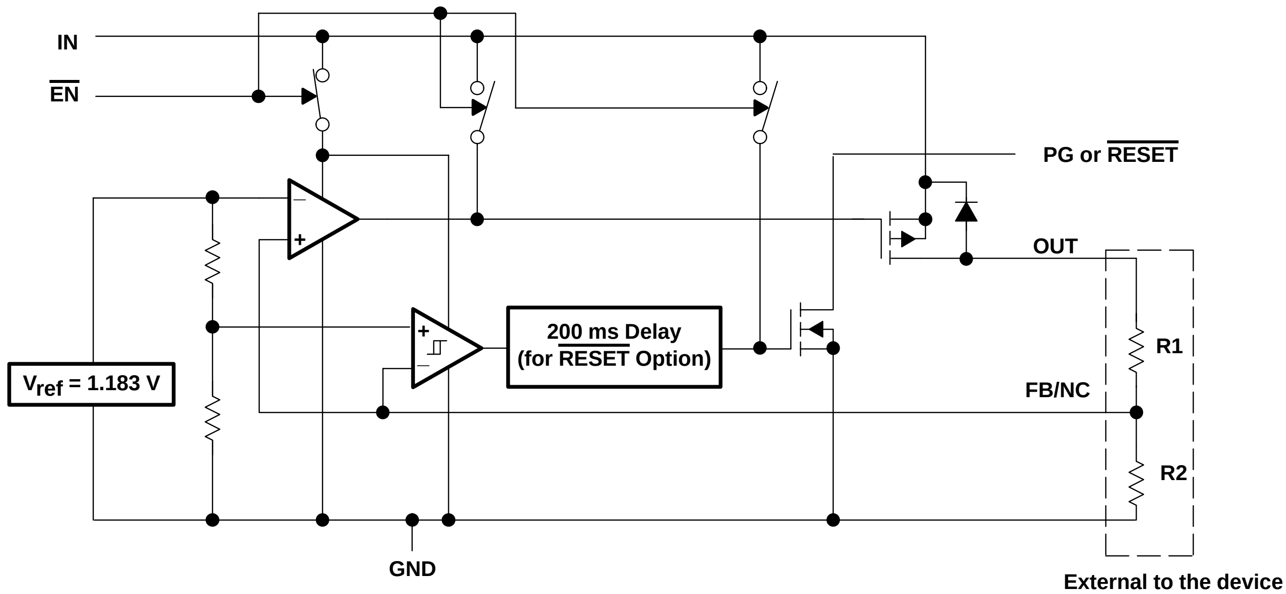
† The TPS775xx has an open-drain power-on reset with a 200-ms delay function. The TPS776xx has an open-drain power good function.
‡ The TPS77x01 is programmable using an external resistor divider (see application information). The D and PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., TPS77501DR).



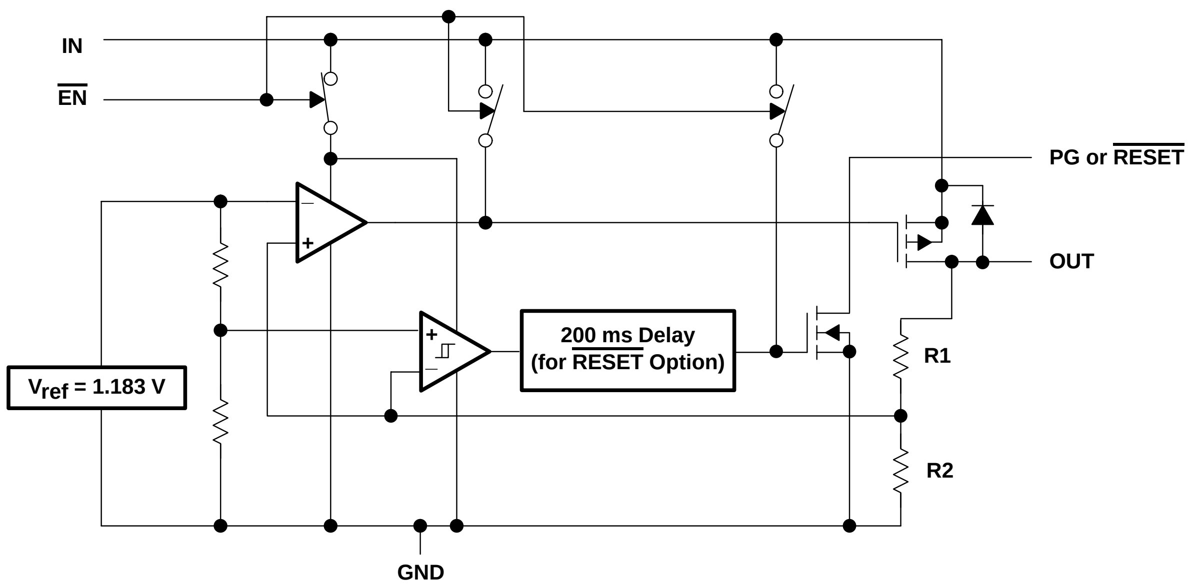
§ See application information section for capacitor selection details.

Figure 1. Typical Application Configuration for Fixed Output Options

functional block diagram—adjustable version



functional block diagram—fixed-voltage version



Terminal Functions

SOIC Package (TPS775xx)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
$\overline{\text{RESET}}$	8	O	$\overline{\text{RESET}}$ output

TSSOP Package (TPS775xx)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input voltage
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
$\overline{\text{RESET}}$	16	O	$\overline{\text{RESET}}$ output

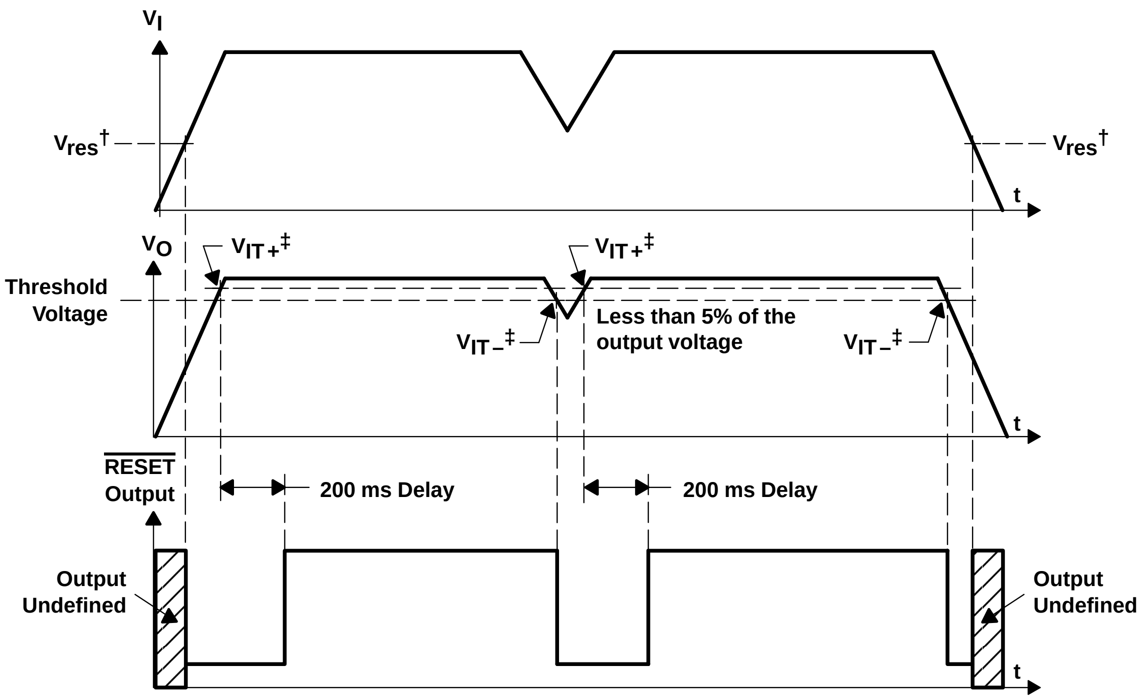
SOIC Package (TPS776xx)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
PG	8	O	PG output

TSSOP Package (TPS776xx)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input voltage
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
PG	16	O	PG output

TPS775xx RESET timing diagram



† V_{res} is the minimum input voltage for a valid RESET. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ V_{IT} –Trip voltage is typically 5% lower than the output voltage (95%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I . . . –0.3 V to 13.5 V
Voltage range at $\overline{\text{EN}}$ . . . –0.3 V to 16.5 V
Maximum $\overline{\text{RESET}}$ voltage (TPS775xx) . . . 16.5 V
Maximum PG voltage (TPS776xx) . . . 16.5 V
Peak output current . . . Internally limited
Output voltage, V_O (OUT, FB) . . . 7 V
Continuous total power dissipation . . . See dissipation rating tables
Operating virtual junction temperature range, T_J . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . –65°C to 150°C
ESD rating, HBM . . . 2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

DISSIPATION RATING TABLE 2 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PWP§	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP¶	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

§ This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in^2).
¶ This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2). For more information, refer to TI technical brief SLMA002.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I#		2.7	10	V
Output voltage range, V_O	TPS77501	1.5	5.5	V
	TPS77601	1.2	5.5	
Operating virtual junction temperature, T_J (see Note 1)		–40	125	°C

To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

electrical characteristics over recommended operating temperature range (TJ = –40°C to 125°C), $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$ V, $C_o = 10\ \mu F$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 µA to 500 mA load) (see Note 2)	TPS77501	$1.5\ V \le V_O \le 5.5\ V$, $T_J = 25°C$		V_O		V
	TPS77501	$1.5\ V \le V_O \le 5.5\ V$,	$0.98V_O$		$1.02V_O$	V
	TPS77601	$1.2\ V \le V_O \le 5.5\ V$, $T_J = 25°C$		V_O		V
	TPS77601	$1.2\ V \le V_O \le 5.5\ V$,	$0.98V_O$		$1.02V_O$	V
	TPS77x15	$T_J = 25°C$, $2.7\ V < V_{IN} < 10\ V$		1.5		V
	TPS77x15	$T_J = –40°C$ to 125°C, $2.7\ V < V_{IN} < 10\ V$	1.470		1.530	V
	TPS77516	$T_J = 25°C$, $2.7\ V < V_{IN} < 10\ V$		1.6		V
	TPS77516	$T_J = –40°C$ to 125°C, $2.7\ V < V_{IN} < 10\ V$	1.568		1.632	V
	TPS77x18	$T_J = 25°C$, $2.8\ V < V_{IN} < 10\ V$		1.8		V
	TPS77x18	$T_J = –40°C$ to 125°C, $2.8\ V < V_{IN} < 10\ V$	1.764		1.836	V
	TPS77x25	$T_J = 25°C$, $3.5\ V < V_{IN} < 10\ V$		2.5		V
	TPS77x25	$T_J = –40°C$ to 125°C, $3.5\ V < V_{IN} < 10\ V$	2.450		2.550	V
	TPS77628	$T_J = 25°C$, $3.8\ V < V_{IN} < 10\ V$		2.8		V
	TPS77628	$T_J = –40°C$ to 125°C, $3.8\ V < V_{IN} < 10\ V$	2.744		2.856	V
	TPS77x33	$T_J = 25°C$, $4.3\ V < V_{IN} < 10\ V$		3.3		V
	TPS77x33	$T_J = –40°C$ to 125°C, $4.3\ V < V_{IN} < 10\ V$	3.234		3.366	V
Quiescent current (GND current) $\overline{EN}$ = 0V, (see Note 2)		$10\ \mu A < I_O < 500$ mA, $T_J = 25°C$		85		µA
		$I_O = 500$ mA, $T_J = –40°C$ to 125°C			125	µA
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 2 and 3)		$V_O + 1\ V < V_I \le 10\ V$, $T_J = 25°C$		0.01		%/V
Load regulation				3		mV
Output noise voltage (TPS77x18)		BW = 200 Hz to 100 kHz, $I_C = 500$ mA $C_O = 10\ \mu F$, $T_J = 25°C$		53		µVrms
Output current limit		$V_O = 0$ V	1.2	1.6	1.9	A
Thermal shutdown junction temperature				150		°C
Standby current		$\overline{EN} = V_I$, $T_J = 25°C$, $2.7\ V < V_I < 10\ V$		1		µA
		$\overline{EN} = V_I$, $2.7\ V < V_I < 10\ V$			10	µA
FB input current	TPS77x01	FB = 1.5 V		2		nA
High level enable input voltage			1.7			V
Low level enable input voltage					0.9	V
Power supply ripple rejection (see Note 2)		f = 1 KHz, $C_o = 10\ \mu F$, $T_J = 25°C$		60		dB

NOTES: 1. Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum IN voltage 10V.
2. If $V_O \le 1.8$ V then $V_{Imin} = 2.7$ V, $V_{Imax} = 10$ V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - 2.7\ V\right)}{100} \times 1000$$

If $V_O \ge 2.5$ V then $V_{Imin} = V_O + 1$ V, $V_{Imax} = 10$ V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - \left(V_O + 1\ V\right)\right)}{100} \times 1000$$

electrical characteristics over recommended operating temperature range (TJ = –40°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0 V, C_o = 10 µF (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
Reset (TPS775xx)	Minimum input voltage for valid $\overline{\text{RESET}}$		$I_{O(RESET)}$ = 300µA			1.1		V
	Trip threshold voltage		V_O decreasing		92		98	%V_O
	Hysteresis voltage		Measured at V_O			0.5		%V_O
	Output low voltage		V_I = 2.7 V,	$I_{O(RESET)}$ = 1mA		0.15	0.4	V
	Leakage current		$V_{(RESET)}$ = 5 V				1	µA
	RESET time-out delay					200		ms
PG (TPS776xx)	Minimum input voltage for valid PG		$I_{O(PG)}$ = 300 µA			1.1		V
	Trip threshold voltage		V_O decreasing		92		98	%V_O
	Hysteresis voltage		Measured at V_O			0.5		%V_O
	Output low voltage		V_I = 2.7 V,	$I_{O(PG)}$ = 1 mA		0.15	0.4	V
	Leakage current		$V_{(PG)}$ = 5 V				1	µA
Input current ($\overline{EN}$)			$\overline{EN}$ = 0 V		–1	0	1	µA
			$\overline{EN}$ = V_I		–1		1	
Dropout voltage (see Note 4)		TPS77628	I_O = 500 mA,	T_J = 25°C		285		mV
			I_O = 500 mA,				410	
		TPS77533	I_O = 500 mA,	T_J = 25°C		169		
			I_O = 500 mA,				287	
		TPS77633	I_O = 500 mA,	T_J = 25°C		169		
			I_O = 500 mA,				287	

NOTE 3: IN voltage equals V_O(typ) – 100 mV; TPS77x15, TPS77516, TPS77x18, and TPS77x25 dropout voltage limited by input voltage range limitations (i.e., TPS77x33 input voltage needs to drop to 3.2 V for purpose of this test).

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3, 4
		vs Free-air temperature	5, 6, 7
	Ground current	vs Free-air temperature	8
	Power supply ripple rejection	vs Frequency	9
	Output spectral noise density	vs Frequency	10
Z_o	Output impedance	vs Frequency	11
V_{DO}	Dropout voltage	vs Input voltage	12
		vs Free-air temperature	13
	Input voltage (min)	vs Output voltage	14
	Line transient response		15, 17
	Load transient response		16, 18
V_O	Output voltage	vs Time	19
	Equivalent series resistance (ESR)	vs Output current	21 – 24

TYPICAL CHARACTERISTICS

TPS77x33
OUTPUT VOLTAGE vs OUTPUT CURRENT

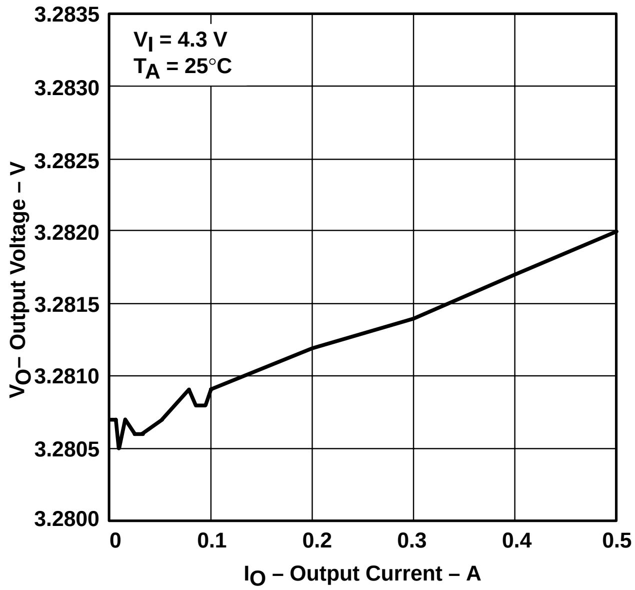


Figure 2

TPS77x15
OUTPUT VOLTAGE vs OUTPUT CURRENT

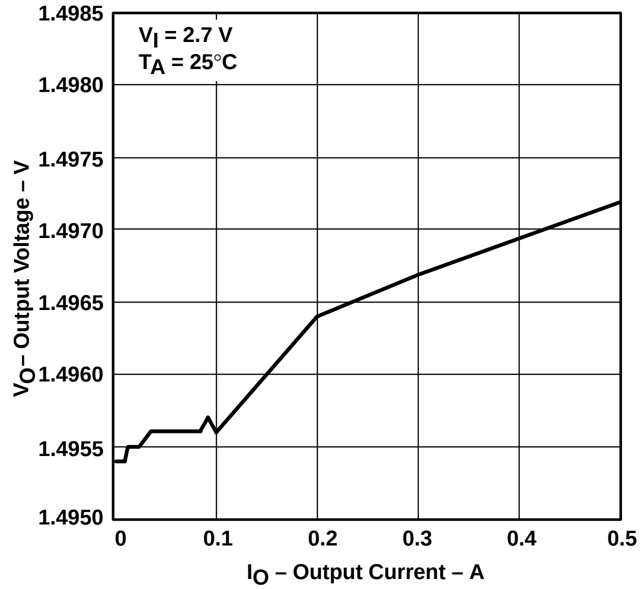


Figure 3

TPS77x25
OUTPUT VOLTAGE vs OUTPUT CURRENT

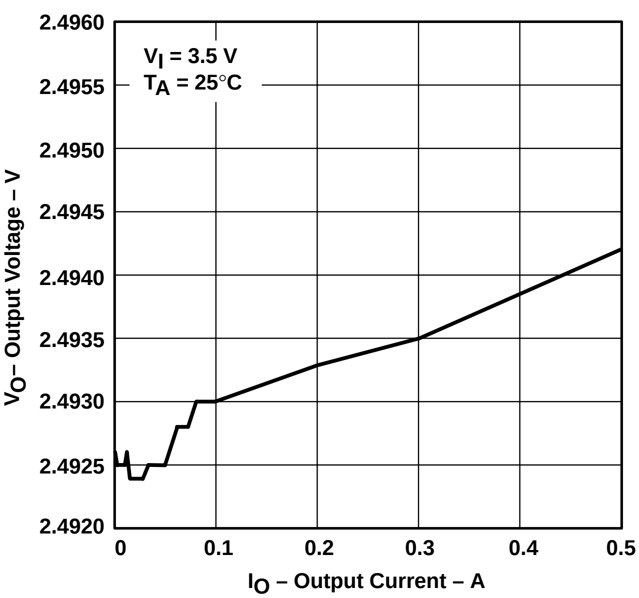


Figure 4

TPS77x33
OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

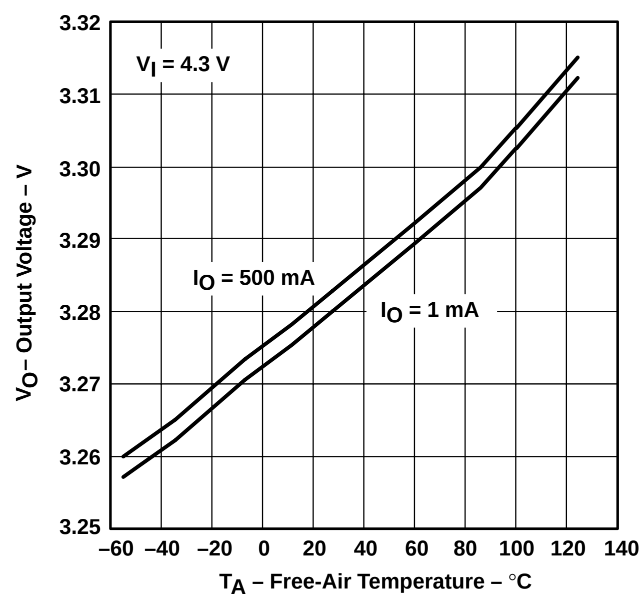


Figure 5

TYPICAL CHARACTERISTICS

TPS77x15
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

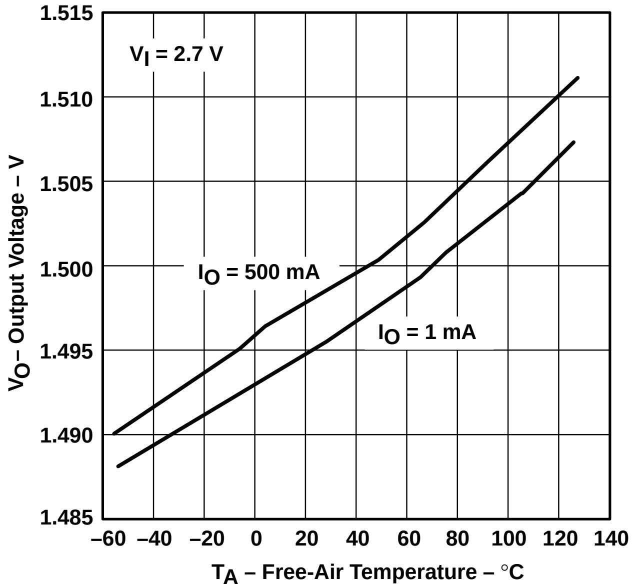


Figure 6

TPS77x25
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

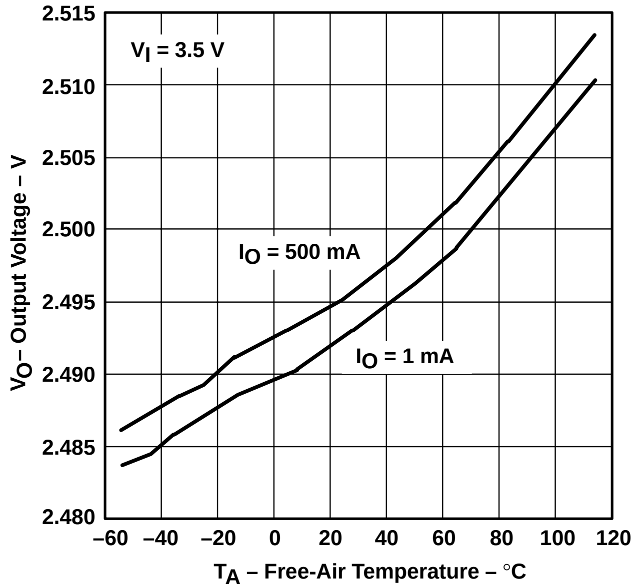


Figure 7

TPS77xxx
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

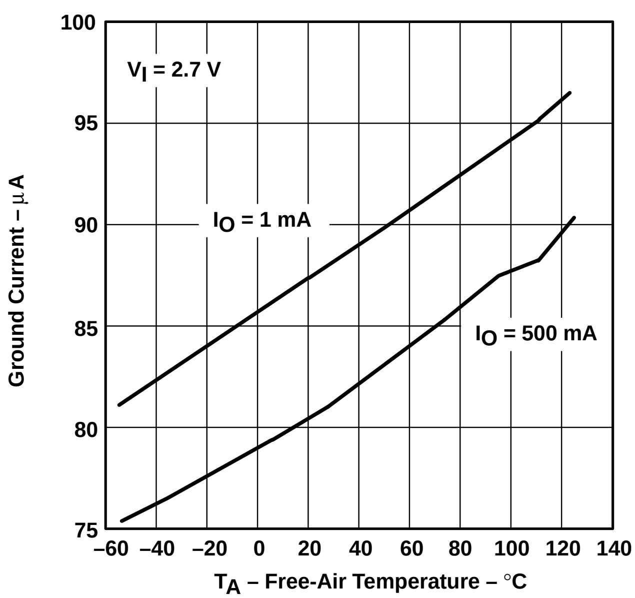


Figure 8

TPS77x33
POWER SUPPLY RIPPLE REJECTION
vs
FREQUENCY

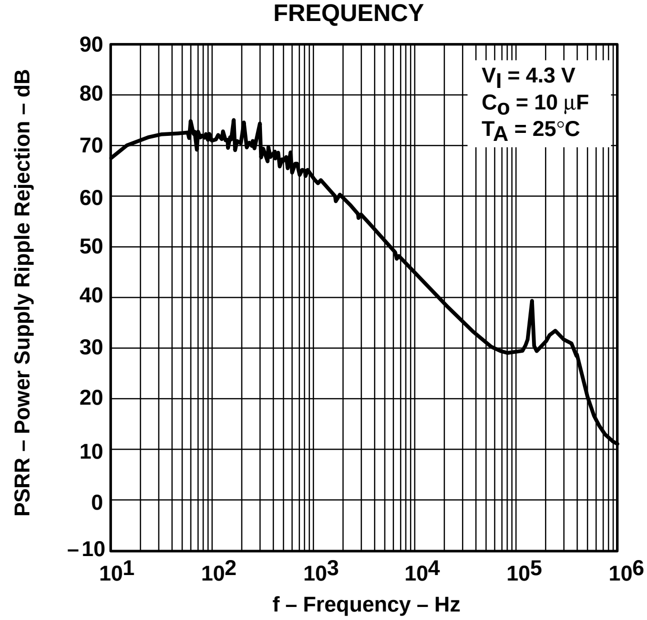


Figure 9

TYPICAL CHARACTERISTICS

TPS77x33
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

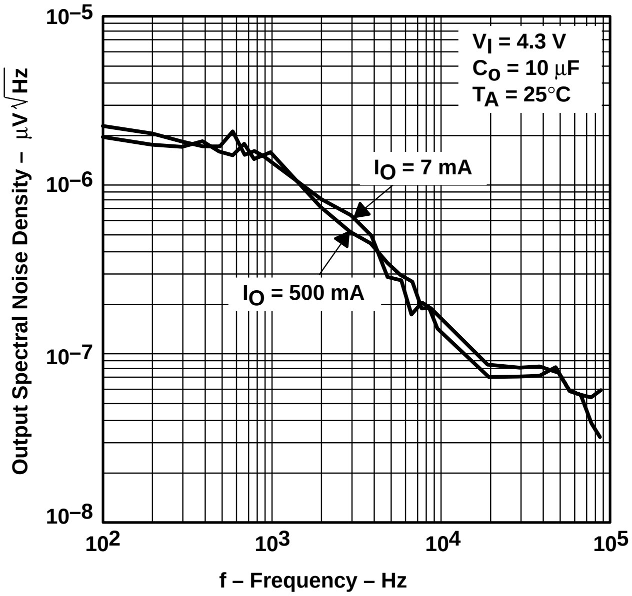


Figure 10

TPS77x33
OUTPUT IMPEDANCE
vs
FREQUENCY

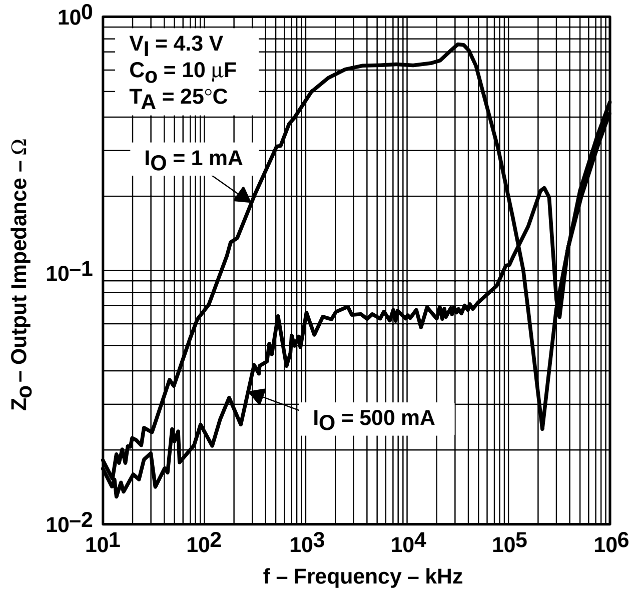


Figure 11

TPS77x01
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

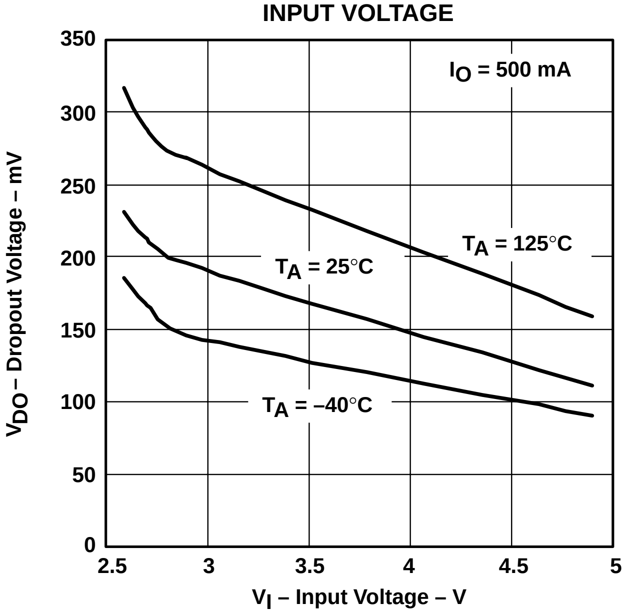


Figure 12

TPS77x33
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

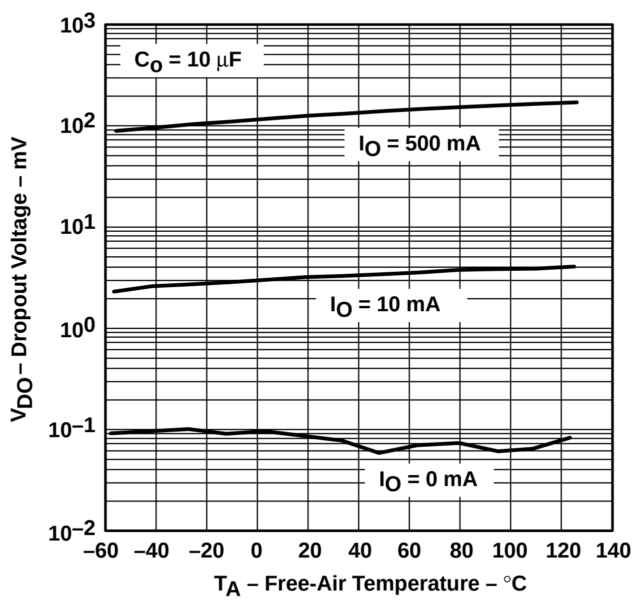


Figure 13

TYPICAL CHARACTERISTICS

INPUT VOLTAGE (MIN) vs OUTPUT VOLTAGE

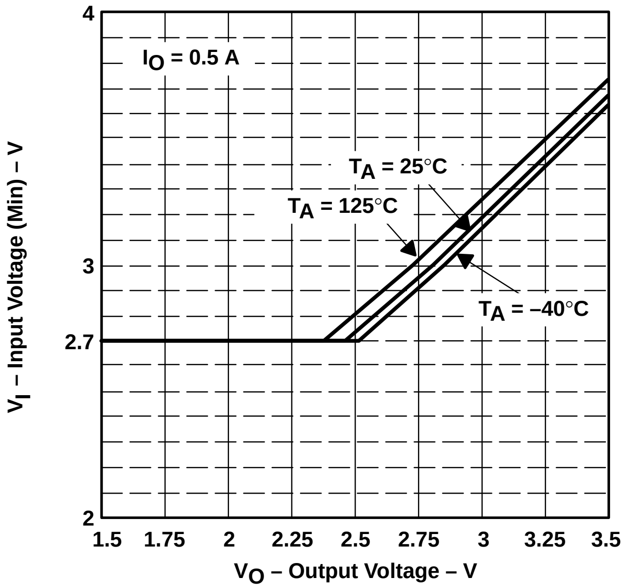


Figure 14

TPS77x15 LINE TRANSIENT RESPONSE

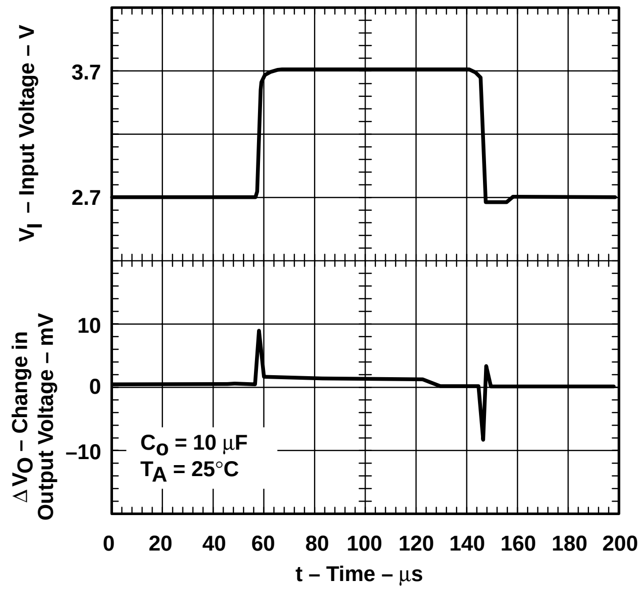


Figure 15

TPS77x15 LOAD TRANSIENT RESPONSE

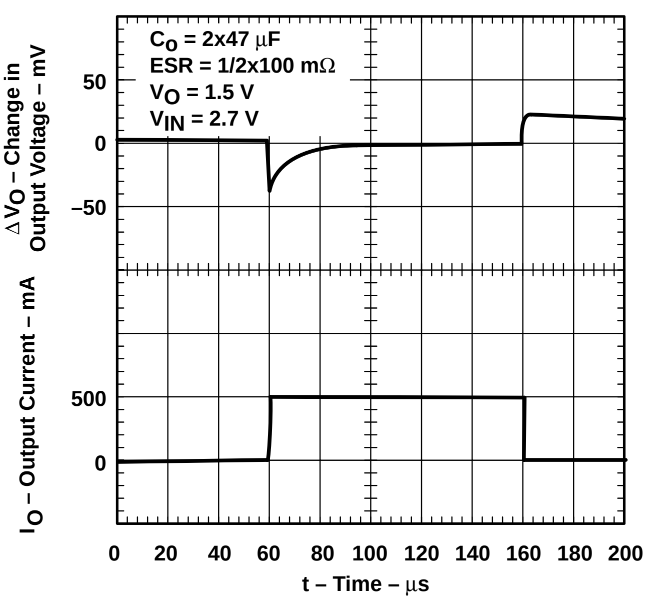


Figure 16

TPS77x33 LINE TRANSIENT RESPONSE

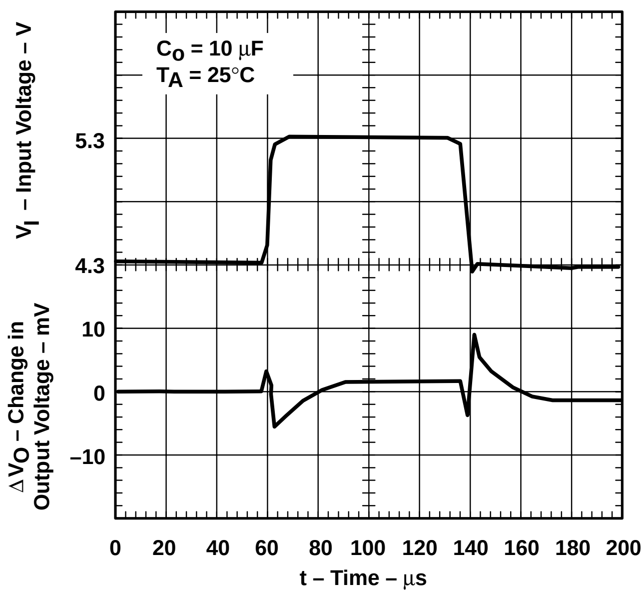


Figure 17

TYPICAL CHARACTERISTICS

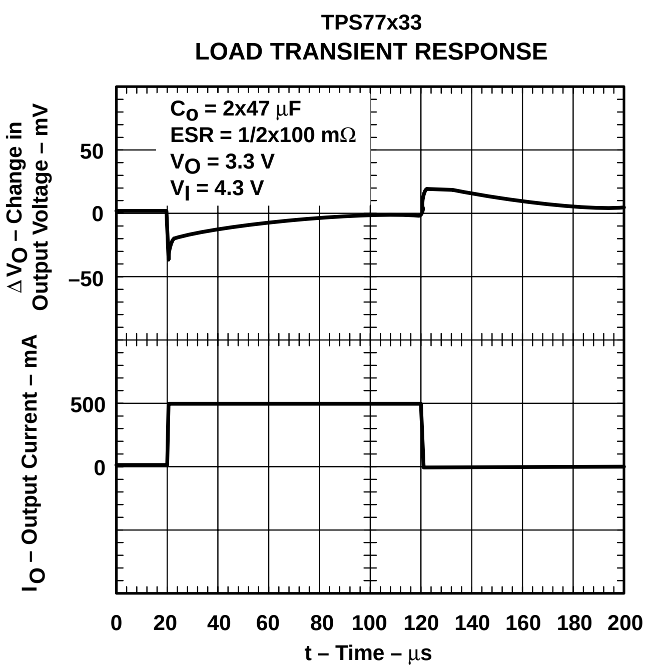


Figure 18

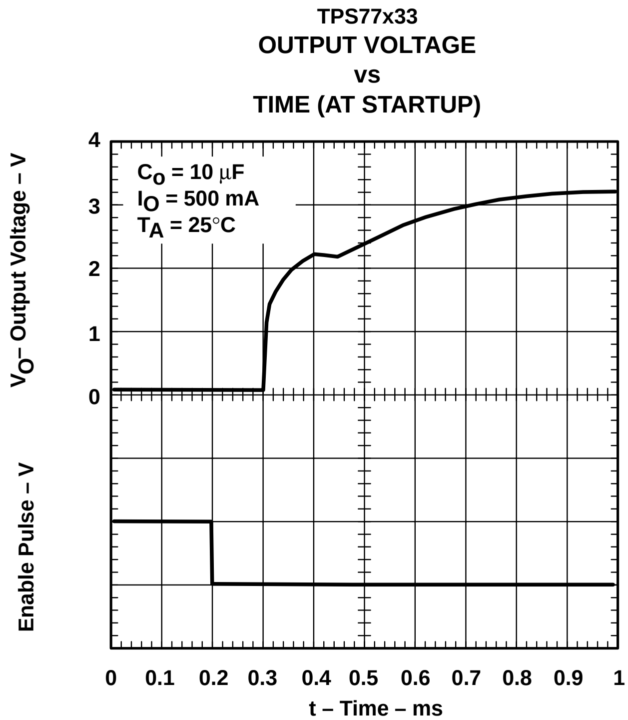


Figure 19

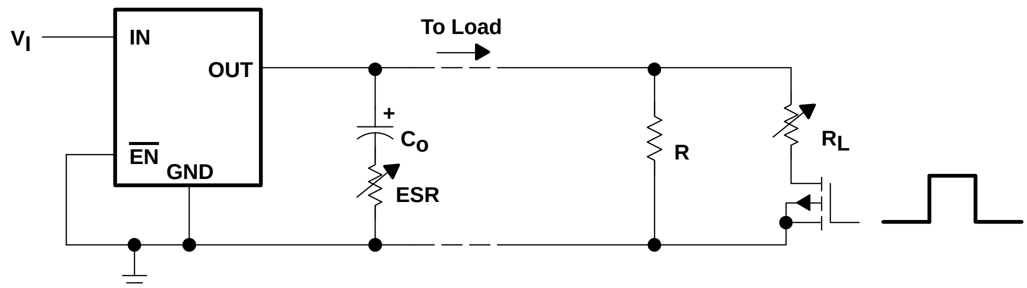


Figure 20. Test Circuit for Typical Regions of Stability (Figures 21 through 24) (Fixed Output Options)

TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

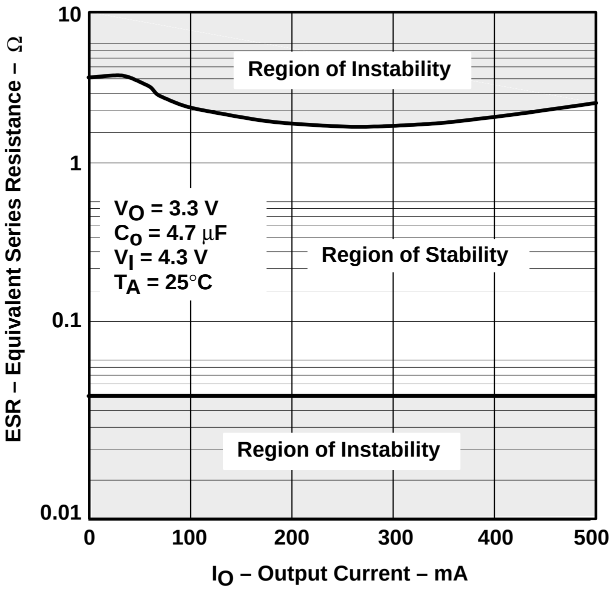


Figure 21

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

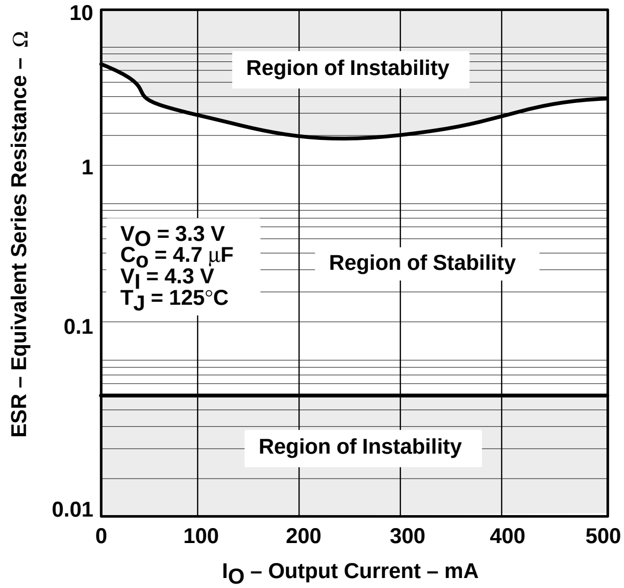


Figure 22

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

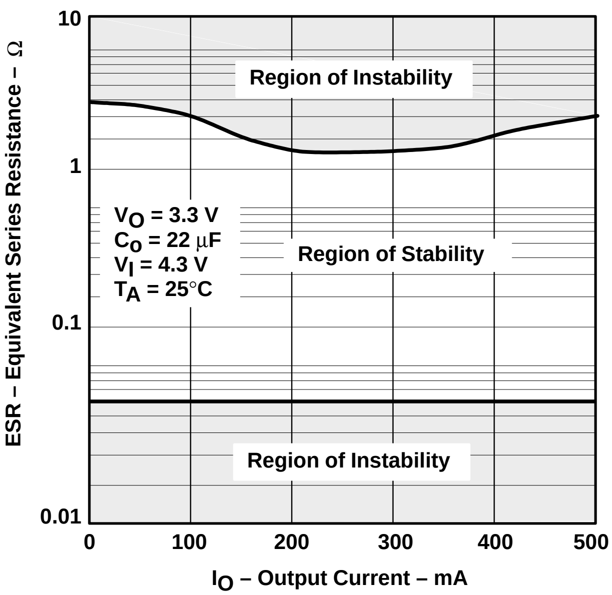


Figure 23

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

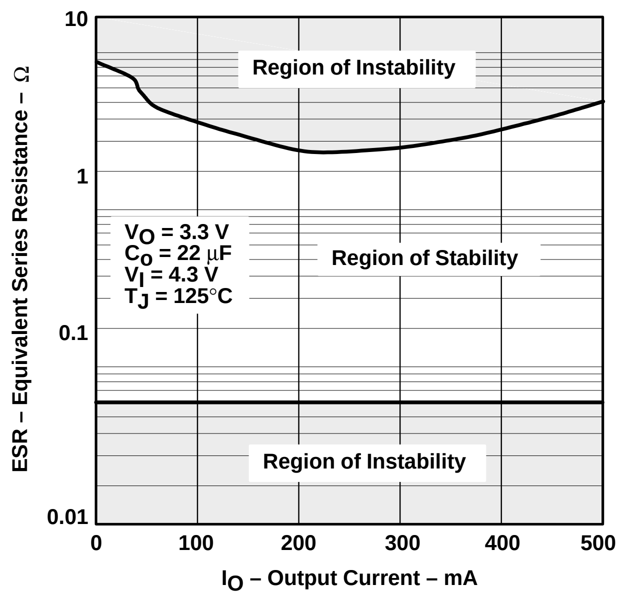


Figure 24

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

APPLICATION INFORMATION

The TPS775xx family includes five fixed-output voltage regulators (1.5 V, 1.6 V, 1.8 V, 2.5 V, and 3.3 V), and an adjustable regulator, the TPS77501 (adjustable from 1.5 V to 5.5 V).

The TPS776xx family includes five fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.8 V, and 3.3 V), and an adjustable regulator, the TPS77601 (adjustable from 1.2 V to 5.5 V).

device operation

The TPS775xx and TPS776xx feature very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS775xx and TPS776xx use a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS775xx and TPS776xx quiescent currents remain low even when the regulator drops out, eliminating both problems.

The TPS775xx and TPS776xx families also feature a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 µA. If the shutdown feature is not used, $\overline{\text{EN}}$ should be tied to ground.

minimum load requirements

The TPS775xx and TPS776xx families are stable even at zero load; no minimum load is required for operation.

FB—pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option . The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 26. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 µF or larger) improves load transient response and noise rejection if the TPS775xx or TPS776xx are located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS775xx and TPS776xx require an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 µF and the ESR (equivalent series resistance) must be between 50 mΩ and 1.5 Ω. Capacitor values 10 µF or larger are acceptable, provided the ESR is less than 1.5 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

APPLICATION INFORMATION

external capacitor requirements (continued)

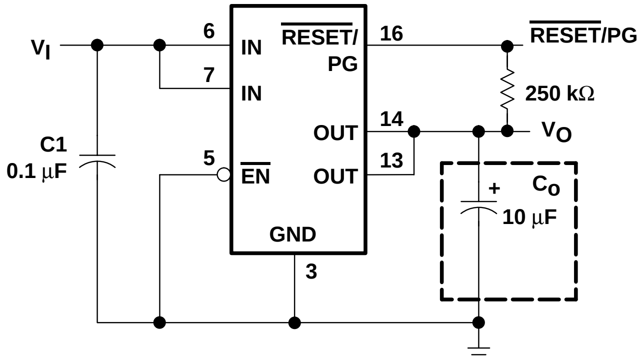


Figure 25. Typical Application Circuit (Fixed Versions)

programming the TPS77x01 adjustable LDO regulator

The output voltage of the TPS77x01 adjustable regulator is programmed using an external resistor divider as shown in Figure 26. The output voltage is calculated using:

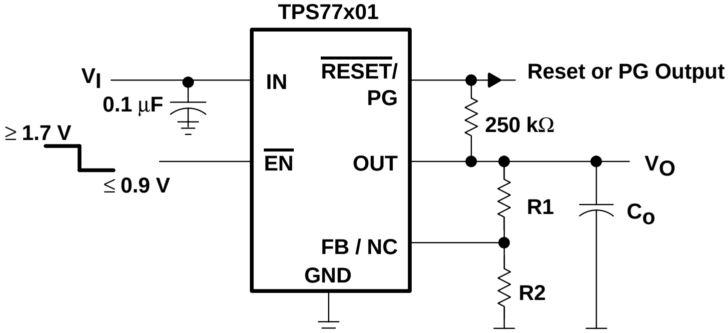
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where:

V_{ref} = 1.1834 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 10-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 110 kΩ to set the divider current at approximately 10 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	121	110	kΩ
3.3 V	196	110	kΩ
3.6 V	226	110	kΩ
4.75 V	332	110	kΩ

Figure 26. TPS77x01 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

reset indicator

The TPS775xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator. $\overline{\text{RESET}}$ does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to timing diagram for start-up sequence).

power-good indicator

The TPS776xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

regulator protection

The TPS775xx and TPS776xx PMOS-pass transistors have a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS775xx and TPS776xx also feature internal current limiting and thermal protection. During normal operation, the TPS775xx and TPS776xx limit output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, and is calculated as

$$\frac{1}{\text{derating factor}}$$ from the dissipation rating tables.

T_A is the ambient temperature.

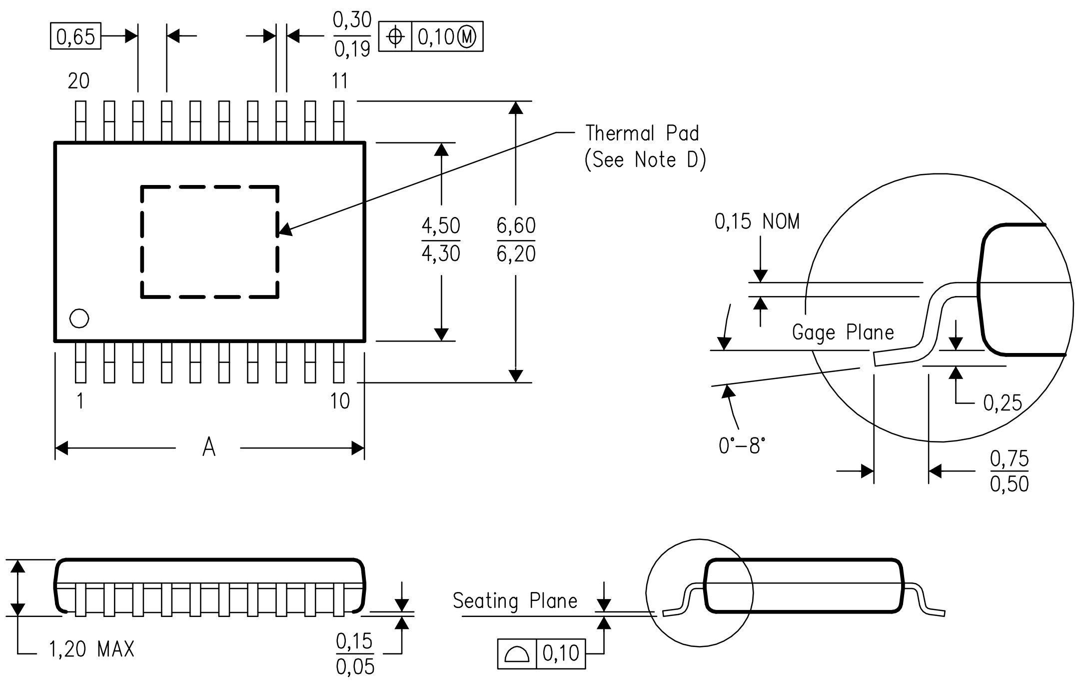
The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

PWP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

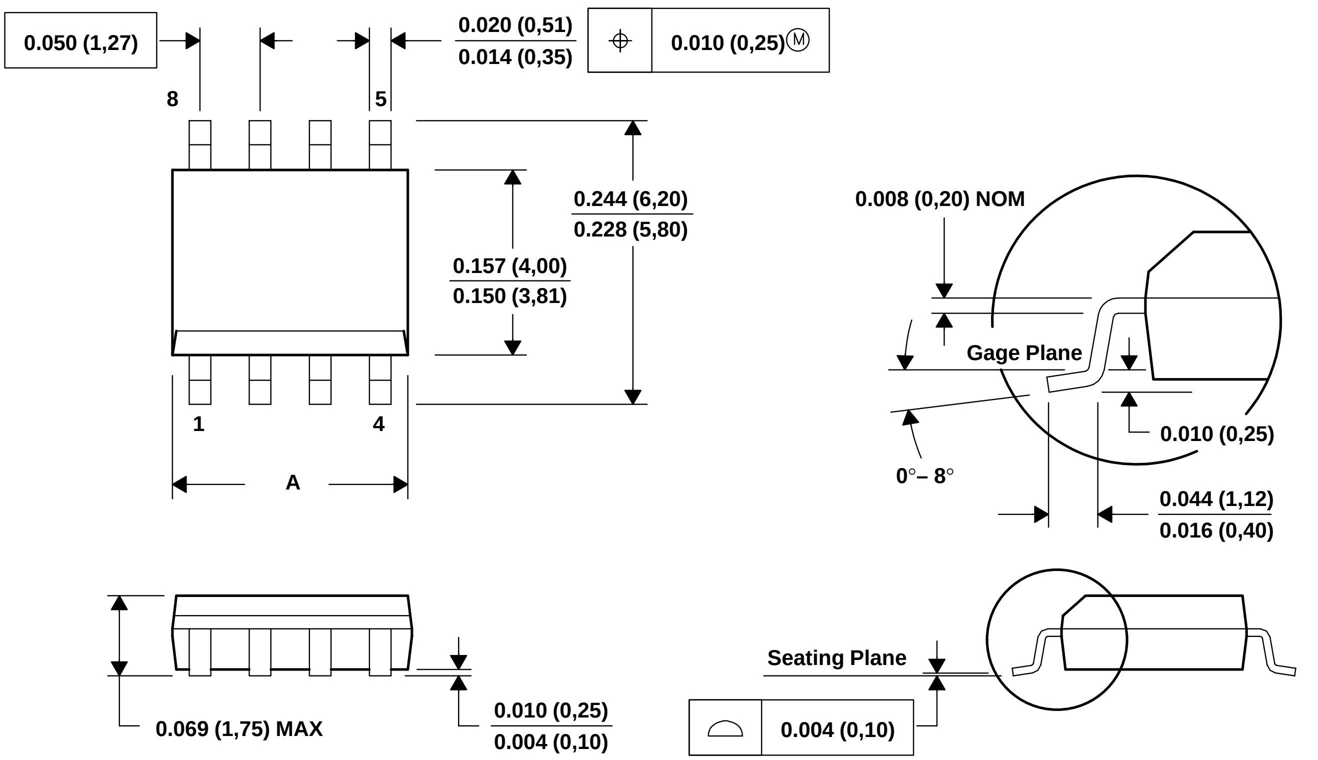
4073225/G 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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