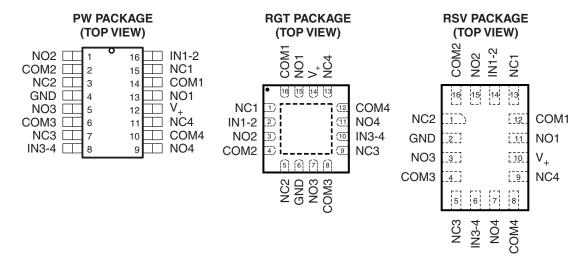
# 0.45-Ω QUAD SPDT ANALOG SWITCH QUAD-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER WITH TWO CONTROLS

#### **FEATURES**

- Specified Break-Before-Make Switching
- Low ON-State Resistance (<0.5 Ω)
- Control Inputs Are 1.8-V Logic Compatible
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 4.3-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

#### **APPLICATIONS**

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals



## **DESCRIPTION/ORDERING INFORMATION**

The TS3A44159 is a quad single-pole double-throw (SPDT) analog switch with two control inputs, which is designed to operate from 1.65 V to 4.3 V. This device is also known as a dual double-pole double-throw (DPDT) configuration. It offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### **ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	RGT – QFN	Tape and reel	TS3A44159RGTR	ZWH
-40°C to 85°C	RSV – QFN	Tape and reel	TS3A44159RSVR	ZWH
	PW - TSSOP	Tape and reel	TS3A44159PWR	YC4159

## SUMMARY OF CHARACTERISTICS(1)

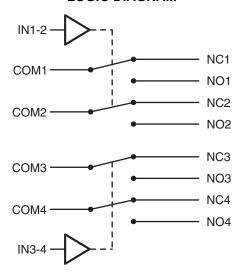
Configuration	Quad 2:1 Multiplexer/Demultiplexer (4 x SPDT or 2 x DPDT)
Number of channels	4
ON-state resistance (r <sub>on</sub> )	0.45 Ω (max)
ON-state resistance match (Δr <sub>on</sub> )	0.07 Ω (max)
ON-state resistance flatness (r <sub>ON(flat)</sub> )	0.1 Ω (max)
Turn-on/turn-off time (t <sub>ON</sub> /t <sub>OFF</sub> )	23 ns/32 ns
Break-before-make time (t <sub>BBM</sub> )	30 ns
Charge injection (Q <sub>C</sub> )	139 pC
Bandwidth (BW)	35 MHz
OFF isolation (O <sub>ISO</sub> )	-71 dB
Crosstalk (X <sub>TALK</sub> )	-73 dB
Total harmonic distortion (THD)	0.003%
Power-supply current (I <sub>+</sub> )	0.4 μΑ
Package option	16-pin QFN

(1) 
$$V_+ = 4.3 \text{ V}, T_A = 25^{\circ}\text{C}$$

## **FUNCTION TABLE**

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
Н	OFF	ON

## **LOGIC DIAGRAM**



Package drawings, thermal data, and symbolization are available at <a href="www.ti.com/packaging">www.ti.com/packaging</a>.
For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>+</sub>	Supply voltage range (3)		-0.5	4.6	V
$V_{NC}$ $V_{NO}$ $V_{COM}$	Analog voltage range <sup>(3)(4)(5)</sup>		-0.5	V <sub>+</sub> + 0.5	V
I <sub>K</sub>	Analog port diode current	$V_{NC}$ , $V_{NO}$ , $V_{COM} < 0$	-50		mA
I <sub>NC</sub>	ON-state switch current		-200	200	
I <sub>NO</sub> I <sub>COM</sub>	ON-state peak switch current <sup>(6)</sup>	$V_{NC}$ , $V_{NO}$ , $V_{COM} = 0$ to $V_{+}$	-400	400	mA
$V_{I}$	Digital input voltage range		-0.5	4.6	V
I <sub>IK</sub>	Digital input clamp current (3)(4)	V <sub>I</sub> < 0	-50		mA
I <sub>+</sub>	Continuous current through V <sub>+</sub>			100	mA
I <sub>GND</sub>	Continuous current through GND		-100		mA
		PW package		108	
$\theta_{JA}$	Package thermal impedance (7)	RGT package		TBD	°C/W
		RSV package		TBD	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

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<sup>(2)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

<sup>(3)</sup> All voltages are with respect to ground, unless otherwise specified.

<sup>(4)</sup> The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>(5)</sup> This value is limited to 4.6 V maximum.

<sup>(6)</sup> Pulse at 1-ms duration <10% duty cycle

<sup>(7)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.



## **ELECTRICAL CHARACTERISTICS FOR 4.3-V SUPPLY<sup>(1)</sup>**

 $T_A = -40$ °C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CO	ONDITIONS	TA	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Analog Switch	II.			,	'				
Analog signal range	$V_{\rm COM}, \ V_{\rm NO}, V_{\rm NC}$					0		V <sub>+</sub>	V
ON-state	r <sub>on</sub>	$V_{NO}$ or $V_{NC} = 2.5 \text{ V}$ ,	Switch ON,	25°C	4.3 V		0.3	0.45	Ω
resistance	·on	$I_{COM} = -100 \text{ mA},$	See Figure 16	Full	1.0 1			0.5	
ON-state	<b>A</b> ::	$V_{NO}$ or $V_{NC} = 2.5 \text{ V}$ ,	Switch ON,	25°C	40.1/		0.05	0.07	_
resistance match between channels	$\Delta r_{on}$	$I_{COM} = -100 \text{ mA},$	See Figure 16	Full	4.3 V			0.1	Ω
ON-state		$V_{NO}$ or $V_{NC} = 1 \text{ V}$ ,	Switch ON,	25°C	4614		0.02	0.1	
resistance flatness	r <sub>on(flat)</sub>	1.5 V, 2.5 V, $I_{COM} = -100 \text{ mA},$	See Figure 16	Full	4.3 V			0.1	Ω
		$V_{NO}$ or $V_{NC} = 0.3 \text{ V}$ ,		25°C		-20	5	20	
NC, NO OFF leakage current	I <sub>NO(OFF)</sub> , I <sub>NC(OFF)</sub>	$V_{COM} = 3.0 \text{ V},$ or $V_{NO} \text{ or } V_{NC} = 3.0 \text{ V},$ $V_{COM} = 0.3 \text{ V},$	See Figure 17	Full	4.3 V	-90		90	nA
		$V_{NO}$ or $V_{NC} = 0.3 \text{ V}$ ,		25°C		-20	5	20	
NC, NO ON leakage current	I <sub>NO(ON)</sub> , I <sub>NC(ON)</sub>	$V_{COM}$ = Open, or $V_{NO}$ or $V_{NC}$ = 3.0 V, $V_{COM}$ = Open,	See Figure 18	Full	4.3 V	-90		90	nA
		$V_{NO}$ or $V_{NC}$ = Open,		25°C		-20	5	20	
COM ON leakage current	I <sub>COM(ON)</sub>	$V_{COM} = 0.3 \text{ V},$ or $V_{NO}$ or $V_{NC} = \text{Open},$ $V_{COM} = 3.0 \text{ V},$	See Figure 18	Full	4.3 V	-90		90	nA
Digital Control Inpu	uts (IN1-2, IN3	-4) <sup>(2)</sup>						<u> </u>	
Input logic high	V <sub>IH</sub>			Full	4.3 V	1.5		4.3	V
Input logic low	V <sub>IL</sub>			Full	4.3 V	0		1	V
Input leakage	In . In	V <sub>IN</sub> = 3.6 V or 0		25°C	4.3 V		0.5	10	nA
current	I <sub>IH</sub> , I <sub>IL</sub>	VIN = 3.0 V 01 0		Full	4.5 V	·		50	шА

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

 <sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
 (2) All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## **ELECTRICAL CHARACTERISTICS FOR 4.3-V SUPPLY (continued)**

 $T_A = -40$ °C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST C	ONDITIONS	TA	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t <sub>ON</sub>	$V_{COM} = V_+,$ $R_1 = 50 \Omega,$	C <sub>L</sub> = 35 pF	25°C Full	4.3 V		17	23 25	ns
Turn-off time	toff	$V_{COM} = V_+,$	C <sub>L</sub> = 35 pF	25°C	4.3 V		12	32	ns
rum-on time	OFF	$R_L = 50 \Omega$ ,	о_ = 35 рі	Full	4.5 V			35	113
Break-before-make time	t <sub>BBM</sub>	$\begin{split} &V_{NC}=V_{NO}=V_{+},\\ &R_{L}=50~\Omega, \end{split}$	C <sub>L</sub> = 35 pF	25°C Full	4.3 V	2	9	30 35	ns
Charge injection	$Q_{\mathbb{C}}$	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C <sub>L</sub> = 1 nF	25°C	4.3 V		139		рС
NC, NO off capacitance	$C_{NC(OFF)}, \ C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 19	25°C	4.3 V		50		pF
NC, NO ON capacitance	C <sub>NC(ON)</sub> , C <sub>NO(ON)</sub>	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 19	25°C	4.3 V		160		pF
COM ON capacitance	C <sub>COM(ON)</sub>	V <sub>COM</sub> = V <sub>+</sub> or GND, Switch ON,	See Figure 19	25°C	4.3 V		160		pF
Digital input capacitance	Cı	$V_I = V_+ \text{ or GND}$		25°C	4.3 V		2.5		pF
Bandwidth	BW	$R_L = 50 \Omega$ ,	Switch ON	25°C	4.3 V		35		MHz
OFF isolation	O <sub>ISO</sub>	$R_L = 50 \Omega$ , f = 100  kHz,	Switch OFF	25°C	4.3 V		-71		dB
Crosstalk	X <sub>TALK</sub>	$R_L = 50 \Omega,$ f = 100 kHz,	Switch ON	25°C	4.3 V		-73		dB
Total harmonic distortion	THD	$R_L = 600 \ \Omega,$ $C_L = 50 \ pF,$	f = 20 Hz to 20 kHz	25°C	4.3 V		0.003		%
Supply					,				
Positive supply	1	$V_1 = V_+ \text{ or GND},$	Switch ON or OFF	25°C	4.3 V		0.15	0.4	^
current	I <sub>+</sub>	$v_{\parallel} = v_{+} \cup i \cup i \cup i$	SWILCH ON OF OFF	Full	4.3 V			1.2	μΑ



## **ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY<sup>(1)</sup>**

 $V_{+} = 3 \text{ V}$  to 3.6 V,  $T_{A} = -40^{\circ}\text{C}$  to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CON	IDITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	$V_{COM}$ , $V_{NO}$ , $V_{NC}$					0		V <sub>+</sub>	V
ON-state	r <sub>on</sub>	$V_{NO}$ or $V_{NC} = 2.0 \text{ V}$ ,	Switch ON,	25°C	3 V		0.37	0.55	Ω
resistance	on	$I_{COM} = -100 \text{ mA},$	See Figure 16	Full	3 V			0.6	22
ON-state		$V_{NO}$ or $V_{NC} = 2.0 \text{ V}, 0.8$	Switch ON,	25°C	0.14		0.06	0.07	•
resistance match between channels	Δr <sub>on</sub>	$V$ , $I_{COM} = -100 \text{ mA}$ ,	See Figure 16	Full	3 V			0.1	Ω
ON-state		$V_{NO}$ or $V_{NC} = 2.0 \text{ V}, 0.8 \text{ V}$	Switch ON.	25°C	0.14		0.05	0.1	•
resistance flatness	r <sub>on(flat)</sub>	$I_{\text{COM}} = -100 \text{ mA},$	See Figure 16	Full	3 V			0.1	Ω
		$V_{NO}$ or $V_{NC} = 0.3 \text{ V}$ ,		25°C		-15	5	15	
NC, NO OFF leakage current	I <sub>NO(OFF)</sub> , I <sub>NC(OFF)</sub>	$\begin{split} &V_{COM} = 3.0 \text{ V},\\ &\text{or}\\ &V_{NO} \text{ or } V_{NC} = 3.0 \text{ V},\\ &V_{COM} = 0.3 \text{ V}, \end{split}$	See Figure 17	Full	3.6 V	-50		50	nA
		$V_{NO}$ or $V_{NC} = 0.3 \text{ V}$ ,		25°C		-15	5	15	
NC, NO ON leakage current	I <sub>NO(ON)</sub> , I <sub>NC(ON)</sub>	$V_{COM} = Open,$ or $V_{NO}$ or $V_{NC} = 3.0 \text{ V},$ $V_{COM} = Open,$	See Figure 18	Full	3.6 V	-50		50	nA
		$V_{NO}$ or $V_{NC}$ = Open,		25°C		-15	5	15	
COM ON leakage current	I <sub>COM(ON)</sub>	$\begin{aligned} &V_{COM} = 0.3 \text{ V,} \\ &\text{or} \\ &V_{NO} \text{ or } V_{NC} = \text{Open,} \\ &V_{COM} = 3.0 \text{ V,} \end{aligned}$	See Figure 18	Full	3.6 V	-50		50	nA
Digital Control Inpo	uts (IN1-2, IN3-	-4) <sup>(2)</sup>							
Input logic high	V <sub>IH</sub>			Full		1.25		4.3	V
Input logic low	V <sub>IL</sub>			Full		0		0.8	V
Input leakage	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>IN</sub> = 3.6 V or 0		25°C	3.6 V		0.5	10	nA
current	'IH, 'IL	VIN - 3.0 V 01 0		Full	3.0 V			50	11/4

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

 <sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
 (2) All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## **ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY (continued)**

 $V_{+} = 3 \text{ V to } 3.6 \text{ V}, T_{A} = -40^{\circ}\text{C to } 85^{\circ}\text{C} \text{ (unless otherwise noted)}$ 

PARAMETER	SYMBOL	TEST CON	IDITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Dynamic									
		N/ N/		25°C	3 V		20	38	
Turn-on time	t <sub>ON</sub>	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	$C_L = 35 \text{ pF}$	Full	3 V to 3.6 V			40	ns
		V V		25°C	3 V		14	34	
Turn-off time	t <sub>OFF</sub>	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	$C_L = 35 \text{ pF}$	Full	3 V to 3.6 V			35	ns
Break-before-make		V V V		25°C	3 V	3	11	35	
time	t <sub>BBM</sub>	$V_{NC} = V_{NO} = V_+,$ $R_L = 50 \Omega,$	$C_L = 35 \text{ pF}$	Full	3 V to 3.6 V	2		55	ns
Charge injection	$Q_{\mathbb{C}}$	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0,	C <sub>L</sub> = 1 nF	25°C	3 V		109		рС
NC, NO OFF capacitance	C <sub>NC(OFF)</sub> , C <sub>NO(OFF)</sub>	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 19	25°C	3 V		51		pF
NC, NO ON capacitance	C <sub>NC(ON)</sub> , C <sub>NO(ON)</sub>	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 19	25°C	3 V		162		pF
COM ON capacitance	C <sub>COM(ON)</sub>	V <sub>COM</sub> = V <sub>+</sub> or GND, Switch ON,	See Figure 19	25°C	3 V		162		pF
Digital input capacitance	C <sub>I</sub>	V <sub>I</sub> = V <sub>+</sub> or GND		25°C	3 V		2.5		pF
Bandwidth	BW	$R_L = 50 \Omega$ ,	Switch ON	25°C	3 V		35		MHz
OFF isolation	O <sub>ISO</sub>	$R_L = 50 \Omega$ , f = 100  kHz,	Switch OFF	25°C	3 V		<b>-71</b>		dB
Crosstalk	X <sub>TALK</sub>	$R_L = 50 \Omega$ , f = 100  kHz,	Switch ON	25°C	3 V		-73		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 \text{ pF},$	f = 20 Hz to 20 kHz	25°C	3 V		0.003		%
Supply									
Positive supply	ı	V = V or CND	Switch ON or OFF	25°C	3.6 V		0.015	0.2	^
current	I <sub>+</sub>	$V_1 = V_+ \text{ or GND},$	SWILCTI ON OF OFF	Full	3.0 V			0.7	μΑ



## **ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY<sup>(1)</sup>**

 $V_{+} = 2.3 \text{ V}$  to 2.7 V,  $T_{A} = -40^{\circ}\text{C}$  to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CON	DITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	$V_{COM}$ , $V_{NO}$ , $V_{NC}$					0		V <sub>+</sub>	V
ON-state	r	$V_{NO}$ or $V_{NC} = 1.8 \text{ V}$ ,	Switch ON,	25°C	2.3 V		0.45	0.6	Ω
resistance	r <sub>on</sub>	$I_{COM} = -100 \text{ mA},$	See Figure 16	Full	2.5 V			0.7	
ON-state		., ., ., ., ., ., ., ., ., ., ., ., ., .	0 % 1 0 1	25°C			0.045	0.07	
resistance match between channels	Δr <sub>on</sub>	$V_{NO}$ or $V_{NC} = 1.8 \text{ V}$ , 0.8 V, $I_{COM} = -100 \text{ mA}$ ,	Switch ON, See Figure 16	Full	2.3 V			0.1	Ω
ON-state		$V_{NO}$ or $V_{NC} = 1.8 \text{ V}, 0.8 \text{ V}$	Switch ON,	25°C			0.06	0.15	
resistance flatness	r <sub>on(flat)</sub>	$I_{COM} = -100 \text{ mA},$	See Figure 16	Full	2.3 V			0.2	Ω
		$V_{NO}$ or $V_{NC} = 0.3 \text{ V}$ ,		25°C		-10	0.5	10	1
NC, NO OFF leakage current	I <sub>NO(OFF)</sub> , I <sub>NC(OFF)</sub>	$V_{COM} = 2.3 \text{ V},$ or $V_{NO} \text{ or } V_{NC} = 2.3 \text{ V},$ $V_{COM} = 0.3 \text{V},$	See Figure 17	Full	2.7 V	-20		20	nA
		$V_{NO}$ or $V_{NC} = 0.3 \text{ V}$ ,		25°C		-10	0.1	10	
NC, NO ON leakage current	I <sub>NO(ON)</sub> , I <sub>NC(ON)</sub>	$V_{COM}$ = Open, or $V_{NO}$ or $V_{NC}$ = 2.3 V, $V_{COM}$ = Open,	See Figure 18	Full	2.7 V	-20		20	nA
		V <sub>NO</sub> or V <sub>NC</sub> = Open,		25°C		-10	0.1	10	
COM ON leakage current	I <sub>COM(ON)</sub>	$V_{COM} = 0.3 \text{ V},$ or $V_{NO}$ or $V_{NC} = \text{Open},$ $V_{COM} = 2.3 \text{ V},$	See Figure 18	Full	2.7 V	-20		20	nA
Digital Control Inj	puts (IN1-2, IN	3-4) <sup>(2)</sup>		•	'				
Input logic high	V <sub>IH</sub>			Full		1.2		4.3	V
Input logic low	V <sub>IL</sub>			Full		0		0.6	V
Input leakage	las la	V <sub>IN</sub> = 3.6 V or 0		25°C	2.7 V		0.5	10	nA
current	I <sub>IH</sub> , I <sub>IL</sub>	VIN - 3.0 V 01 0		Full	Z.1 V			50	11/1

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

<sup>(2)</sup> All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## **ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY (continued)**

 $V_{+}$  = 2.3 V to 2.7 V,  $T_{A}$  = -40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CON	DITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Dynamic		<del>'</del>							
				25°C	2.5 V		2.6	47	
Turn-on time	t <sub>ON</sub>	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	$C_L = 35 pF$	Full	2.3 V to 2.7 V			50	ns
		V V		25°C	2.5 V		16.5	34	
Turn-off time	t <sub>OFF</sub>	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	$C_L = 35 pF$	Full	2.3 V to 2.7 V			35	ns
Drook before		V V V		25°C	2.5 V	4	15	35	
Break-before- make time	t <sub>BBM</sub>	$V_{NC} = V_{NO} = V_+,$ $R_L = 50 \Omega,$	$C_L = 35 pF$	Full	2.3 V to 2.7 V	3		35	ns
Charge injection	Q <sub>C</sub>	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0,	C <sub>L</sub> = 1 nF	25°C	2.5 V		84		рС
NC, NO OFF capacitance	$C_{NC(OFF)}, \ C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 19	25°C	2.5 V		52		pF
NC, NO ON capacitance	C <sub>NC(ON)</sub> , C <sub>NO(ON)</sub>	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 19	25°C	2.5 V		163		pF
COM ON capacitance	C <sub>COM(ON)</sub>	$V_{COM} = V_{+} \text{ or GND},$	See Figure 19	25°C	2.5 V		163		pF
Digital input capacitance	C <sub>I</sub>	V <sub>I</sub> = V <sub>+</sub> or GND		25°C	2.5 V		2.5		pF
Bandwidth	BW	$R_L = 50 \Omega$ ,	Switch ON	25°C	2.5 V		35		MHz
OFF isolation	O <sub>ISO</sub>	$R_L = 50 \Omega$ , f = 100  kHz,	Switch OFF	25°C	2.5 V		-71		dB
Crosstalk	X <sub>TALK</sub>	$R_L = 50 \Omega$ , f = 100  kHz,	Switch ON	25°C	2.5 V		-73		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz	25°C	2.5 V		0.009		%
Supply				•	'				
Positive supply	1	V – V or CND	Switch ON or OFF	25°C	2.5 V		0.004	0.1	
current	I <sub>+</sub>	$V_I = V_+ \text{ or GND},$	SWILCTI ON OF OFF	Full	2.5 V			0.5	μΑ



## **ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY<sup>(1)</sup>**

 $V_{+} = 1.65 \text{ V}$  to 1.95 V,  $T_{A} = -40 ^{\circ}\text{C}$  to 85  $^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST COND	ITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	$V_{\rm COM}, \ V_{\rm NO}, V_{\rm NC}$					0		V <sub>+</sub>	٧
ON-state		$V_{NO}$ or $V_{NC} = 1.5 \text{ V}$ ,	Switch ON,	25°C	1.65 V		0.5	0.7	Ω
resistance	r <sub>on</sub>	$I_{COM} = -100 \text{ mA},$	See Figure 16	Full	1.05 V			0.8	12
ON-state		., ., ., ., ., ., ., ., ., ., ., ., ., .	0 11 1 011	25°C			0.05	0.07	
resistance match between channels	$\Delta r_{on}$	$V_{NO}$ or $V_{NC} = 1.5 \text{ V}$ , 0.6 V $I_{COM} = -100 \text{ mA}$ ,	Switch ON, See Figure 16	Full	1.65 V			0.1	Ω
ON-state		$V_{NO}$ or $V_{NC} = 1.5 \text{ V}, 0.6 \text{ V}$	Switch ON.	25°C			0.5	0.7	
resistance flatness	r <sub>on(flat)</sub>	1.5 V, 2.5 V, I <sub>COM</sub> = -100 mA,	See Figure 16	Full	1.65 V			0.8	Ω
		$V_{NO}$ or $V_{NC} = 0.3 \text{ V}$ ,		25°C		-10	0.5	10	
NC, NO OFF leakage current	I <sub>NO(OFF)</sub> , I <sub>NC(OFF)</sub>	$V_{COM} = 1.65 \text{ V},$ or $V_{NO} \text{ or } V_{NC} = 1.65 \text{ V},$ $V_{COM} = 0.3 \text{ V},$	See Figure 17	Full	1.95 V	-20		20	nA
		$V_{NO}$ or $V_{NC} = 0.3 \text{ V}$ ,		25°C		-10	0.1	10	
NC, NO ON leakage current	I <sub>NO(ON)</sub> , I <sub>NC(ON)</sub>	$V_{COM}$ = Open, or $V_{NO}$ or $V_{NC}$ = 1.65 V, $V_{COM}$ = Open,	See Figure 18	Full	1.95 V	-20		20	nA
		$V_{NO}$ or $V_{NC}$ = Open,		25°C		-10	0.1	10	
COM ON leakage current	I <sub>COM(ON)</sub>	$V_{COM} = 0.3V,$ or $V_{NO}$ or $V_{NC} = Open,$ $V_{COM} = 1.65 V,$	See Figure 18	Full	1.95 V	-20		20	nA
Digital Control Inj	outs (IN1-2, IN	I3-4) <sup>(2)</sup>			·				
Input logic high	$V_{IH}$			Full		1		4.3	V
Input logic low	$V_{IL}$			Full	_	0		0.4	V
Input leakage	la. la	V <sub>IN</sub> = 3.6 V or 0		25°C	1.95 V		0.5	10	nA
current	$I_{\rm IH},I_{\rm IL}$	VIN - 3.0 V 01 0		Full	1.30 V			50	IIA

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

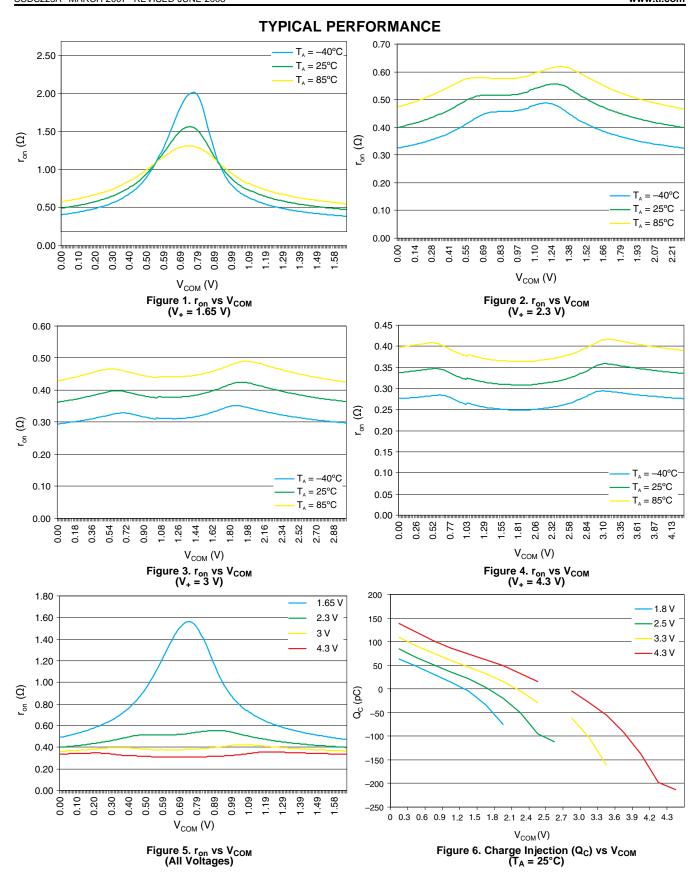
<sup>(2)</sup> All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## **ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY (continued)**

 $V_{+} = 1.65 \text{ V}$  to 1.95 V,  $T_{A} = -40 ^{\circ}\text{C}$  to 85  $^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST COND	ITIONS	TA	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Dynamic				•	'				
		V V		25°C	1.8 V		40	70	
Turn-on time	t <sub>ON</sub>	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	$C_L = 35 pF$	Full	1.65 V to 1.95 V			75	ns
		V V		25°C	1.8 V		22	45	
Turn-off time	t <sub>OFF</sub>	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	$C_L = 35 pF$	Full	1.65 V to 1.95 V			50	ns
Drook before		V V V		25°C	1.8 V	5	25	70	
Break-before- make time	t <sub>BBM</sub>	$V_{NC} = V_{NO} = V_+,$ $R_L = 50 \Omega,$	$C_L = 35 pF$	Full	1.65 V to 1.95 V	4		75	ns
Charge injection	$Q_{\mathbb{C}}$	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C <sub>L</sub> = 1 nF	25°C	1.8 V		64		рС
NC, NO OFF capacitance	$C_{NC(OFF)}, \ C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 19	25°C	1.8 V		52		pF
NC, NO ON capacitance	$C_{NC(ON)}, \ C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 19	25°C	1.8 V		164		pF
COM ON capacitance	C <sub>COM(ON)</sub>	V <sub>COM</sub> = V <sub>+</sub> or GND, Switch ON,	See Figure 19	25°C	1.8 V		164		pF
Digital input capacitance	$C_{I}$	$V_I = V_+ \text{ or GND}$		25°C	1.8 V		2.5		pF
Bandwidth	BW	$R_L = 50 \Omega$ ,	Switch ON	25°C	1.8 V		35		MHz
OFF isolation	O <sub>ISO</sub>	$R_L = 50 \Omega$ , f = 100 kHz,	Switch OFF	25°C	1.8 V		<b>-</b> 71		dB
Crosstalk	X <sub>TALK</sub>	$R_L = 50 \Omega$ , f = 100  kHz,	Switch ON	25°C	1.8 V		-73		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz	25°C	1.8 V		0.1		%
Supply					<u>.</u>				
Positive supply	1	V – V or CND	Switch ON or OFF	25°C	1.95 V		0.001	0.05	^
current	I <sub>+</sub>	$V_I = V_+ \text{ or GND},$	SWILCTI ON OF OFF	Full	1.95 V			0.15	μΑ







## **TYPICAL PERFORMANCE (continued)**

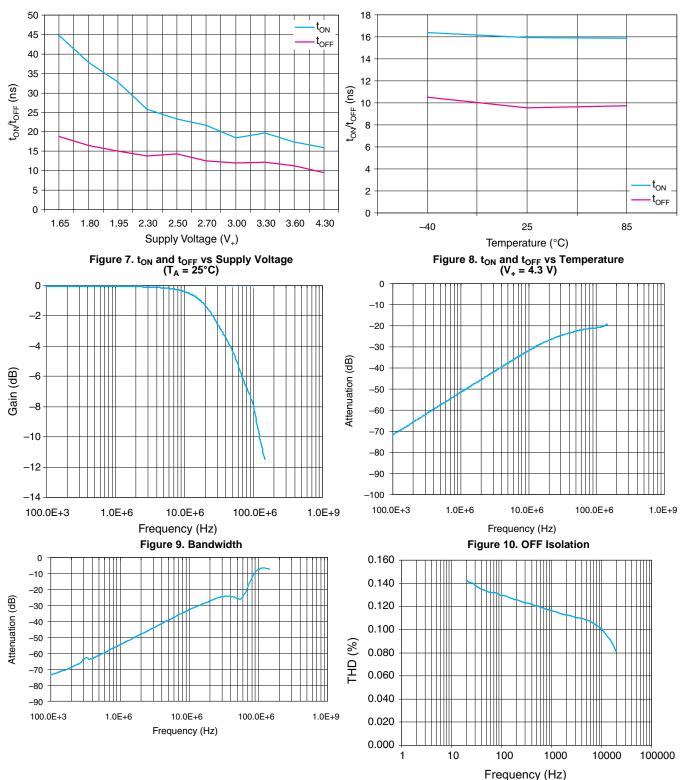


Figure 11. Crosstalk

Figure 12. Total Harmonic Distortion vs Frequency  $(V_+ = 1.8 \text{ V})$ 



## **TYPICAL PERFORMANCE (continued)**

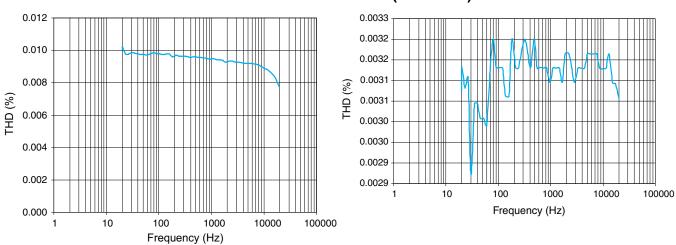


Figure 13. Total Harmonic Distortion vs Frequency  $(V_+ = 2.5 \text{ V})$ 

Figure 14. Total Harmonic Distortion vs Frequency ( $V_{+} = 3.3 \text{ V}$ )

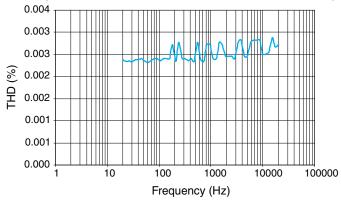


Figure 15. Total Harmonic Distortion vs Frequency  $(V_+ = 4.3 \text{ V})$ 



## PARAMETER MEASUREMENT INFORMATION

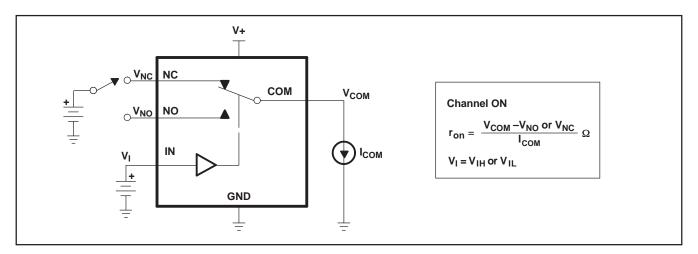


Figure 16. ON-state Resistance (ron)

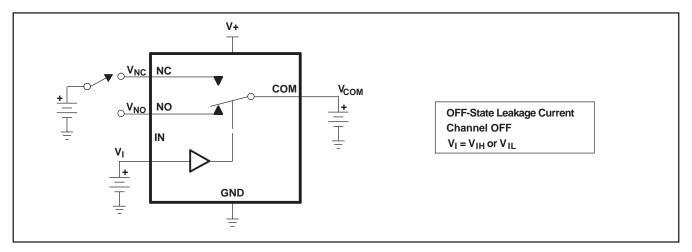


Figure 17. OFF-State Leakage Current (I<sub>NC(OFF)</sub>, I<sub>NO(OFF)</sub>, I<sub>NO(OFF)</sub>, I<sub>NO(PWROFF)</sub>, I<sub>COM(PWROFF)</sub>)



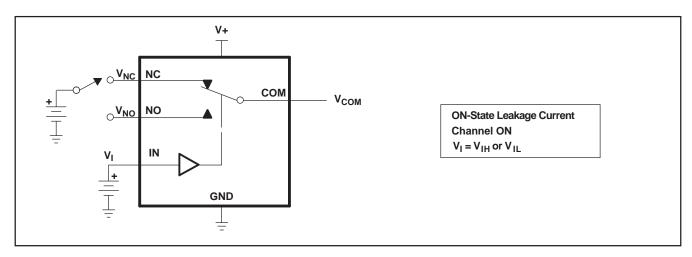


Figure 18. ON-State Leakage Current (I<sub>COM(ON)</sub>, I<sub>NC(ON)</sub>, I<sub>NO(ON)</sub>)

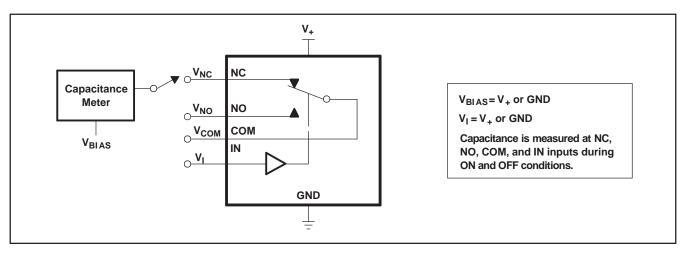
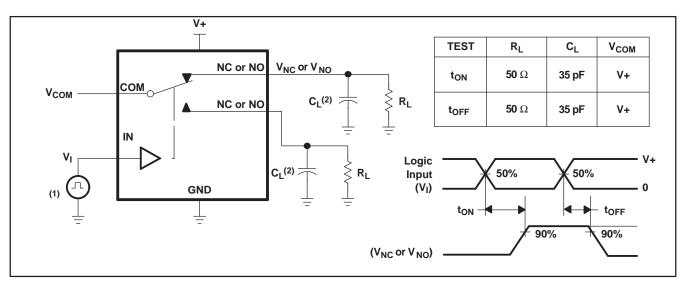


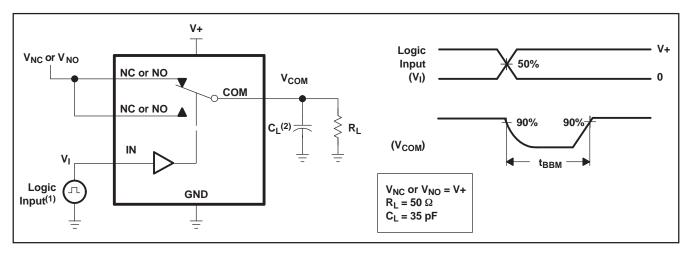
Figure 19. Capacitance (C<sub>I</sub>, C<sub>COM(ON)</sub>, C<sub>NC(OFF)</sub>, C<sub>NO(OFF)</sub>, C<sub>NC(ON)</sub>, C<sub>NO(ON)</sub>)





- A. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f < 5$  ns,  $t_f < 5$  ns.
- B. C<sub>L</sub> includes probe and jig capacitance.

Figure 20. Turn-On (ton) and Turn-Off Time (toff)



- A. C<sub>L</sub> includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .

Figure 21. Break-Before-Make Time (t<sub>BBM</sub>)



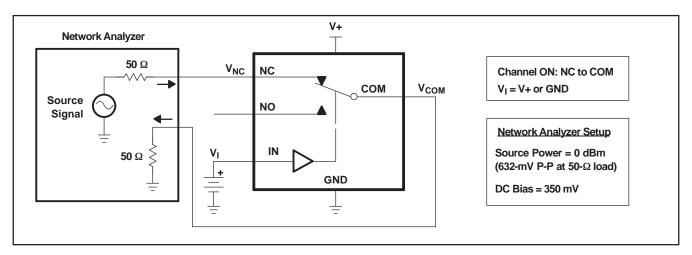


Figure 22. Bandwidth (BW)

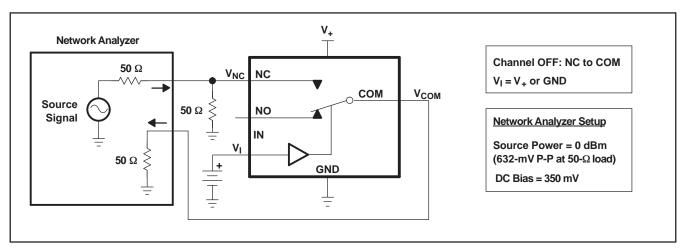


Figure 23. OFF Isolation (O<sub>ISO</sub>)

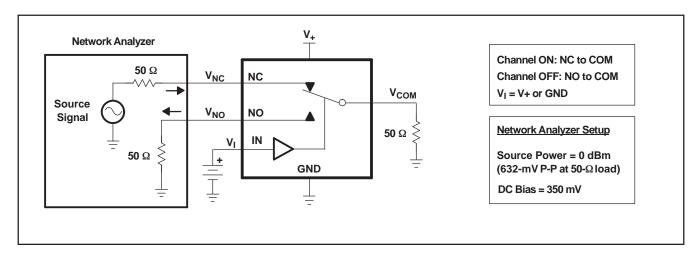
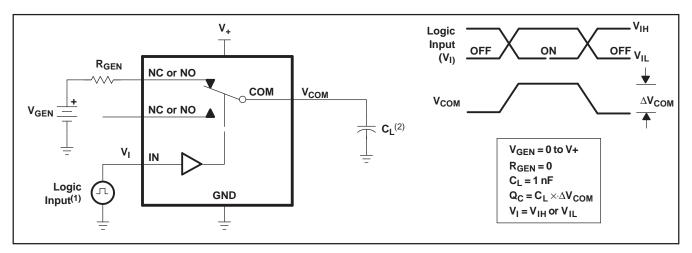


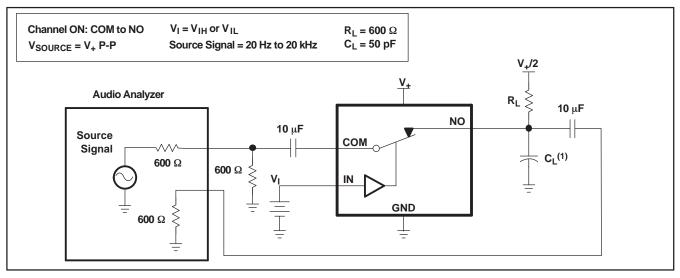
Figure 24. Crosstalk (X<sub>TALK</sub>)





- A. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- B. C<sub>L</sub> includes probe and jig capacitance.

Figure 25. Charge Injection (Q<sub>C</sub>)



A. C<sub>L</sub> includes probe and jig capacitance.

Figure 26. Total Harmonic Distortion (THD)





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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TS3A44159PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3A44159PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3A44159RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3A44159RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3A44159RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS3A44159RSVRG4	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## **PACKAGE OPTION ADDENDUM**

16-May-2011

In no event shall TI's liabilit	v arising out of such information	exceed the total purchase	price of the TI part(s	a) at issue in this document sold by	y TI to Customer on an annual basis.

## PACKAGE MATERIALS INFORMATION

13-Oct-2011 www.ti.com

## TAPE AND REEL INFORMATION

### **REEL DIMENSIONS**





### **TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### TAPE AND REEL INFORMATION

## \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A44159PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A44159RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

www.ti.com 13-Oct-2011



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A44159PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
TS3A44159RGTR	QFN	RGT	16	3000	346.0	346.0	35.0

PW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



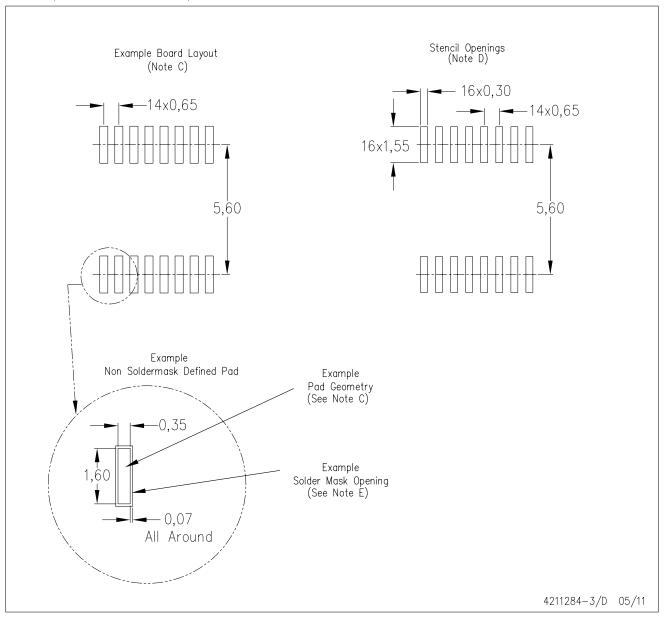
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



## PW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# RGT (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD 3,15 2,85 - A В 3,15 2,85 PIN 1 INDEX AREA TOP AND BOTTOM 0,20 REF. SEATING PLANE 0,08 0,05 0,00 Ċ 16 THERMAL PAD SIZE AND SHAPE SHOWN ON SEPARATE SHEET

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

12

- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.

13

- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

16X  $\frac{0,30}{0,18}$ 

0,50

0,10 M C A B 0,05 M C

4203495/H 10/11

F. Falls within JEDEC MO-220.



## RGT (S-PVQFN-N16)

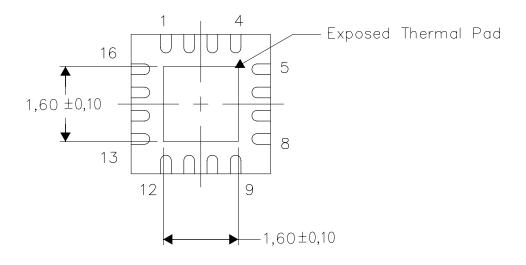
## PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

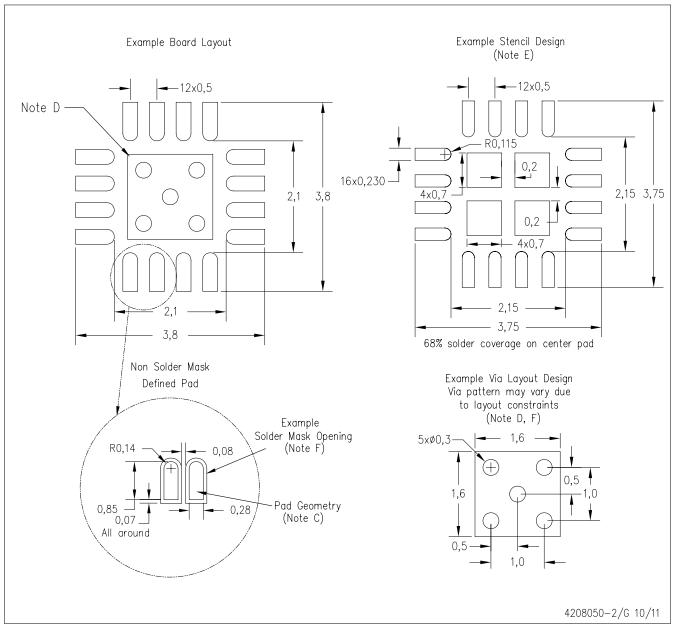
4206349-3/Q 10/11

NOTE: All linear dimensions are in millimeters



## RGT (S-PVQFN-N16)

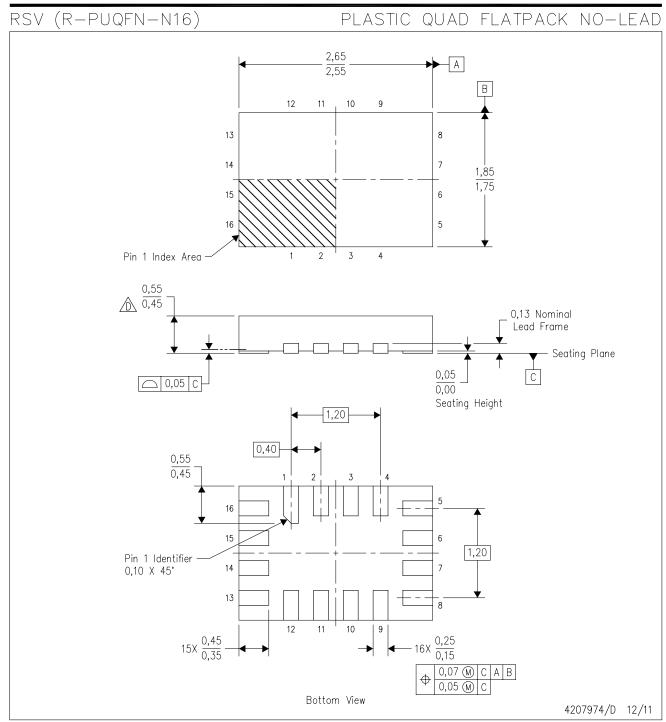
## PLASTIC QUAD FLATPACK NO-LEAD



#### NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="https://www.ti.com">www.ti.com</a>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.





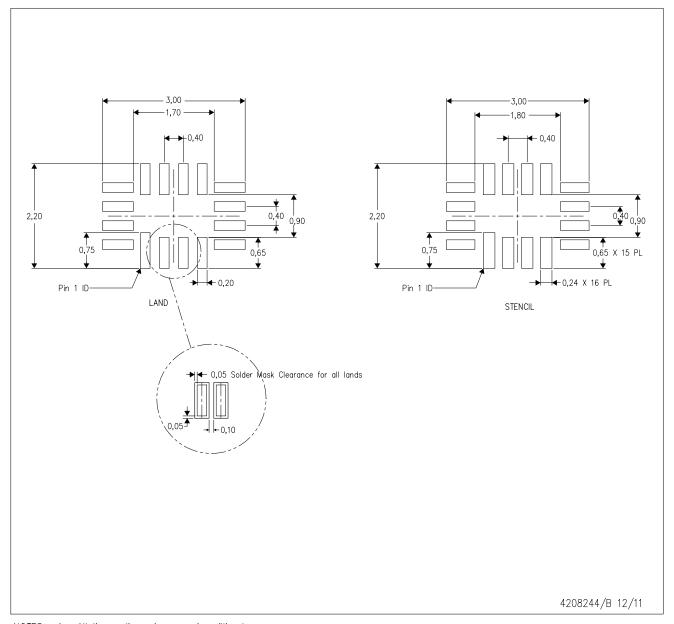
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- This package complies to JEDEC MO-288 variation UFHE, except minimum package thickness.



## RSV (R-PUQFN-N16)

## PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over—print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



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